VĚDECKÉ SPISY VYSOKÉHO UČENÍ TECHNICKÉHO V BRNĚ
Edice Habilitační a inaugurační spisy, sv. 509
ISSN 1213-418X

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DIGITAL PREDISTORTION AND ITS INTEGRATION IN THE SOFTWARE DEFINED RADIO TRANSCEIVER

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DIGITAL PREDISTORTION AND ITS INTEGRATION IN THE SOFTWARE DEFINED RADIO TRANSCEIVER

ČÍSLICOVÉ PŘEDZKRESLENÍ A JEHO INTEGRACE V SOFTWAROVĚ DEFINOVANÉM VYSÍLAČI

A THESIS OF A TALK FOR THE PROFESSORIAL APPOINTIVE PROCEDURE IN THE STUDY FIELD OF ELECTRONICS AND COMMUNICATIONS

VUTIUM

BRNO 2015

KEYWORDS
Software defined radio, digital communications, predistortion

KLÍČOVÁ SLOVA
Softwarově definované radio, digitální komunikace, předzkreslení

THE THESIS IS AT DISPOSAL AT
Department of Radio electronics
Faculty of Electrical Engineering and Communication
Technická 12
616 00 Brno
Czech Republic

ISBN 978-80-214-5201-5
ISSN 1213-418X

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About author

Roman Maršálek (1976) entered Brno University of Technology (BUT), Faculty of electrical engineering and computer science in 1994. He prepared his master thesis *Design of a synchronization algorithm for UMTS-WCDMA receiver* in a framework of EU program Socrates at ESIEE Paris, France. He graduated at the department of Control, Measurement and Instrumentation, BUT in 1999 in study program Cybernetics, Control and Measurement and received a dean's price for the excellent master thesis. Then he entered the Czech-French doctoral study program Electronics and signal processing (Electronique, traitement du signal) supported by the French government scholarship. The research work was oriented into domain of power amplifier linearization using digital signal predistortion and was done in cooperation between BUT and ESIEE Paris/ Université de Marne la Vallée. He defended his doctoral dissertation *Contributions to the power amplifier linearization using digital baseband adaptive predistortion* in 2003 at University of Marne la Vallée, France with honors and congratulations of jury (the best possible rank for PhD dissertations in France).

Since 2004 he is with Department of Radio Electronics, BUT, where he got his habilitation in 2008 (topic *Multicarrier modulations and PAPR reduction*). In winter term of 2013/2014 he was a teaching and research fellow at Johannes Kepler University (JKU) Linz, Austria. His current teaching activities include *Wireless communication theory* and *Software radio* courses. In the past he also took a part in the teaching of courses such as *Radio and mobile communications*, *Communication systems*, *Signals and systems*, *HF and microwave technique* or *Microprocessor techniques*. He currently supervises three Ph.D. students. Four of the students supervised already obtained their Ph.D. degree, one of them in a Czech-French doctoral study (jointly with Prof. Baudoin and Prof. Villegas from Université Paris-Est). He regularly accepts the students from foreign institutions working on their projects in the framework of Socrates (LLP) program.

Roman Maršálek has been a principal investigator of several research projects such as *Algorithms for improvement of efficiency of digital baseband predistorters* (Grant Agency of the Academy of Sciences of the Czech Republic), *Algorithms and subsystems for software defined and cognitive multicarrier radio* (Czech Science Foundation, GAČR), *Time-frequency approach for the Czech Republic business cycle dating* (GAČR) or *Optical measurements of explosions* (Technology Agency of the Czech Republic, TAČR). He took a part in other national and international research projects as a team member, such as *Agile RF Transceivers and Front-Ends for Future Smart Multi-Standard Communications Applications* (ENIAC JU), COST action *IC0803 RF/Microwave Communication Subsystems for Emerging Wireless Technologies* or *RSTN - Radio for Smart Transmission Networks* (TAČR)

He was involved in the industrial projects and seminars such as a lecture on OFDM and CDMA (Flextronics), lecture on software defined radio (Motorola) or a project *Measurement, analysis and modeling of FM signal interferences and influence of interferences on RDS-TMC messages reception* (Škoda Auto). Since 2013 he is a member of an executive committee of the Czechoslovakia Section of IEEE, responsible for student activities. Since 2014 he is an area editor of *International Journal of Electronics and Communications* (former AEÜ).

1 Introduction

Research described in this thesis has been carrier out at the Department of Radio Electronics, Brno University of Technology. It has been done in cooperation with several other colleagues - Tomáš Götthans, Jiří Blumenstein and Ph.D. students Martin Pospíšil and Jiří Dvořák. I would like to express my gratitude to all of them.

In the current communication and wireless networking systems, the radio signals with non-constant envelope are mainly used in order to fulfill ever-increasing demands for high data rates. In order to gain better Power Amplifier (PA) efficiency, the amplifiers are often used close to the saturation point. Such a constellation leads to significant nonlinear distortion of the transmitted signals with undesirable effects on the increased bit error rate and spurious transmission into adjacent channels.

A huge family of methods for the compensation of power amplifier nonlinearities exists, such as feed-forward techniques [1], Cartesian feedback [2] and (usually Digital and adaptive) PreDistortion (DPD). This thesis deals mainly with DPD, performed in the complex baseband domain. Description of the core parts of this thesis is based on our recent publications [3], [4] and [5]. A part of the results has been obtained during the research in the framework of ENIAC JU project 270683-2, ARTEMOS.

2 Digital Predistortion principle

The first real experiments with digital predistortion date back to 1980's [6]. The predistortion principle is based on the artificial distortion of the transmitted signal with the nonlinear function that models the inverse characteristics of the PA. The inverse function can be implemented in several ways differing in the complexity as well as in the performance of the linearization. The simplest way is based on the Look Up Table (LUT) or polynomial function approximation. These two approaches cannot compensate for the memory effects in the amplifier, significant especially for the wide-band input signals. In order to count for the memory effects, approaches like polynomials with memory, Volterra series or generalized memory polynomials have been proposed. The predistortion is often adaptive - the inverse function adapts to PA changes caused by changing carrier frequency, power or temperature variations.

Digital predistorters are often implemented in the Field Programmable Gate Arrays (FPGA) [7] and first experiments using the Software Defined Radio platforms have been published, as in [8]. Currently, single-purpose chips for digital predistortion [9] or specialized IP cores for programmable devices [10] are also available. Unfortunately, these two solutions are not easy to use in the commercial software defined radios, moreover often equipped with small or medium-sized FPGA devices.

The basic principle of adaptive digital predistortion for linearization of power amplifiers is shown in Figure 1. Here we consider the baseband predistortion, where a transmitted baseband signal is upconverted (in digital or analog form) to desired carrier frequency. A part of the transmitted signal is fed back to the baseband through a directional coupler (and attenuator) to have a reference signal for a predistorter adaptation.

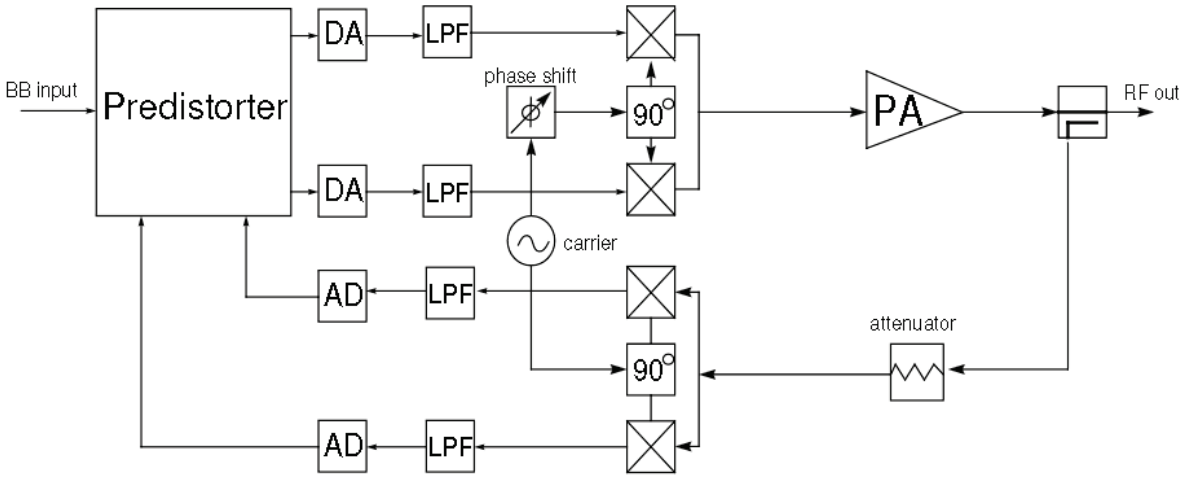

Figure 1: Digital predistortion principle.

3 Look Up Table predistortion

3.1 Algorithm and its implementation

In the described experiment, we consider a complex gain LUT predistorter similarly as in [11]. The predistorter output z_p at time instant n is then

$$z_p(n) = z(n) f_{pre}(i), \tag{1}$$

where $f_{pre}(i)$ is a content of LUT entry i representing the inverse of the PA characteristics and $z(n)$ is a sample of modulated baseband signal. Note that in order to compensate for both amplitude and phase distortions, the LUT content is complex. The LUT can be addressed using either the instantaneous signal module or its instantaneous power. In order to get better linearization performance, the linear interpolation of the LUT entries is often done and we used it too. Recently, the advantage of the cubic interpolation has been described in [12]. The number of LUT entries can be significantly reduced in this case.

The adaptation of the predistorter has been done using an indirect-learning Recursive Least Squares (RLS) method published in [11]. In contrast to this sample-by-sample approach, we have slightly modified the algorithm to use it in the off-line block-by-block system. First the blocks of N data samples from the PA input and output are sampled, delay compensated (it's need is illustrated e.g. in [13]) and the predistorter LUT is computed from these blocks. Then the predistorter is applied to a new block of signal. In such a case we do not use any forgetting factor and the modulator output is used for the adaptation instead of the predistoter (that is not yet used in the adaptation phase) output. This leads to the adaptation formula:

$$f_{pre}(i) = \frac{\sum_{l=1}^{N} z(l) z_a(l)}{\sum_{l=1}^{N} |z_a(l)|^2}, \tag{2}$$

where z_a is the PA output (divided by the desired gain of the system after predistortion) and z the digital modulator output (i.e. PA input). You can notice that such a method is very simple and thus suitable for implementation in programmable devices. A block schematic of the indirect learning adaptation is shown on Fig. 2. Prior the implementation we analyzed the requirements on the bit representation of predistorter and its adaptation

Table 1: LUT predistortion bit widths: minimal (b_{min}), simulated (b_{sim}) and used for implementation (b_{imp}).

signal	b_{min}	b_{sim}	b_{imp}
z	12	14	18
z_p	12	14	18
z_a	12	14	18
z_{aG}	12	14	18
G_{ref}	9	9	18
numerator	21	24	36
denominator	21	24	36
z_{post}	12	14	18

algorithm. First the minimal widths (b_{min}) were determined from the range of signals used for MATLAB model. Next, the simulation of the algorithm was run several times and additional bits were added in order to guarantee the adaptation stability (b_{sim}). Then the bit widths used for the implementation (the size of elementary FPGA Xilinx multiplier is 18x18 bits) were chosen. All the values are shown in Table 1, with the signals corresponding to schematic in Fig. 2. Note that signals *numerator* and *denominator* correspond to the sums in the numerator and denominator in Eq. 2.

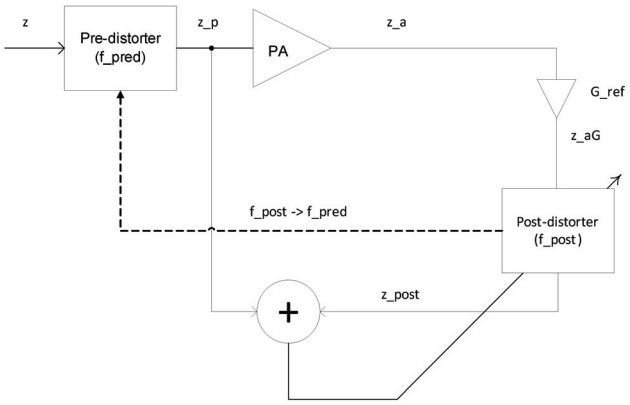

Figure 2: Indirect learning architecture.

Prior to implementation in programmable device, it is possible to simulate the algorithm performance in fixed point precision using MATLAB. Result of such simulation, in comparison with the standard MATLAB floating point simulation of predistortion adaptation is show in Fig. 3 for an example of the Long Term Evolution (LTE) adaptation signal. Here, the amplitude and phase corrections, i.e., the LUT entries are shown. You can notice only slight difference between the fixed and floating point results.

3.2 Integration to USRP software defined radio

3.2.1 Software defined radio

A software radio (SR) is defined [14] as *a transmitting/receiving device in which the digitization is at (or very near to) antenna and all of the processing required is performed by software in high speed signal processing elements.* Although many other definitions can be found in the literature ("more user friendly radio", "radio with personalization and software

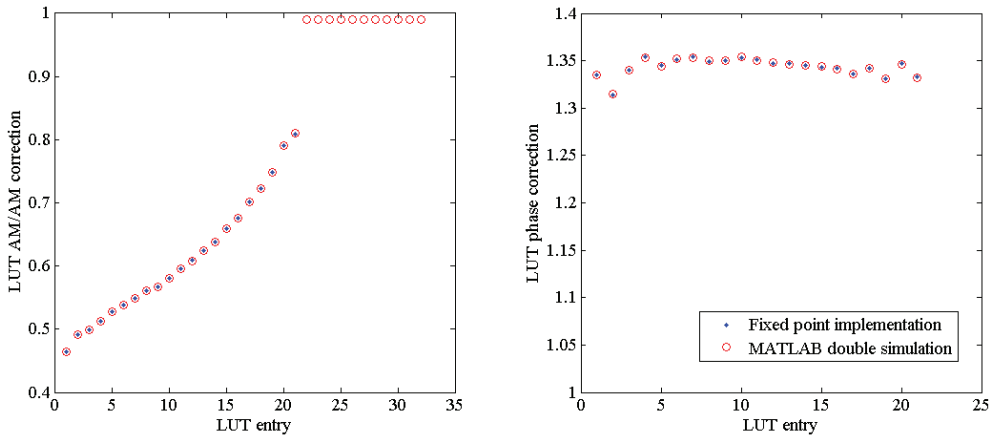

Figure 3: Comparison of floating and fixed point simulation in MATLAB

download on demand" etc.), such a definition is probably the most appropriate from the hardware design point of view.

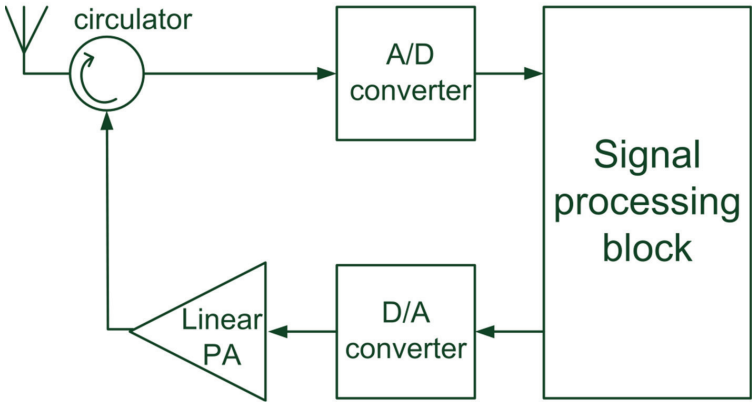

Figure 4: Basic concept of a software radio

As can be seen from Fig. 4, the ideal software radio contains only a signal processing block, data converters, a power amplifier, a circulator and an antenna. There are several drawbacks associated with such a concept, such as a need for the high speed data converters, requirements on signal processing in real-time or capability to process weak signals. Thus, the software radio represents rather an ultimate goal and the most of real current transceivers employ rather a concept called Software Defined Radio (SDR). An SDR is defined [14] as *a radio in which the receive digitization is performed at some stage downstream from the antenna, typically after wideband filtering, low noise amplification, and down conversion to a lower frequency in subsequent stages – with a reverse process occurring for the transmit digitization. Digital signal processing in flexible and reconfigurable functional blocks defines the characteristics of the radio*

Various software defined radios are currently available on the market. Table 2 provides the parameters of selected devices of two probably most-widespread families in the research community - Universal Software Radio Peripheral (USRP) from Ettus Research (now National instruments) and Blade RF designed and fabricated by NUAND company. Except USRP1, all devices of USRP family are MIMO capable and can be used with various front-

Device type	FPGA	Bus	Bandwidth	A/D converters
USRP	Altera	USB 2.0	8 MHz	12bit, 64 MSa/s.
USRP2	Spartan 3A	Gig.ETH	25 MHz	14bit, 100 MSa/s.
USRP N210	Spartan 3A	Gig.ETH	25MHz	14bit, 100 MSa/s.
USRP E110	Spartan 3A+OMAP3	Gig.ETH	8MHz	12bit, 64 MSa/s.
USRP X310	Kintex 7	1/10Gig.ETH	120MHz	14bit, 200 MSa/s.
BladeRF x40	Cyclone 4E	USB 3.0	28 MHz	12 bit, 40 MSa/s.
BladeRF x115	Cyclone 4E+ARM9	USB 3.0	28 MHz	12 bit, 40 MSa/s.

Table 2: Parameters of selected SDR devices

ends such as LFTX/RX (covering frequency range from DC to 30 MHz), WBX (50-2200 MHz), TVRX2 (50-860 MHz) or the most recent CBX-120 (1200-6000 MHz). The BladeRF radios are MIMO expandable to 2x2 (x40) or 4x4 (x115) and work with a fixed front-end based on a LMS6002 chip for 300-3800 MHz frequency range (with extension to 60kHz-300 MHz) coverage.

3.2.2 Integration of digital predistortion

In order to test new techniques for communication systems, the use of an Universal Software Radio Peripheral (USRP) from Ettus company (now National Instruments) is very popular among researchers in both academia and industry. In many cases, the USRP is used in connection with a host PC, and the more advanced data processing is done in PC using either GNU radio, GNU radio companion graphical environment, Simulink or LabView as in [8].

From among the variety of the USRP devices, we have used the USRP N200. Its main board is equipped with the Xilinx Spartan 3A-DSP 1800 device and dual 14 bits A/D converters with 100 MSa./s. sampling rate. The USRP can be used in connection with various front-end modules ranging from DC to 6 GHz frequency bands.

In the USRP, data from the antenna are received by the front-end module, converted to digital domain by the A/D converters and subsequently Digitally Down-Converted (DDC) to baseband. The USRP source code is ready to be modified by the custom Verilog code to be included in several positions of the transceiver chain. In the receiver, the user can access data from the front-end, input to the DDC, output of the DDC or baseband data. The transmitting chain is very similar. In our experiments we have accessed the final baseband data.

For the communication of the modules in the general USRP N2x0 design, an open source Wishbone bus is used. In this particular case the bus has 32-bit data width and 32-bit address space. There is one wishbone master (WB master) in the USRP design, which is the ZPU soft processor. The bus is configured to have 16 slaves, but some of the slave positions are not used. Memory map is quite complex because bus granularity is used. The interface (implemented by TESLA a.s. in the framework of joint ENIAC JU project ARTEMOS) to the general USRP design is inserted between the DUC/DDC (Digital Up Converter/ Digital Down Converter) and the VITA RX/TX chain where the baseband IQ samples are processed (see Figure 5). By default, the USRP has two RX chains to be able to receive on two channels. As this functionality is not needed for the intended application, the second RX chain was removed from the design to save the FPGA resources.

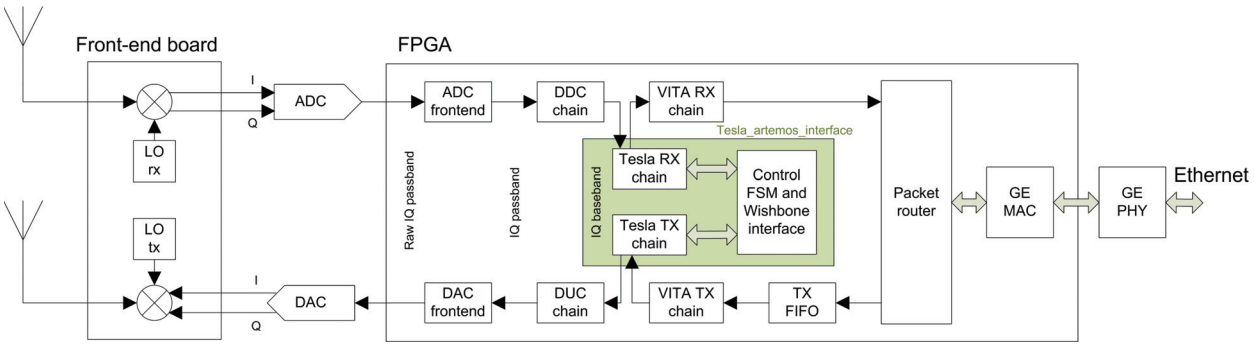

Figure 5: Integration into USRP system.

3.2.3 Experimental workplace

The workplace setup is shown in Fig. 6. The USRP N200 TX is used with the WBX front-end module, whose output is amplified with the PA working in nonlinear region. This PA to linearize was a monolithic InGap HBT amplifier GVA84+ from Mini Circuits with approximately 20 dB power at 1dB compression. At the PA output a directional coupler CP0603GN with -34dB coupling from AVX company has been used to get the attenuated part of PA output fed back to the USRP RX chain. The PA output is also monitored using a Rohde&Schwarz FSQ 3 spectrum and vector signal analyzer to get the output spectrum, IQ diagram and to analyze EVM. The USRP has been controlled via a control software in PC (a GNU radio companion plus custom programmed part). Using this software the sampling frequencies and RX/TX gains can be changed.

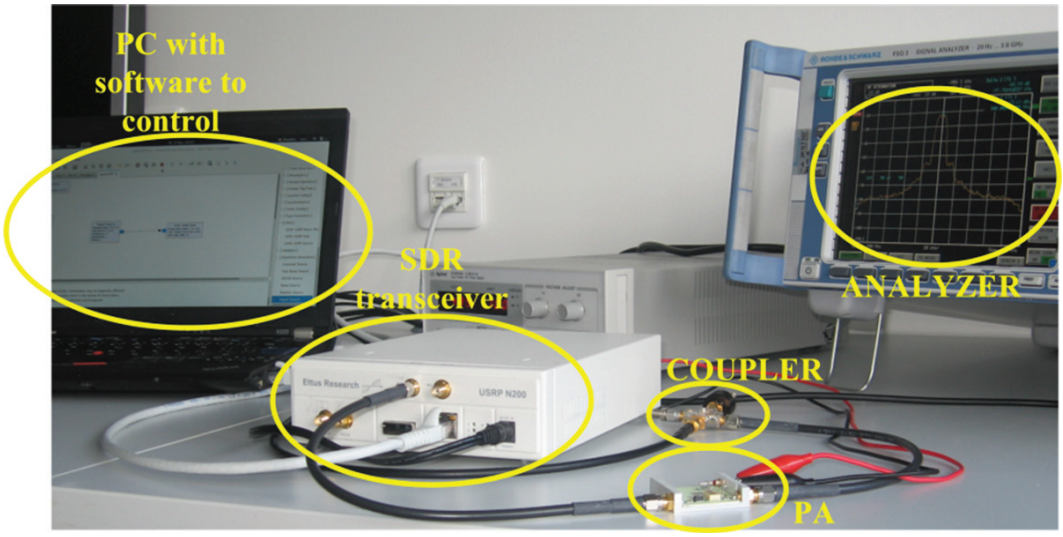

Figure 6: Measurement workplace.

3.2.4 Measurement results

The PA has been fed up first with QPSK and 16-QAM signals (2 MHz bandwidth). The measured AM/AM characteristic is shown in black color in Figure 7. You can observe a dispersion of points in the characteristics caused possibly by the PA memory effects or incoherency of RX and TX oscillators. The effect of predistortion on the input signal is

shown on the predistorter AM/AM characteristic (in cyan). The predistorter has been also tested with the LTE uplink signal with 3.84MHz bandwidth, generated by a generator SMU 200A with a LTE option. The spectra of the amplifier output with and without predistortion are shown in Figure 8 for 16QAM and LTE signals. You can observe around 10 dB reduction in the adjacent channels close to the main channel, i.e. in the regions where the filtration of the undesirable components is impossible. The application of predistorter also leads to EVM improvement (at working point from 3.3% to 1.7% RMS).

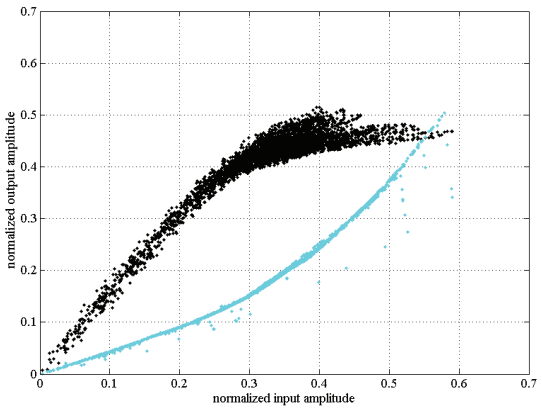

Figure 7: Measured AM/AM characteristics of PA (black) and of DPD (cyan).

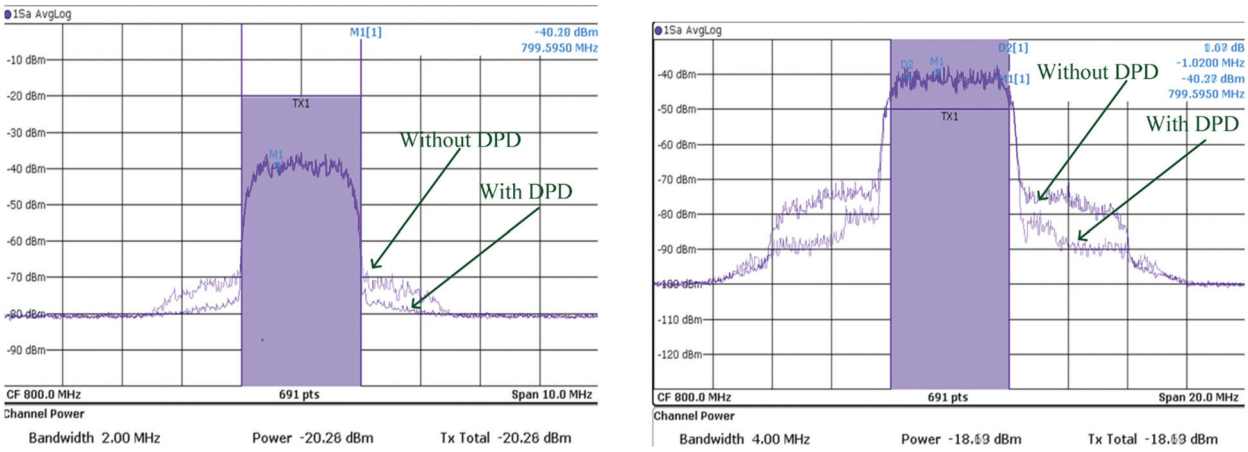

Figure 8: Spectra of the PA output without and with predistortion for 16-QAM (left) and LTE (right) signals.

4 LUT predistorters versus polynomial-based predistorters

4.1 Polynomial models of power amplifiers

In early stage of predistortion algorithm research, the memoryless nature of RF power amplifier was supposed. The measurements of the intermodulation distortion in function of

frequency at PA input carried out by Kenney [15] for three different amplifiers have shown this result: the low power (0.5W) GaAs PA exhibited negligible memory effects, and they become more significant with increasing power of PA (the 30W LDMOS PA and 45W BJT PA were measured). From frequency dependency of nonlinear distortion, one can assume a hypothesis that more the PA input signal has larger band, more memory effects are exhibited by the PA.

There are several approaches to model PA's including memory effects - one of them is to employ the behavioral models describing the PA as the nonlinear function without explicit correspondence to physical phenomenas.

The relationship between input $z(n)$ and output $z_a(n)$ complex envelopes for nonlinear system, e.g. PA, with memory can be expressed in the form of complex Volterra series [16]:

$$z_a(n) = \sum_{i=0}^{Q} h_1(i) z(n-i) + \sum_{i=0}^{Q}\sum_{j=0}^{Q}\sum_{k=0}^{Q} h_3(i,j,k) z(n-i) z(n-j) z^*(n-k) \ldots + \epsilon(n) \quad (3)$$

where h_1 and h_3 are called lowpass equivalent Volterra kernels, n denotes discrete time, Q the memory length and ϵ the modeling error. Such model is usually too complex to be used in real-time applications.

Much more practical approach to model the power amplifier with memory effects is the memory polynomial model that can be constructed:

$$z_a(n) = \sum_{k=1}^{K}\sum_{q=0}^{Q} f_{kl} z(n - qn_0) \left| z(n - qn_0) \right|^{k-1} \quad (4)$$

where K, Q are the degree of nonlinearity and the memory depth of the nonlinear system (e.g. amplifier), n_0 is the elementary delay of memory and f_{kl} are the coefficients of the model. Besides the Volterra and memory polynomial models, some other models based on the polynomial structure have been proposed such as a Orthogonal Memory Polynomials (OMP) [17] or Dynamic Deviation Reduction (DDR) models [18].

We applied the memory polynomial model to model the characteristics of the real measured power amplifier working in 800 MHz band. The data from the PA input and output have been obtained using the USRP N200 devices with a WBX daughter board tuned to carrier-frequency 2 GHz. OFDM signal with 512-points FFT size, 256 data subcarriers and 256 null subcarriers has been used. The model adaptation was based on the least squares error minimization:

$$J(n) = \sum_{l=1}^{n} \left(z_a(n) - z_m(n) \right)^2, \quad (5)$$

as shown on Fig. 9. In [5] a Recursive Least Squares (RLS) algorithm [19] with variable model order was compared with an Order Recursive Least Squares (ORLS) algorithm [20].

The results (AM/AM curves) for two distinct sets of memory length and polynomial order are shown on Fig. 10.

4.2 Comparison of LUT and polynomial predistorters

Recently [4], we have compared the performance of the predistorter based on the LUT with the memory polynomial-based predistorters. It has been shown that the predistortion performance highly depends on the PA and its operating point. Example results of PA

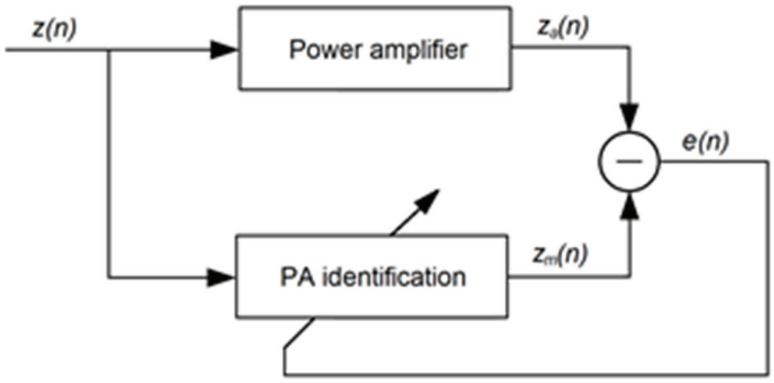

Figure 9: PA model adaptation

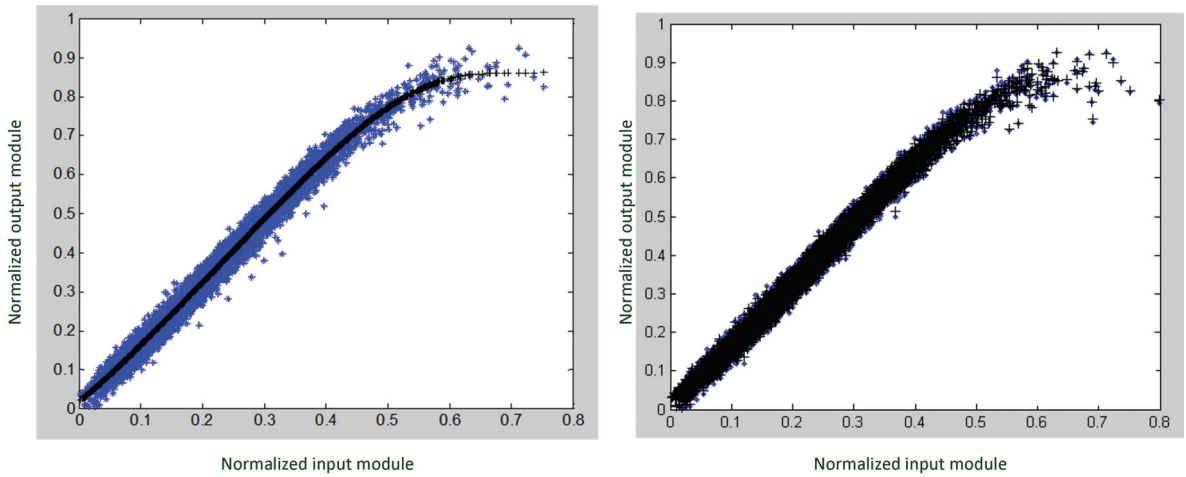

Figure 10: Memory polynomial model fits to measured PA signal: K=7,Q=0 (left) and K=3,Q=23 (right)

output spectras are shown on Fig. 11 and 12. From these figures it can be concluded, that the performance of the LUT predistorter is comparable to 3-rd order polynomial predistorter.

4.3 Time delay adjustment in the feedback path

A careful adjustment of the delay in the feedback path (see Fig. 2) of the indirect learning digital predistortion algorithm must be performed. Otherwise the delay mismatch could be interpreted as the PA memory effects and the complexity of the algorithm for the DPD can rapidly increase. We thus used an integer + fine fractional delay estimation and compensation with the use of modified Farrow interpolator structure and the MSE criterion, see Fig. 14.

Farrow interpolator [21] makes use of the polynomial-based interpolation of input samples $x\left(nT_s\right)$ to get the new samples at different sampling period T_{out}:

$$y(rT_{out}) = \sum_{m=0}^{M} v_m(n)(\mu_r)^m, \tag{6}$$

where M is the polynomial order, $v_m(n) = \sum_{i=-U/2+1}^{U/2} x\left[(n-i)T_s\right] c_m(i)$, with c_m being the

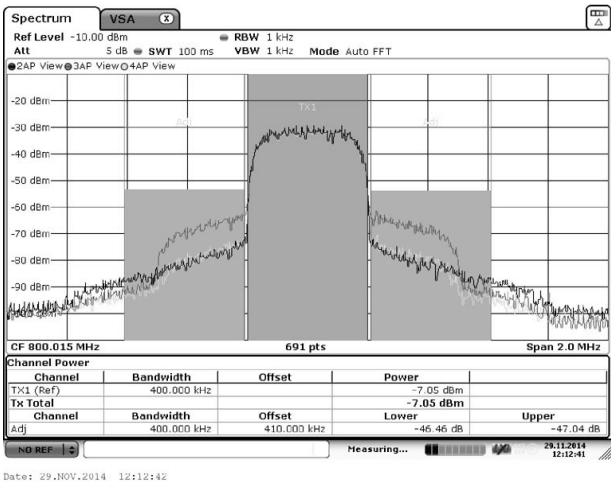

Figure 11: Power spectrum for example PA in 800 MHz band excited with 16QAM signal: TR2 - black curve denotes LUT DPD, TR3 - green color is PA without DPD, and TR4 - orange trace is DPD with orthogonal memory polynomial with orders $K = 7$ and $Q = 3$.

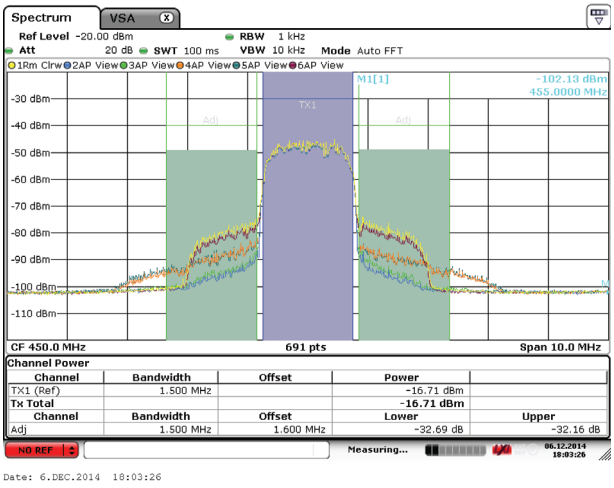

Figure 12: Power spectrum for example PA in 450 MHz band: TR1 - yellow is PA without DPD, TR2 - blue curve denotes DDR2 DPD ($K = 11$, $Q = 0$), TR3 - green color is PA with DDR DPD ($K = 7$, $Q = 0$), and TR4 - orange trace is DDR2 DPD ($K = 3$, $Q = 0$), TR5 - dark green is DPD with LUT (cubic interpolation) and TR6 - purple is PA without DPD for different output power.

filter coefficients and U the length of the individual sub-filters. A (normalized) fractional interval μ_r represents a distance between r-th output and $n-$th input sample, see Fig. 13:

$$\mu_r = r\frac{T_{out}}{T_s} - n = \frac{rT_{out} - nT_s}{T_s}, \tag{7}$$

The measured AM/AM characteristic of PA without and with fine fractional time delay adjustment are shown in Fig. 15.

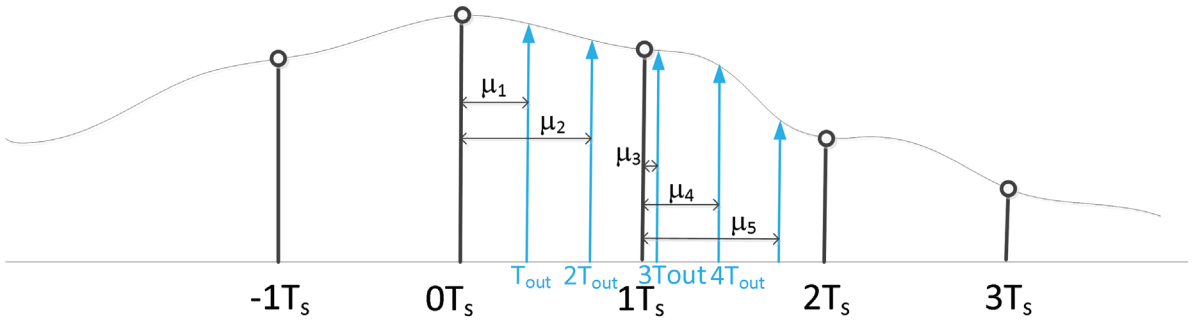

Figure 13: Illustration of Farrow interpolation resampling

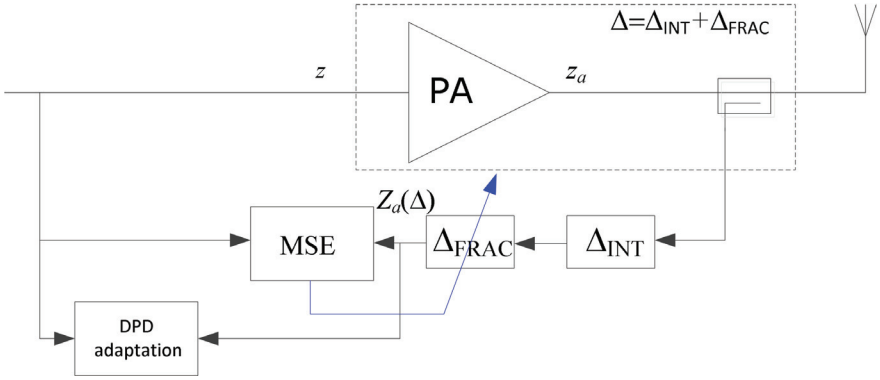

Figure 14: Block schematic of time-delay adjustment

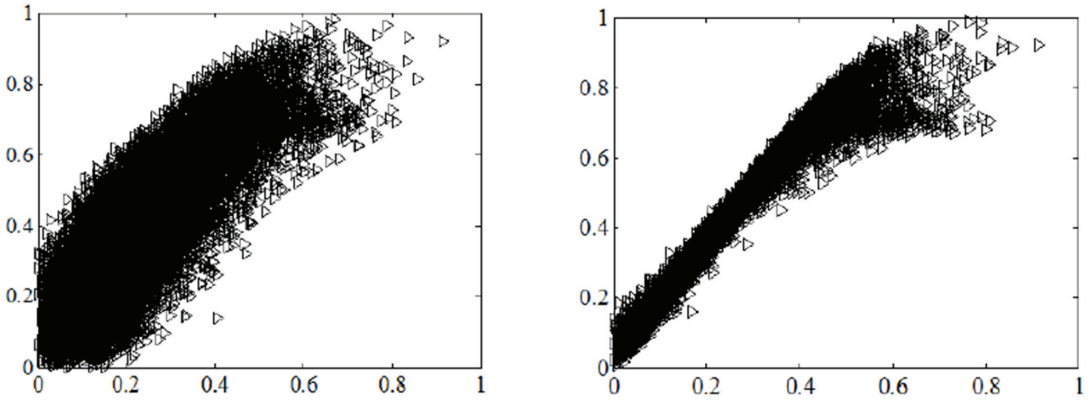

Figure 15: AM/AM without (left) and with (right) fine delay estimation

5 Conclusions

The experiments with the low-complexity digital predistortion and its integration into software defined radio device have been described in this thesis. Although the first research papers in this domain emerged more than 25 years ago, this research area is still of high interest of the researchers. Current research in the predistortion is often oriented into predistortion of mobile devices [22] or predistortion in MIMO systems, taking into account the crosstalk between various front-ends [23]. This represent a challenging task especially in the case of future massive MIMO systems [24] with hundreds of antennas. The search for optimal order of predistorters with memory is also currently investigated, see [5]. Note

that besides the digital predistortion, the analog predistortion with adaptive mechanism can also be used [25]. The predistortion performance is affected by other RF impairments, such as IQ imbalances that can be corrected for, see [26] or filters. An interesting application of anti-aliasing filter pre-correction is shown in [27]. Digital predistortion is used not only for class AB or B amplifiers, but its application to switched mode PA's has also been examined [28] recently. The predistortion can be used in various digital communication systems or wireless local area networks. Its application in the future fifth generation (5G) [29] of wireless communications, based on new modulation waveforms such as Filter Banks MultiCarrier [30] is also of high importance.

Finally note that the power amplifier nonlinearity can be, besides other RF imperfections, used as a device fingerprint allowing to provide an additional level of mobile device identification [31].

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Abstrakt

Současné a budoucí komunikační systémy a systémy bezdrátových lokálních sítí jsou založeny na přenosu signálů s nekonstantní obálkou. Typickým příkladem jsou například standard LTE, nebo WiFi systém IEEE 802.11a. Současně, pro zvýšení účinnosti komunikačních zařízení, je žádoucí provozovat koncové stupně výkonových zesilovačů v blízkosti saturace. Tyto navzájem protichůdné požadavky vedou na nutnost použití metod pro linearizaci koncových stupňů, případně na aplikaci metod pro redukci dynamiky vysílaných signálů.

Jednou z nejpoužívanějších linearizačních metod je metoda číslicového předzkreslení, založená na číslicovém zkreslení signálu pomocí nelineární charakteristiky inverzní k charakteristice zesilovače. Tento dokument prezentuje část výzkumu v dané oblasti prováděného na Ústavu radioelektroniky v období let 2011-2015.

Po stručném úvodu do problematiky jsou popsány prováděné experimenty s číslicovými předzkreslovači v základním pásmu. První část je věnována předzkreslovačům ve formě vyhledávací tabulky (LUT). Pro takový předzkreslovač je popsán i proces integrace do softwarově definovaného transceiveru USRP. Ve druhé části je provedeno srovnání LUT předzkreslovačů s předzkreslovači založenými na polynomiálních modelech. Jsou také prezentovány výsledky měření na reálných zesilovačích a popsány základní modely zesilovačů.

Přestože první experimenty s metodou číslicového předzkreslení byly prováděny již v osmdesátých létech minulého stolení, je tato metoda i v dnešní době aktuální a perspektivní i v kontextu budoucích sítí mobilních komunikací páté generace.