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LINEAR FUNCTION BLOCKS FOLLOWING RECENT TRENDS IN ANALOG CIRCUIT DESIGN

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LINEÁRNÍ FUNKČNÍ BLOKY SLEDUJÍCÍ AKTUÁLNÍ TRENDY V NÁVRHU ANALOGOVÝCH OBVODŮ

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Analogové zpracování signálu, proudový mód, napěťový mód, transadmitanční mód, transimpedanční mód, smíšený mód, kmitočtový filtr, multifunkční filtr, univerzální filtr, frekvenčně agilní filtr, fázovací článek prvního řádu, filtr vyššího řádu, nediferenční filtr, diferenční filtr, KHN-ekvivalent, simulátor induktoru, násobič kapacity, napětím řízený rezistor, kmitočtově závislý negativní rezistor, kvadraturní oscilátor, vícefázový oscilátor.

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Since 2008, Dr. Herencsár also serves as invited reviewer in many SCI-E Journals including IEEE TCAS-I, IEEE TCAS-II, IEEE TIM, etc., and international conferences and completed more than 150 reviews. Dr. Herencsár is IEEE Senior Member (StM'07–M'12–SM'15). For year 2015, he was elected as IEEE Czechoslovakia Section CAS/COM/SP Joint Chapter Chair and appointed as IEEE Czechoslovakia Section Membership Development Officer. He is also Senior Member of the IACSIT and IRED, Member of the IAENG, ACEEE, RS, and Committee Member of the IACSIT Electronics and Electrical Society (EES).

1 INTRODUCTION

Research in analog signal processing is significantly considered in the analyses and application possibilities of different active building blocks (ABBs). Operational amplifier played an important role as an active building block in the research. Therefore, enormous number of publications exist in the literature on various analog electronics circuits using operational amplifiers. However, new integrated analog circuit applications have emerged and the performance requirements for analog circuits have changed. Operational amplifiers circuits have limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product of the active element. Furthermore, the limited slew-rate of operational amplifiers affect the large-signal for high-frequency operation. When wide bandwidth, low-power consumption and low-voltage operation are needed simultaneously, the voltage-mode operational amplifier becomes very complex. These disadvantages can be eliminated by using recently introduced high-performance ABBs. By following the most recent trends and progress in this research field, this habilitation thesis is organized as described below.

- The first part of the habilitation thesis is focused on single-ended (S-E) and fully-differential (F-D) first-order all-pass filter (APF) design working in voltage-, current-, mixed-, or dual-mode and fulfill one or simultaneously more from the listed requirements [1]–[22].
- The next section discuses quadrature or multiphase oscillator design with specific features and/or using special types of function blocks [2], [3], [23]–[25].
- The third part deals with second-order analog frequency filters, where the main intention is on minimal configuration multifunction or universal filter structures design without changing the circuit topology [26]–[31]. Simultaneously, higher-order topologies are also discussed [32].
- Finally, in the last section passive component emulator circuits such as grounded voltage controlled positive resistor (GVCPR), lossy/lossless floating/grounded inductance simulators, floating frequency dependent negative resistor (FDNR), or floating capacitance multipliers are discussed [33]–[38].

As the full thesis for habilitation consists in total of 38 papers having been elaborated by the author in close collaboration with his highly recognized colleagues since 2011, this short version of thesis discusses results published in [10], [25], [26], and [38].

2 RECENT TRENDS IN ANALOG CIRCUIT DESIGN

2.1 Novel All-Pass Filter Design Methods

Frequency filters are circuits that shape the spectrum of the input signal in order to obtain an output signal with the desired frequency content. Hence, they have wide area of application in instrumentation, automatic control, communication systems, video signal processing, and broadcasting systems. For phase equalization and for a frequency dependent delay design, while the amplitude of the output signal over the desired frequency range is kept constant, all-pass filters are generally used. Hence, APFs are basic building blocks that are widely used in analog signal processing. During last years the progress in this research area is significant and the biggest challenge was and still is to propose such circuits that fulfill one or simultaneously more from the following requirements: 1. Consist of only one active building block (ABB), 2. employ single grounded capacitor, 3. no passive resistors are required i.e. resistorless circuit, 4. provide electronic control of pole frequency (f_{p}) and/or filter pass-band gain (G_0), 5. suitable for low-voltage and low-power operation at higher-frequency region (tens of MHz), and/or 6. partially/fully cascadable.

Using minimal number of ABBs in the filtering topologies it is expected that the total chip area would be smaller in case of on-chip fabrication. It is well-known that the terminal parasitic capacitances of ABBs in series with floating capacitors in the structure may cause additional unwanted pole and degrade the high-frequency behavior of filters. Therefore, the use of grounded capacitor is welcomed and very important from the monolithic integration point of view. The control of f_{p} and/or filter G_0 is also important feature that makes the proposed circuits attractive in many applications. In practice, the adjustment of these parameters

can be done by (i) means of transconductance parameter g_{m}, (ii) varying the intrinsic resistance of low-impedance current input of ABBs, (iii) by using n-channel metal-oxide-semiconductor field-effect transistor (NMOS) working in triode operation as voltage controlled resistor (VCR), or (iv) by changing the current and/or voltage gain of ABB. Recently, there is also an increasing trend on the design of low-voltage circuits with low-power consumption due to the requirement of efficient portable electronic systems with long battery lifetime. From the filters' cascadability point of view, from circuit theory it is well-known fact that the input and output impedances of circuits should be ideally equal to the extreme values (zero $\{0\}$ or infinity $\{\infty\}$ impedances for short), depending on the type of input and output operational modes. For current-mode (CM) circuits the input and output impedance should be 0 and ∞ while for voltage-mode (VM) circuits ∞ and 0, respectively. Note that due to this property there is no need for additional current followers or voltage buffers for cascading and it decreases the number of active elements in the final solution.

By following the above listed requirements and the most recent trends, the discussion has been done on numerous voltage-, current-, transadmittance-, and transimpedance-mode S-E or F-D first-order APFs [1]–[22].

2.1.1 Current-Mode First-Order Filter Design

The proposed CM topology for realizing various first-order filters is shown in Fig. 2.1 [10]. It can be seen that it employs an inverting amplifier with the voltage gain of $-\beta$. The employed inverting amplifier should have high input and low output impedances ideally. Analysis of the proposed CM configuration of Fig. 2.1 gives the following responses:

(i) Non-inverting low-pass transfer function (TF) and phase response:

$$\frac{I_{\mathrm{lp1}}}{I_{\mathrm{in}}} = \frac{1}{1+sC_1R_1}, \tag{2.1}$$

$$\varphi_{\mathrm{lp1}}(\omega) = -\tan^{-1}(\omega C_1 R_1). \tag{2.2}$$

(ii) Non-inverting high-pass TF and phase response:

$$\frac{I_{\mathrm{hp1}}}{I_{\mathrm{in}}} = \frac{sC_1R_1}{1+sC_1R_1}, \tag{2.3}$$

$$\varphi_{\mathrm{hp1}}(\omega) = \frac{\pi}{2} - \tan^{-1}(\omega C_1 R_1). \tag{2.4}$$

(iii) Inverting low-pass TF and phase response:

$$\frac{I_{\mathrm{lp2}}}{I_{\mathrm{in}}} = \frac{\beta\frac{R_1}{R_2}}{1+sC_1R_1}, \tag{2.5}$$

$$\varphi_{\mathrm{lp2}}(\omega) = \pi - \tan^{-1}(\omega C_1 R_1). \tag{2.6}$$

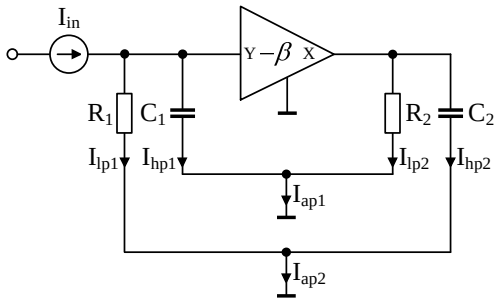


Fig. 2.1: Developed CM configuration for realizing first-order filters

(iv) Inverting high-pass TF and phase response:

$$\frac{I_{\rm hp2}}{I_{\rm in}} = \frac{s\beta C_2 R_1}{1+sC_1R_1}, \tag{2.7}$$

$$\varphi_{\rm hp2}(\omega) = -\frac{\pi}{2} - \tan^{-1}(\omega C_1 R_1). \tag{2.8}$$

Here, the pole frequency of the filter from Fig. 2.1 is found as $\omega_{\rm p} = 1/(C_1R_1)$. Further, if $\beta = 1$, the following responses can be obtained:

(v) Inverting all-pass TF and phase response if $R_2 = R_1$ as:

$$\frac{I_{\rm ap1}}{I_{\rm in}} = \frac{I_{\rm hp1}}{I_{\rm in}} + \frac{I_{\rm lp2}}{I_{\rm in}} = -\frac{1-sC_1R_1}{1+sC_1R_1}, \tag{2.9}$$

$$\varphi_{\rm ap1}(\omega) = \pi - 2\tan^{-1}(\omega C_1 R_1). \tag{2.10}$$

(vi) Non-inverting all-pass TF and phase response if $C_2 = C_1$ as:

$$\frac{I_{\rm ap2}}{I_{\rm in}} = \frac{I_{\rm lp1}}{I_{\rm in}} + \frac{I_{\rm hp2}}{I_{\rm in}} = \frac{1-sC_1R_1}{1+sC_1R_1}, \tag{2.11}$$

$$\varphi_{\rm ap2}(\omega) = -2\tan^{-1}(\omega C_1 R_1). \tag{2.12}$$

It should be noted that the all-pass filters of [11] and [12] can simultaneously realize only one all-pass response. In order to obtain output currents at high-output-impedance terminals from the structure in Fig. 2.1, a current buffer is required for each current. For this purpose a current follower (CF) can be a good choice [39]. However, a CF has an input parasitic resistance denoted by $R_{\rm p}$. The output of the developed inverting all-pass filter connected to the input of a CF is shown in Fig. 2.2. Considering the required conditions for the inverting all-pass response as $R_1 = R_2$ and $\beta = 1$, the corresponding gain and phase responses are computed as:

$$\frac{I_{\rm ap1}}{I_{\rm in}} = -\frac{1-sC_1R_1}{1+\frac{R_{\rm p}}{R_1}+sC_1(R_1+3R_{\rm p})}, \tag{2.13}$$

$$\varphi_{\rm ap1}(\omega) = \pi - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_1(R_1+3R_{\rm p})}{1+\frac{R_{\rm p}}{R_1}}\right). \tag{2.14}$$

From (2.13) and (2.14), one should select $R_1 \geq 3R_{\rm p}$ to prevent the loading effect.

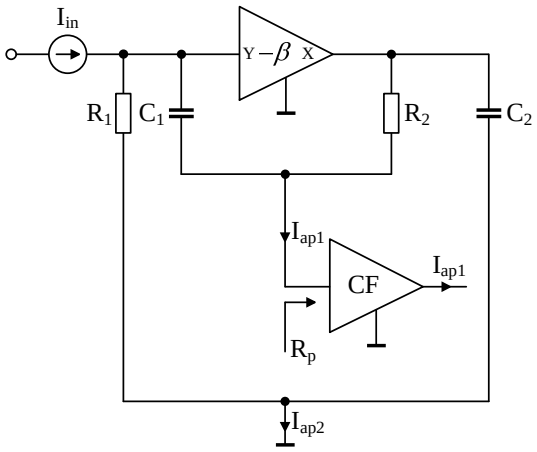


Fig. 2.2: The output of the suggested all-pass filter connected to the input of a CF

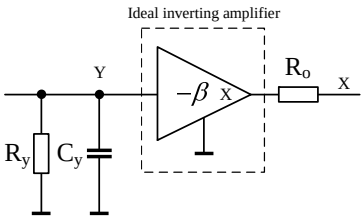


Fig. 2.3: Inverting amplifier with parasitic impedances

Analysis of Parasitic Effects

The parasitic of the employed amplifier can be considered as parallel capacitance and resistance at its input terminal ($R_y \parallel C_y$) and output resistance (R_o) in series at its output terminal as shown in Fig. 2.3. Since R_y and C_y appears in parallel with externally connected R_1 and C_1, their effects can be neglected with selecting $R_1 \ll R_y$ and $C_1 \gg C_y$. Considering the output resistance R_o of the inverting amplifier, while the current responses I_{lp1} and I_{hp1} remain undisturbed, I_{lp2} and I_{hp2} and their corresponding phase responses convert to:

$$\frac{I_{lp2}}{I_{in}} = -\frac{\beta R_1}{(1+sC_1R_1)(R_2+R_o+sC_2R_2R_o)}, \tag{2.15}$$

$$\varphi_{lp2}(\omega) = \pi - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_2 R_2 R_o}{R_2+R_o}\right), \tag{2.16}$$

$$\frac{I_{hp2}}{I_{in}} = -\frac{\beta s C_2 R_1 R_2}{(1+sC_1R_1)(R_2+R_o+sC_2R_2R_o)}, \tag{2.17}$$

$$\varphi_{hp2}(\omega) = -\frac{\pi}{2} - \tan^{-1}(\omega C_1 R_1) - \tan^{-1}\left(\frac{\omega C_2 R_2 R_o}{R_2+R_o}\right). \tag{2.18}$$

It can be seen that a second pole appears in the TF of the filter due to the nonzero output resistance of the amplifier as:

$$\omega_{p2} = \frac{R_2+R_o}{C_2R_2R_o} = \frac{1}{C_2R_o} + \frac{1}{C_2R_2}, \tag{2.19}$$

Thus one should select $R_o \ll R_2$ in order to neglect the effect of the second pole. Similarly, for the all-pass responses we can obtain:

$$\frac{I_{ap1}}{I_{in}} = -\frac{R_1\left(\beta - sC_1(R_2+R_o) - s^2C_1C_2R_2R_o\right)}{(1+sC_1R_1)(R_2+R_o+sC_2R_2R_o)}, \tag{2.20}$$

$$\varphi_{ap1}(\omega) = \pi - \tan^{-1}\left(\frac{\omega C_1(R_2+R_o)}{\beta+\omega^2C_1C_2R_2R_o}\right) - \tan^{-1}(\omega C_1R_1) - \tan^{-1}\left(\frac{\omega C_2R_2R_o}{R_2+R_o}\right), \tag{2.21}$$

$$\frac{I_{ap2}}{I_{in}} = \frac{R_2+R_o-sC_2R_2(\beta R_1-R_o)}{(1+sC_1R_1)(R_2+R_o+sC_2R_2R_o)}, \tag{2.22}$$

$$\varphi_{ap2}(\omega) = -\tan^{-1}\left(\frac{\omega C_2R_2(\beta R_1-R_o)}{R_2+R_o}\right) - \tan^{-1}(\omega C_1R_1) - \tan^{-1}\left(\frac{\omega C_2R_2R_o}{R_2+R_o}\right). \tag{2.23}$$

Note that the proposed all-pass filter having no capacitor connected in series to the X terminal of the inverting amplifier; accordingly, it can be worked at higher frequencies.

The inverting amplifier used in the structure of the proposed CM all-pass filter can be implemented with two NMOS transistors as shown in Fig. 2.4(a) [10]. The gain of the amplifier is found as:

$$\frac{V_o}{V_{in}} = -\beta = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}, \tag{2.24}$$

where $(W/L)_i$ is the ratio of the channel width to channel length of the ith ($i = 1, 2$) transistor.

Noise Analysis

The inverting amplifier including noise sources of the transistors is shown in Fig. 2.4(b). The noise density sources of the transistors can be represented as:

$$\overline{dV_1^2} = 4kTR_{\text{eff1}}df, \tag{2.25}$$

$$\overline{dV_2^2} = 4kTR_{\text{eff2}}df, \tag{2.26}$$

where k is the Boltzmann's constant, T is absolute temperature in Kelvin, and $R_{\text{eff}i}$ is the effective thermal noise resistance of the ith transistor, which is given as:

$$R_{\text{eff}i} = \frac{\frac{2}{3}}{g_{\text{m}i}} + R_{\text{G}i} + R_{\text{B}i}(n-1)^2. \tag{2.27}$$

In (2.27), $\frac{\frac{2}{3}}{g_{\text{m}}}$ represents the channel noise effect, R_{G} is the poly gate resistor and R_{B} is the substrate resistance [40]. The substrate resistance is multiplied a factor of $(n-1)^2$ where $n-1$ is equal to the ratio of the bulk transconductance to the transconductance of the transistor, i.e. $\frac{g_{\text{mb}}}{g_{\text{m}}}$.

The noise voltage of transistor M_2 in Fig. 2.4(b) is visible at its source terminal. Thus the equivalent input noise density of the amplifier is found as:

$$\overline{dV_{\text{ieq}}^2} = \overline{dV_1^2} + \frac{g_{\text{m2}}^2}{g_{\text{m1}}^2}\overline{dV_2^2} = \overline{dV_1^2} + \frac{1}{\beta^2}\overline{dV_2^2}. \tag{2.28}$$

Assuming matched transistors $g_{\text{m1}} \cong g_{\text{m2}}$ and consequently $\beta = 1$, the total equivalent input noise density is $\overline{dV_{\text{ieq}}^2} \cong \overline{2dV_1^2}$.

For the all-pass filter of Fig. 2.1, there are additional thermal noises due to the external resistors R_1 and R_2. Thus, the total equivalent input noise of the proposed CM all-pass filter can be given as:

$$\overline{dV_{\text{ieq-ap}}^2} = 4kTR_1df + 2\overline{dV_1^2} + \frac{1}{\beta^2}4kTR_2df. \tag{2.29}$$

From (2.29), an equivalent input resistance ($R_{\text{ieq-ap}}$) for noise calculation purpose can be defined as:

$$R_{\text{ieq-ap}} = R_1 + 2R_{\text{eff1}} + \frac{1}{\beta^2}R_2. \tag{2.30}$$

The bandwidth (BW) of the equivalent input noise density is limited by the external capacitor C_1. Thus the integrated noise of this resistor-capacitor combination (or all-pass filter) is found by taking the integral over all frequencies as:

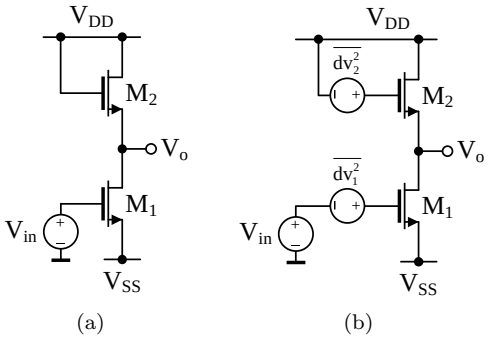


Fig. 2.4: (a) NMOS-based inverting amplifier, (b) noise model

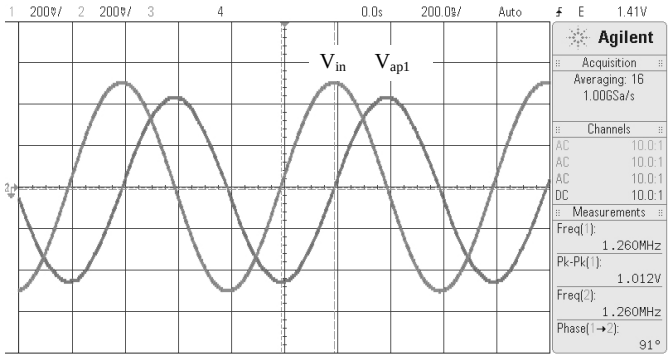


Fig. 2.5: Measured time domain response of the I_{ap1}

$$\overline{V_{\mathrm{ieq\text{-}ap}}^2} = \int_0^\infty \frac{\overline{dV_{\mathrm{ieq\text{-}ap}}^2}}{1+\left(\frac{f}{BW}\right)^2} = 4kTR_{\mathrm{ieq\text{-}ap}}BW\frac{\pi}{2}, \tag{2.31}$$

where

$$BW = \frac{1}{2\pi R_{\mathrm{ieq\text{-}ap}}C_1}. \tag{2.32}$$

Substituting (2.32) into (2.31), the integrated noise is simply found as kT/C_1. For wideband systems the integrated noise is important, thus to reduce the noise we have to select larger capacitances which obviously will increase the power consumption [40].

Experimental Verification

The behavior of the I_{ap1} response of the proposed all-pass filter has also been verified by experimental measurements. In measurements the readily available array transistors CD4007UB [41] by Texas Instruments with ±15 V dc supply voltages have been used. To perform the measurements of the proposed current-mode filter, the circuit was extended by voltage-to-current and current-to-voltage converters realized by OPA860 ICs [42] by Texas Instruments with dc power supply voltages equal to ±5 V. Since the OPA 860 generally behaves as CCII+, the measured voltage compared to the I_{ap1} is shifted in the phase by 180°. The experiments have been performed with $R_1 = R_2 = 1.2$ kΩ and $C_1 = C_2 = 100$ pF. In this case the 90° phase shift is at $f_0 \cong 1.26$ MHz. The time-domain response of the measured I_{ap1} response of the all-pass filter is shown in Fig. 2.5 in which a sine-wave input of 1 V peak-to-peak and frequency of 1.26 MHz was applied to the filter. From Fig. 2.5 it can be seen that the phase shift in the I_{ap1} output against the input is 91°. It is also observed that the experimental results are in close proximity with the ideal ones as expected. Nevertheless, the discrepancy among ideal, simulation and experimental results fundamentally arises from non-idealities of NMOS transistors.

2.2 Recent Progress in Oscillator Design

Typical application area of all-pass filters is the design of sinusoidal oscillators, which can be implemented by cascading the APF to a lossy integrator in a closed loop [2], [3]. In general, quadrature oscillators are important circuits for various communication applications, wherein there is a requirement of multiple sinusoids that are 90° phase shifted, e.g. in quadrature mixers and single-sideband modulators, or for measurement purposes in the vector generator or selective voltmeters. Therefore, the research was also focused on oscillator design with specific features and/or using special types of function blocks [23]. Similarly, a very compact active CMOS-RC realization of sinusoidal oscillator capable of generating four quadrature voltage outputs was proposed in [24]. The governing laws for the condition of oscillation (CO) and the frequency of oscillation (FO) are

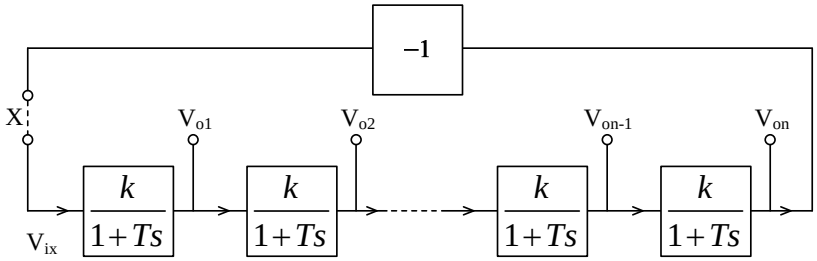


Fig. 2.6: Generalized block diagram of an n-phase sinusoidal oscillator [43], [44]

single-resistance-controlled (SRC), which allow independent FO tuning. Unlike previously reported SRC-based sinusoidal oscillators based on ABB-based approach, this direct CMOS realization provides a much reduced transistor count circuit and consequently offers a low power solution.

2.2.1 Multiphase Sinusoidal Oscillators (MSOs)

The generalized structure of an n-phase sinusoidal oscillator is shown in Fig. 2.6 [43], [44]. It consists of n cascaded lossy integrators and a unity gain inverting amplifier in a closed loop. For lossy integrator sections k is the low-frequency stage gain, and T is the system time constant [43]. The system loop gain is given by:

$$L(s) = \frac{V_{\mathrm{on}}(s)}{V_{\mathrm{ix}}(s)} = -\left(\frac{k}{1+Ts}\right)^n. \tag{2.33}$$

For oscillation to sustain, the Barkhausen criteria must be fulfilled [45]:

$$-\left(\frac{k}{1+Ts}\right)^n\Big|_{s=j\omega_0} = 1. \tag{2.34}$$

That is:

$$(1+j\omega_0 T)^n + k^n = 0. \tag{2.35}$$

Eq. (2.35) can be rewritten as:

$$\left(1+\omega_0^2 T^2\right)^{n/2} \cdot e^{jn\cdot\tan^{-1}\omega_0 T} = k^n \cdot e^{j\pi}. \tag{2.36}$$

Thus the CO and FO are found as:

$$\mathrm{CO}: \quad k = \left(1+\omega_0^2 T^2\right)^{1/2}, \tag{2.37}$$

$$\mathrm{FO}: \quad \omega_0 = \frac{1}{T}\tan\left(\frac{\pi}{n}\right). \tag{2.38}$$

Substituting ω_0 of Eq. (2.38) in Eq. (2.37) gives:

$$\mathrm{CO}: \quad k = \left[1+\tan^2\left(\frac{\pi}{n}\right)\right]^{1/2}. \tag{2.39}$$

From Eq. (2.39) it can be seen that the oscillation condition depends on the number of the oscillation phases, n. It is obvious that the oscillation occurs when $n \geq 3$. The output number of the oscillator is n, each output voltage V_{on} is shifted in phase by $180°/n$.

2.2.2 Novel Current- and Voltage-Mode MSOs

In [25], on CM & VM MSO structures have been investigated using current backward transconductance amplifiers (CBTAs). The CBTA terminal equations can be defined as [46] $I_{\mathrm{z}} = g_{\mathrm{m}}(s)(V_{\mathrm{p}} - V_{\mathrm{n}})$, $V_{\mathrm{w}} = \mu_{\mathrm{w}}(s)V_{\mathrm{z}}$,

$I_\mathrm{p} = \alpha_\mathrm{p}(s)I_\mathrm{w}$, $I_\mathrm{n} = -\alpha_\mathrm{n}(s)I_\mathrm{w}$. In these equations $\alpha_\mathrm{p}(s)$, $\alpha_\mathrm{n}(s)$, and $\mu(s)$ are respectively the current and voltage gains and they can be expressed as $\alpha_\mathrm{p}(s) = \omega_{\alpha\mathrm{p}}(1-\varepsilon_{\alpha\mathrm{p}})/(s+\omega_{\alpha\mathrm{p}})$, $\alpha_\mathrm{n}(s) = \omega_{\alpha\mathrm{n}}(1-\varepsilon_{\alpha\mathrm{n}})/(s+\omega_{\alpha\mathrm{n}})$, $g_\mathrm{m}(s) = g_\mathrm{o}\omega_\mathrm{gm}(1-\varepsilon_\mathrm{gp})/(s+\omega_\mathrm{gm})$, and $\mu_\mathrm{w}(s) = \omega_\mathrm{w}(1-\varepsilon_\mathrm{w})/(s+\omega_\mathrm{w})$ whereas $|\varepsilon_{\alpha\mathrm{p}}| \ll 1$, $|\varepsilon_{\alpha\mathrm{n}}| \ll 1$, $|\varepsilon_\mathrm{gm}| \ll 1$, and $|\varepsilon_\mu| \ll 1$. Here, g_o is the DC transconductance gain. Also, $\varepsilon_{\alpha\mathrm{p}}$ and $\varepsilon_{\alpha\mathrm{n}}$ denote the current tracking errors, ε_μ denotes the voltage tracking error, ε_gm denotes transconductance error, and $\omega_{\alpha\mathrm{p}}$, $\omega_{\alpha\mathrm{n}}$, ω_gm, ω_μ denote corner frequencies. Note that, in the ideal case, the voltage and current gains are unity i.e. $\mu_\mathrm{w}(s) = 1$ and $\alpha_\mathrm{p}(s) = \alpha_\mathrm{n}(s) = 1$ and frequency independent.

The CBTA realization of the MSO constitutes of two sub-circuits, i.e. lossy integrator and inverting amplifier shown in Fig. 2.7. The voltage gains of the circuits in Figs. 2.7(a) and 2.7(b) can be found respectively as:

$$\frac{V_{\mathrm{o}i}}{V_{\mathrm{o}i-1}} = \frac{\frac{\mu_\mathrm{w} g_{\mathrm{m}i}}{C_i}}{s + \frac{\mu_\mathrm{w} g_{\mathrm{m}i}}{C_i}} = \frac{1}{1 + s\frac{C_i}{\mu_\mathrm{w} g_{\mathrm{m}i}}}, \tag{2.40}$$

and

$$\frac{V_\mathrm{o}}{V_\mathrm{i}} = -\mu_\mathrm{w} g_\mathrm{mf} R_\mathrm{f} = -K, \tag{2.41}$$

where g_mf is the transconductance of the CBTA used in the inverting amplifier of Fig. 2.7(b). Moreover, from Eq. (2.41) $K = \mu_\mathrm{w} g_\mathrm{mf} R_\mathrm{f}$ is the gain (in magnitude) of the VM inverting amplifier shown in Fig. 2.7(b).

The general realization of arbitrary n-phase sinusoidal oscillator can be easily realized by interconnecting the above CBTA-based sub-circuits as shown in Fig. 2.8(a). The resulting VM circuit is shown in 2.8(b) and its closed loop gain can be expressed as:

$$L(s) = -\mu_\mathrm{w} g_\mathrm{mf} R_\mathrm{f} \left[\frac{1}{1 + s\frac{C_i}{\mu_\mathrm{w} g_{\mathrm{m}i}}}\right]^n = -K \left[\frac{1}{1 + s\frac{C_i}{\mu_\mathrm{w} g_{\mathrm{m}i}}}\right]^n. \tag{2.42}$$

For oscillation to sustain, the Barkhausen criteria must be fulfilled, that is:

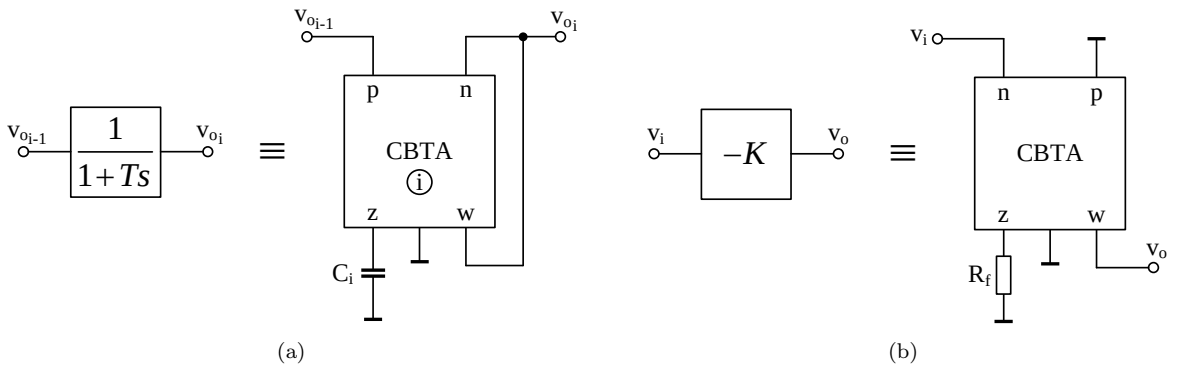
$$-K \left[\frac{1}{1 + s\frac{C_i}{\mu_\mathrm{w} g_{\mathrm{m}i}}}\right]^n = 1. \tag{2.43}$$

Therefore, the oscillation condition and the oscillation frequency are found from Eq. (2.43) as:

$$\mathrm{CO}: \quad K = \left(1 + \frac{\omega_\mathrm{o}^2 C_i^2}{\mu_\mathrm{w}^2 g_{\mathrm{m}i}^2}\right)^{n/2}, \tag{2.44}$$

$$\mathrm{FO}: \quad \omega_0 = \frac{\mu_\mathrm{w} g_{\mathrm{m}i}}{C_i} \tan\left(\frac{\pi}{n}\right). \tag{2.45}$$

Substituting ω_0 of Eq. (2.45) into (2.44) gives:



(a) (b)

Fig. 2.7: Sub-circuits and their realization using CBTA: (a) VM lossy integrator, (b) VM inverting amplifier

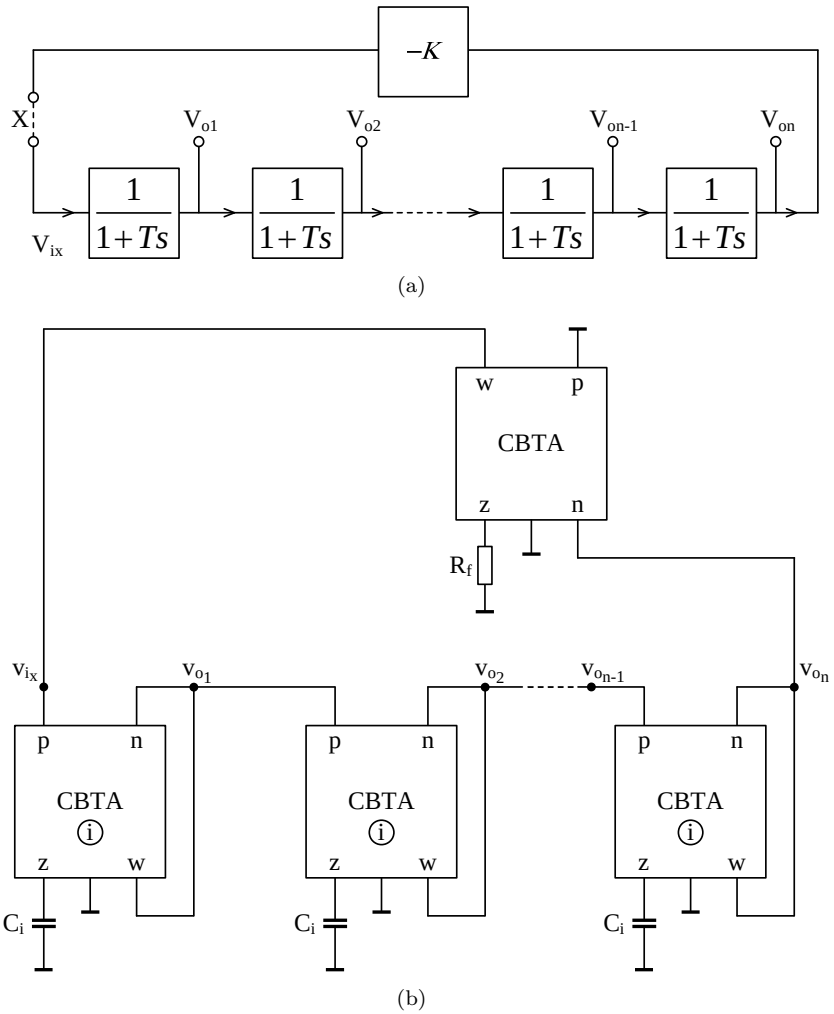


Fig. 2.8: (a) Generalized block diagram of the proposed n-phase sinusoidal oscillator, (b) proposed voltage-mode CBTA-based MSO

$$\text{CO}: \quad K = \left[1 + \tan^2\left(\frac{\pi}{n}\right)\right]^{n/2}. \tag{2.46}$$

Further, from Eq. (2.45) and (2.46) it can be seen that the oscillation frequency can be independently controlled through equal valued $g_{\text{m}i}$ parameters which are electronically adjustable by changing the bias currents of the CBTAs.

The output impedance of the proposed structure can be found as:

$$Z_{\text{o}_i} = Z_{\text{n}_i} \| Z_{\text{p}_{i+1}} \| Z_{\text{w}_i}. \tag{2.47}$$

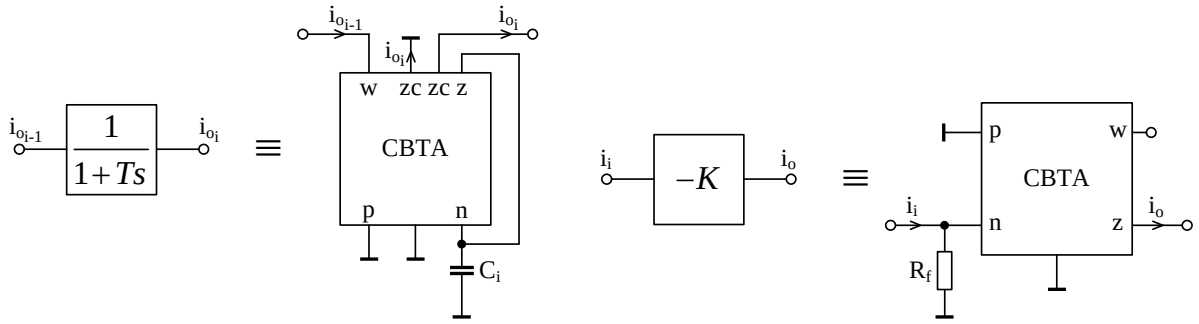
In ideal case $Z_{\text{w}_i} = 0$, thus $Z_{\text{o}_i} = 0$.

The second proposed CBTA-based MSO circuit which operates in current-mode can be obtained using two sub-circuits shown in Fig. 2.9. The current gains of the circuits in Figs. 2.9(a) and 2.9(b) can be found respectively as follows:

$$\frac{I_{\text{o}_i}}{I_{\text{o}_{i-1}}} = \frac{\frac{\alpha_{\text{n}} g_{\text{m}i}}{C_i}}{s + \frac{g_{\text{m}i}}{C_i}} = \frac{\alpha_{\text{n}}}{1 + s\frac{C_i}{g_{\text{m}i}}}, \tag{2.48}$$

and

$$\frac{I_{\text{o}}}{I_{\text{i}}} = -g_{\text{mf}} R_{\text{f}} = -K, \tag{2.49}$$



(a) (b)

Fig. 2.9: Sub-circuits and their realization using CBTA: (a) CM lossy integrator, (b) CM inverting amplifier

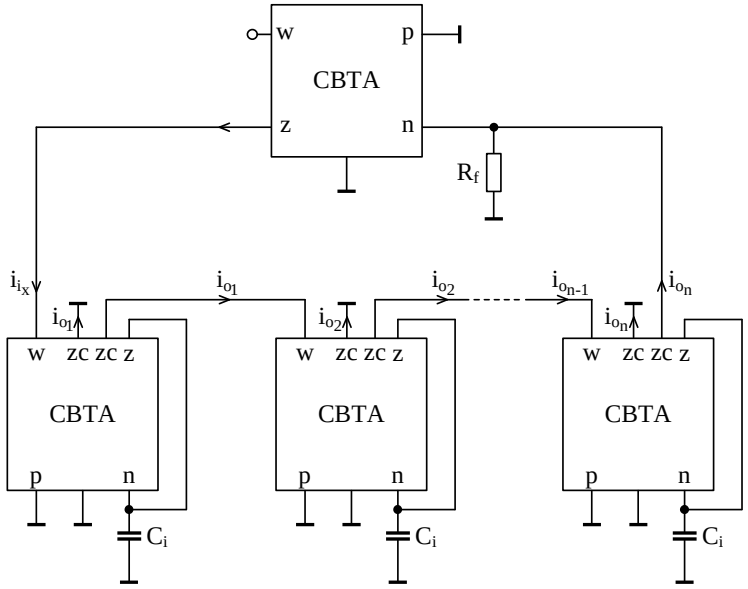


Fig. 2.10: Proposed current-mode CBTA-based MSO

where $g_{\rm mf}$ is the transconductance of the CBTA used in the inverting amplifier of Fig. 2.9(b). From Eq. (2.49) $K = g_{\rm mf}R_{\rm f}$ which is the gain of the CM inverting amplifier shown in Fig. 2.9(b).

The general realization of arbitrary n-phase sinusoidal oscillator can be easily realized by interconnecting the above CBTA-based sub-circuits in accordance to the block diagram of Fig. 2.6. The resulting circuits are shown in Fig. 2.10. The closed loop gains of the circuits in Fig. 2.10 can be expressed as:

$$L(s) = -g_{\rm mf}R_{\rm f}\left[\frac{\alpha_{\rm n}}{1+s\frac{C_i}{g_{{\rm m}i}}}\right]^n = -K\left[\frac{\alpha_{\rm n}}{1+s\frac{C_i}{g_{{\rm m}i}}}\right]^n. \tag{2.50}$$

For oscillation to sustain, the Barkhausen criteria must be fulfilled, that is:

$$-K\left[\frac{\alpha_{\rm n}}{1+s\frac{C_i}{g_{{\rm m}i}}}\right]^n = 1. \tag{2.51}$$

Therefore, the oscillation condition and the oscillation frequency are found from Eq. (2.51) as:

$$\text{CO}: \quad K = \alpha_{\rm n}^{-n}\left(1+\frac{\omega_{\rm o}^2C_i^2}{g_{{\rm m}i}^2}\right)^{n/2}, \tag{2.52}$$

$$\text{FO}: \quad \omega_0 = \frac{g_{{\rm m}i}}{C_i}\tan\left(\frac{\pi}{n}\right). \tag{2.53}$$

Substituting ω_0 of Eq. (2.53) into (2.52) gives CO:

$$\text{CO}: \quad K = \alpha_{\text{n}}^{-n}\left[1+\tan^2\left(\frac{\pi}{n}\right)\right]^{n/2}. \tag{2.54}$$

Again from Eq. (2.53) and (2.54) it can be realized that the oscillation frequency can be independently controlled through equal valued $g_{\text{m}i}$ parameters which are electronically adjustable by changing the bias currents of the CBTAs.

The output impedance of the proposed structure can be found as:

$$Z_{\text{o}_i} = R_{\text{z}_i} \parallel (1/sC_{\text{z}_i}) \, , \ldots i = 1, 2, \ldots, n \tag{2.55}$$

where R_{z} and C_{z} are the z-terminal resistances and capacitance of the CBTAs. In ideal case $Z_{\text{o}_i} = \infty$.

Simulation Results

The MSO circuit for $n = 3$ is designed with the passive component values $C_1 = C_2 = C_3 = 10$ pF and $R_{\text{f}} = 16$ kΩ, all bias currents of the CBTAs are chosen as 50 μA ($g_{\text{m}} = 0.5$ mS). Figure 2.11 shows the current outputs of each stage in the MSO. In this case ($n = 3$) with all the above parameters, the oscillation frequency is obtained as 10.8 MHz from the simulation while the theoretical value is 13.77 MHz. The difference between theoretical and simulated values can be attributed to the parasitic effects of the CBTAs. The phase differences among the outputs for $n = 3$ is in the vicinity of 120 degree. The THD values for $i_{\text{o}1}$, $i_{\text{o}2}$, $i_{\text{o}3}$ voltage outputs are 5.57%, 1.93%, and 0.98%, respectively. The FFT spectrum of the each current output signals for $n = 3$ are shown in Fig. 2.12. As seen from Figs. 2.11 and 2.12, the oscillations are observed to be stable and the simulation results confirm the workability of the proposed current-mode oscillator circuit.

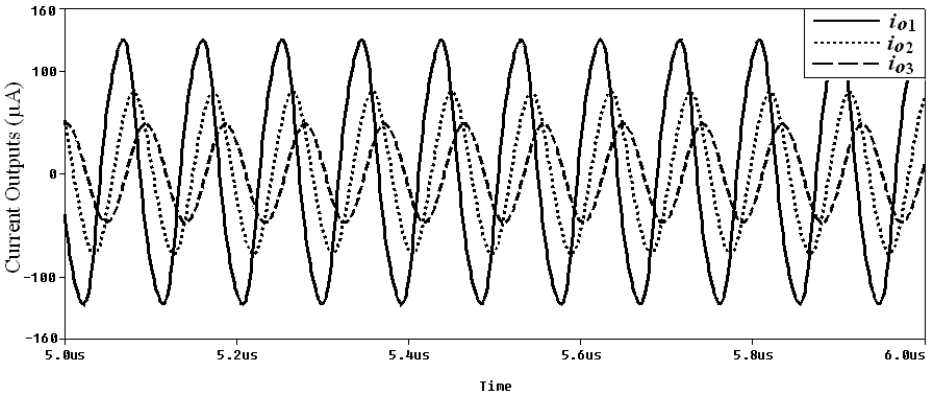


Fig. 2.11: Current outputs of the proposed CM MSO for $n = 3$

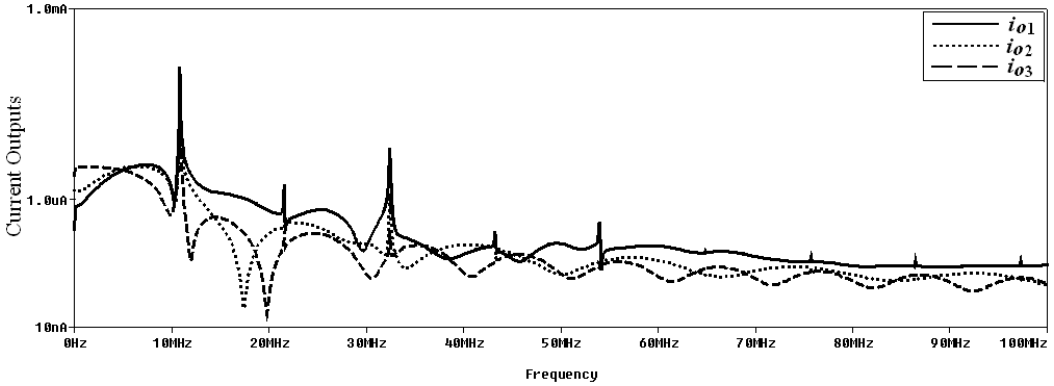


Fig. 2.12: FFT spectrum of the sinusoidal current outputs

2.3 Second-Order Filter Topologies

Probably, the most discussed and most popular analog filters in the literature are the second-order filters that are also called as biquads. One of the advantage of these circuits is that a general filter of a higher-order can be designed by cascading a number of second-order ones. Based on circuit topologies and complexity the biquads can be divided into several categories. Nowadays the highest attention is paid to such second-order filter structures that can provide at least the basic three standard filter functions, i.e. low-, band-, high-pass or additionally also band-stop and all-pass filter responses without changing the circuit topology. These filtering structures are called multifunction or universal filters, respectively. Similarly, considering the number of inputs and outputs in topologies then biquads can be categorized to so-called multi-input single-output (MISO) or single-input multi-output (SIMO). From simplicity point of view the universal CM MISO proposed in [27] worth to be mentioned. Although it is of minimal configuration, additional current followers are required for their cascading. This disadvantage is overcame in [28], however, for the cost of biquad complexity. Particularly, the SIMO type biquads are more attractive, because they are able to realize several responses simultaneously with the same topology and without changing its configuration. This kind of filter, which finds wide applications in phase-locked loop FM stereo demodulation, touch-tone telephone tone decoding etc., is advantages in consideration of versatility, simplicity, and cost reduction. Advantages of 'voltage differencing' feature of the voltage differencing current conveyor (VDCC) have been demonstrated in [29]. In addition, the two improved SIMOs in [30] simultaneously realize all five standard filter functions and Q and f_0 can be controlled orthogonally, i.e. f_0 can be adjusted arbitrarily and at the same time Q can be set to any value through passive resistor without disturbing f_0. Unfortunately, the complexity of circuit topologies has increased. Recently, special tunable (reconfigurable) biquad design technique has been introduced, namely frequency-agile filters (FAFs) that have the property of agility, i.e. in order to not disturb the signal processing during the transmission of the signal, the hop between two consecutive frequencies f_1 and f_2 must be able to be carried out very quickly [31]. On the other hand, filters with good frequency selectivity have to be of the order higher than two. In work [32], two active only grounded-C equivalents of third-order VM elliptic low-pass (LP) LC ladder prototype active equivalents are proposed and the real behavior of the optimized active only grounded-C third-order VM elliptic LP filter experimentally verified.

2.3.1 Universal Filter with Minimal Configuration

From simplicity point of view as VM counterpart of the universal MISO proposed in [27] the VM MISO employing voltage differencing inverting buffered amplifier (VDIBA) can be considered [26]. The VDIBA is a recently introduced four-terminal active device [2]. It has a pair of high-impedance voltage inputs $v+$ and $v-$, a high-impedance current output z, and low-impedance voltage output $w-$. The input stage of VDIBA can be easily implemented by a differential-input single-output operational transconductance amplifier (OTA), which converts the input voltage to output current that flows out of the z terminal. The output stage can be formed by unity-gain inverting voltage buffer (IVB). Since both stages can be implemented by commercially available ICs, and moreover it contains OTA whose g_m can be electronically controllable via DC bias current, the introduced active element is attractive for resistorless and electronically controllable circuit applications.

Using standard notation, the relationship between port currents and voltages of the VDIBA can be described by following hybrid matrix:

$$\begin{bmatrix} I_{\mathrm{v}+} \\ I_{\mathrm{v}-} \\ I_{\mathrm{z}} \\ V_{\mathrm{w}-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_\mathrm{m} & -g_\mathrm{m} & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_{\mathrm{v}+} \\ V_{\mathrm{v}-} \\ V_{\mathrm{z}} \\ I_{\mathrm{w}-} \end{bmatrix}, \tag{2.56}$$

where g_m represents the transconductance of VDIBA.

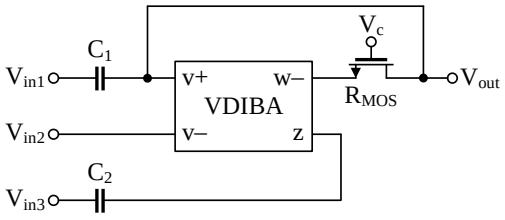


Fig. 2.13: Proposed VM universal filter

The proposed VM MISO universal filter is shown in Fig. 2.13 [26]. The circuit employs single VDIBA as active element, two capacitors, and one nMOS transistor working as voltage-controlled resistor (VCR). Although in practice, filters employing only grounded capacitors are preferred, new IC technologies offer floating capacitor realization possibility as a double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor [47]. The nMOS transistor works in triode region and its resistance R_{MOS} for low value of signal amplitudes can be calculated as follows:

$$R_{\mathrm{MOS}} \cong \frac{1}{\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{c}} - V_{\mathrm{THn}})}, \tag{2.57}$$

where C_{ox} is the gate oxide capacitance per unit area, μ_{n} is the free electron mobility in the channel, W and L are the channel width and length of the nMOS, V_{THn} is the threshold voltage of the transistor, and V_{c} is DC control voltage used for tuning. Using (2.56), circuit analysis yields the following output voltage V_{out} of the proposed circuit in Fig. 2.13:

$$V_{\mathrm{out}} = \frac{s^2 C_1 C_2 R_{\mathrm{MOS}} V_{\mathrm{in1}} - s C_2 V_{\mathrm{in3}} + g_{\mathrm{m}} V_{\mathrm{in2}}}{s^2 C_1 C_2 R_{\mathrm{MOS}} + s C_2 + g_{\mathrm{m}}}. \tag{2.58}$$

From Eq. (2.58) it can be observed that the proper connection of the relevant input terminals yields the five standard types of biquadratic filter functions as follows:

(i) If $V_{\mathrm{in1}} = V_{\mathrm{in3}} = 0$ (grounded), a second-order LP filter can be obtained with $V_{\mathrm{out}}/V_{\mathrm{in2}}$;
(ii) If $V_{\mathrm{in1}} = V_{\mathrm{in2}} = 0$ (grounded), a second-order inverting BP filter can be obtained with $V_{\mathrm{out}}/V_{\mathrm{in3}}$;
(iii) If $V_{\mathrm{in2}} = V_{\mathrm{in3}} = 0$ (grounded), a second-order HP filter can be obtained with $V_{\mathrm{out}}/V_{\mathrm{in1}}$;
(iv) If $V_{\mathrm{in3}} = 0$ (grounded) and $V_{\mathrm{in1}} = V_{\mathrm{in2}} = V_{\mathrm{in}}$, a second-order BR filter can be obtained with $V_{\mathrm{out}}/V_{\mathrm{in}}$;
(v) If $V_{\mathrm{in1}} = V_{\mathrm{in2}} = V_{\mathrm{in3}} = V_{\mathrm{in}}$, a second-order AP filter can be obtained with $V_{\mathrm{out}}/V_{\mathrm{in}}$.

Thus, the circuit is capable of realizing LP, BP, HP, BR, and AP responses from the same topology without any requirement for component-matching conditions or use of additional inverting voltage inputs. For all filter responses the resonance angular frequency ω_0, quality factor Q, and bandwidth ω_0/Q derived from the denominator of Eq. (2.58) are:

$$\omega_0 = \sqrt{\frac{g_{\mathrm{m}}}{C_1 C_2 R_{\mathrm{MOS}}}}, \tag{2.59}$$

$$Q = \sqrt{\frac{C_1 g_{\mathrm{m}} R_{\mathrm{MOS}}}{C_2}}, \tag{2.60}$$

$$\frac{\omega_0}{Q} = \frac{1}{C_1 R_{\mathrm{MOS}}}. \tag{2.61}$$

It should be noted that the gain factors for all five filter responses are equal to unity in magnitude.

A sensitivity study forms an important index of the performance of any active network. The active and passive relative sensitivities of the proposed circuit derived from (2.59)–(2.61) are given as:

$$S_{g_{\mathrm{m}}}^{\omega_0} = -S_{C_1, C_2, R_{\mathrm{MOS}}}^{\omega_0} = \frac{1}{2}, \quad S_{C_1, g_{\mathrm{m}}, R_{\mathrm{MOS}}}^{Q} = -S_{C_2}^{Q} = \frac{1}{2},$$

$$S_{C_1,R_{\rm MOS}}^{\omega_0/Q} = -1. \tag{2.62}$$

From the results it is evident that the sensitivities are low and not larger than unity in absolute value.

Stability Analysis

Considering the non-idealities of the VDIBA, the matrix relationship of Eq. (2.56) converts to:

$$\begin{bmatrix} I_{\rm v+} \\ I_{\rm v-} \\ I_{\rm z} \\ V_{\rm w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{\rm m}(s) & -g_{\rm m}(s) & sC_{\rm z}+1/R_{\rm z} & 0 \\ 0 & 0 & -\beta(s) & R_{\rm w-} \end{bmatrix} \begin{bmatrix} V_{\rm v+} \\ V_{\rm v-} \\ V_{\rm z} \\ I_{\rm w-} \end{bmatrix}, \tag{2.63}$$

where the parasitic impedance $R_{\rm z}$ is ideally infinity as well as $C_{\rm z}$ and $R_{\rm w-}$ are ideally equal to zero and the β and $g_{\rm m}$ are non-ideal voltage and transconductance error gains of VDIBA, respectively.

Considering the effects of these non-ideal gains on the proposed filter, the output voltage $V_{\rm out}$ in Eq. (2.58) turns to:

$$V_{\rm out} \cong \frac{s^2C_1C_2R_{\rm MOS}V_{\rm in1} - \beta sC_2V_{\rm in3} + \beta g_{\rm m}V_{\rm in2}}{s^2C_1C_2R_{\rm MOS} + sC_2 + \beta g_{\rm m}}. \tag{2.64}$$

It should be mentioned that non-ideal gains β and $g_{\rm m}$ are frequency-dependent parameters that using a single-pole model [48] can be defined as follows:

$$\beta(s) = \frac{\beta_{\rm o}}{1+s\tau_\beta}, \tag{2.65}$$

$$g_{\rm m}(s) = \frac{g_{\rm mo}}{1+s\tau_{g_{\rm m}}}, \tag{2.66}$$

where $\beta_{\rm o} = 1-\varepsilon_{\beta_{\rm v}}$ and $g_{\rm mo} = g_{\rm o}(1-\varepsilon_{g_{\rm m}})$ are DC voltage and transconductance gains of VDIBA, respectively.

The best way to test the stability of the proposed filter characteristics is the use of Routh–Hurwitz stability criterion [49]. Thus, assuming that the single-pole model analysis gives satisfactory result and neglecting the effect of τ_β, by replacing Eq. (2.66) into (2.64) its denominator turns into the following third-order polynomial:

$$D(s) = \sum_{i=0}^{3}(a_i s^i). \tag{2.67}$$

Here, the coefficients of a_i $(i = 0, 1, 2, 3)$ are calculated as:

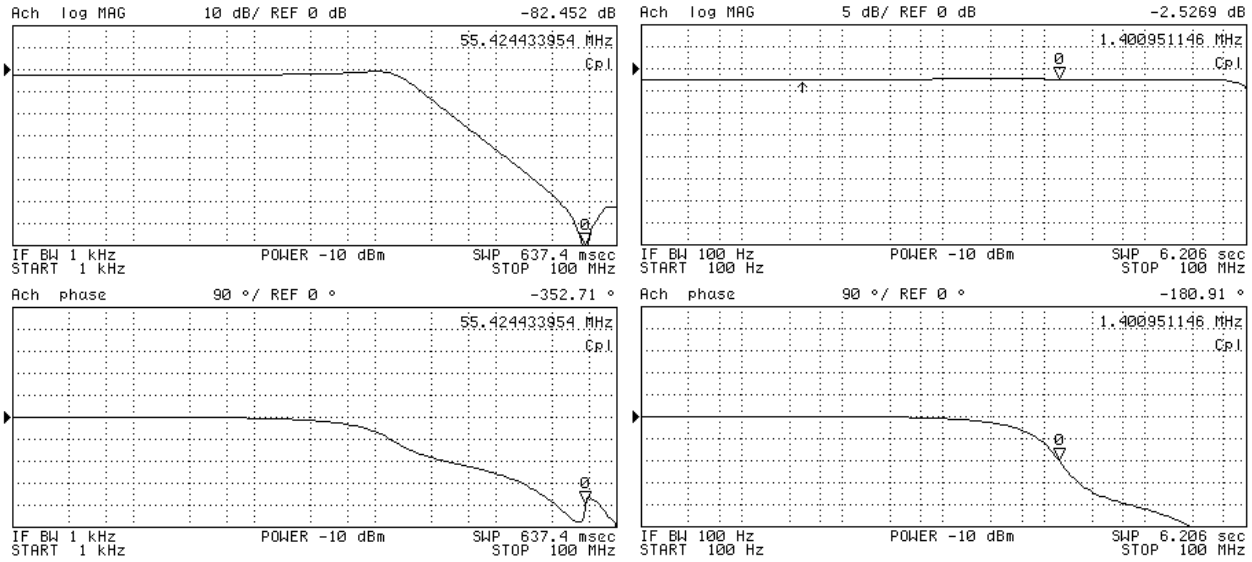
$$\begin{aligned} a_0 &= \beta_{\rm o}g_{\rm mo}, \\ a_1 &= C_2, \\ a_2 &= C_2(C_1R_{\rm MOS} + \tau_{g_{\rm m}}), \\ a_3 &= C_1C_2R_{\rm MOS}\tau_{g_{\rm m}}. \end{aligned} \tag{2.68}$$

Thus, in order to prevent stability problems, the following condition should be satisfied:

$$\tau_{g_{\rm m}} < \frac{C_1C_2R_{\rm MOS}}{\beta_{\rm o}C_1g_{\rm mo}R_{\rm MOS} - C_2}. \tag{2.69}$$

Experimental Verification

The proposed filter has been developed on printed circuit board (PCB) and its behavior has been verified by experimental measurements using network-spectrum analyzer Agilent 4395A. To realize the input stage of VDIBA the readily available IC OPA660 by BURR BROWN [50] was used, which contains the so-called



(a) (b)

Fig. 2.14: Measured magnitude and phase responses of (a) low-pass, (b) all-pass filters

'diamond' transistor (DT) and fast voltage buffer (VB). The resistor R_{ADJ} was chosen as 220 Ω [50]. In order to increase the linearity of collector current versus input voltage V_{d}, the DT is complemented with degeneration resistor $R_{\mathrm{G}} \gg 1/g_{\mathrm{mT}}$, added in series to the emitter, where the g_{mT} is the DT transconductance. Then the total transconductance decreases to the approximate value $1/R_{\mathrm{G}}$ [50]. The output stage IVB was realized by IC AD830 produced by Analog Devices [51]. The DC power supply voltages of both ICs were equal to ±5 V. In all measurements the values of the passive components were selected as $C_1 = C_2 = 100$ pF and $R_{\mathrm{G}} = R_{\mathrm{MOS}} = 1$ kΩ to obtain the designed MISO filter responses with $Q = 1$ at pole frequency $f_0 = \omega_0/2\pi \cong 1.59$ MHz. Measured results of low-pass and all-pass magnitude and phase responses are shown in Fig. 2.14. From the results it can be observed that due to extra parasitic capacitances of the fabricated PCB the resonance frequency is $f_0 \cong 1.48$ MHz, which, however, is close to the theoretical one.

2.4 Passive Component Emulators: Acitve Resistor, Inductance Simulators, FDNR, Capacitance Multiplier Design

The last part of the thesis deals with emulation of passive components in active form such as grounded voltage controlled positive resistor (GVCPR), lossy/lossless floating/grounded inductance simulators using various ABBs, or novel floating frequency dependent negative resistor (FDNR), and floating capacitance multipliers design [33]–[38]. Electronically tunable resistors are widely used in analog signal processing such as in active RC filters with variable f_0, controlled oscillators, variable gain amplifiers, voltage or current dividers, and voltage or current to frequency converters, etc. In [33], the proposed new CMOS-based GVCPR with one control voltage employs only five CMOS transistors. Note that in the structure one of transistors operates in triode region while others in saturation region or OFF. One of the main properties of the novel GVCPR is its ultra low power consumption and its superior performance was also proved by numeric Figure of Merit calculation. An inductor is also a required element in circuit design. Conventional spiral inductors directly made on chip occupy significant chip area and therefore are too costly and suffer from substrate resistive losses and capacitive couplings. In addition, process tolerances lead to component variations, which cannot easily be tuned in the passive case. Therefore, in recent years, synthetic inductor realizations have been focused on the field of the integrated circuit (IC) design due to the resulting reduction in size and cost effectiveness [34]–[37].

2.4.1 Novel Floating General Element Simulator

In [38], a general floating immittance function simulator realizing frequency dependent negative resistor (FDNR), inductor, capacitance multiplier, and resistor was proposed. It is composed of two CBTAs and three passive components that are all grounded. The circuit does not require any component matching conditions and it has good sensitivity performance with respect to tracking errors. Moreover, the proposed FDNR, inductance, capacitor and resistor simulator can be tuned electronically by changing the biasing current of the CBTA or can be controlled through the grounded resistor or capacitor.

Consider floating admittance in Fig. 2.15(a) and simulator circuit in Fig. 2.15(b), the short circuit admittance matrices of these circuits can be respectively written as:

$$[y_{ij}] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = Y_{\rm f} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.70}$$

$$[y_{ij}] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \frac{\alpha_1 \mu_{\rm w1}}{\alpha_2 \mu_{\rm w2}} \frac{g_{\rm m1} Y_1 Y_3}{g_{\rm m2} Y_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.71}$$

where $\alpha_{\rm p} \approx \alpha_{\rm n} = \alpha$ and $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{ij} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$.

From (2.70) and (2.71) it is seen that depending on the choice of passive component a floating FDNR, inductor, capacitor and resistor simulator can be realized as follows:

(i) If $Y_1 = sC_1$, $Y_2 = G_2$, and $Y_3 = sC_3$ are selected, a floating FDNR is implemented as follows:

$$[Y_{\rm D}] = \frac{\alpha_1 \mu_{\rm w1}}{\alpha_2 \mu_{\rm w2}} \frac{s^2 g_{\rm m1} C_1 C_3}{g_{\rm m2} G_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.72}$$

which represents a floating FDNR whose parameter is given by $D_{\rm f} = \frac{\alpha_1 \mu_{\rm w1}}{\alpha_2 \mu_{\rm w2}} \frac{g_{\rm m1} C_1 C_3}{g_{\rm m2} G_2}$. In ideal conditions, $D_{\rm f} = \frac{g_{\rm m1} C_1 C_3}{g_{\rm m2} G_2}$. Hence, the proposed circuit of Fig. 2.15(b) behaves as an ideal floating FDNR. By setting either $V_2 = 0$ or $V_1 = 0$, the proposed circuit can also be used as a grounded FDNR. Note that $D_{\rm f}$ can be tuned through $g_{\rm m1}$, $g_{\rm m2}$, G_2, C_1, or C_3.

(ii) If the admittances are chosen as $Y_1 = G_1$, $Y_2 = sC_2$, and $Y_3 = G_3$, the input admittance becomes:

$$[Y_{\rm L}] = \frac{\alpha_1 \mu_{\rm w1}}{\alpha_2 \mu_{\rm w2}} \frac{g_{\rm m1} G_1 G_3}{s g_{\rm m2} C_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.73}$$

which represents a floating inductor whose inductance is given by $L_{\rm f} = \frac{\alpha_2 \mu_{\rm w2}}{\alpha_1 \mu_{\rm w1}} \frac{g_{\rm m2} C_2}{g_{\rm m1} G_1 G_3}$. In ideal conditions $L_{\rm f} = \frac{g_{\rm m2} C_2}{g_{\rm m1} G_1 G_3}$. By setting either $V_2 = 0$ or $V_1 = 0$, the proposed circuit can also be used as a grounded inductor.

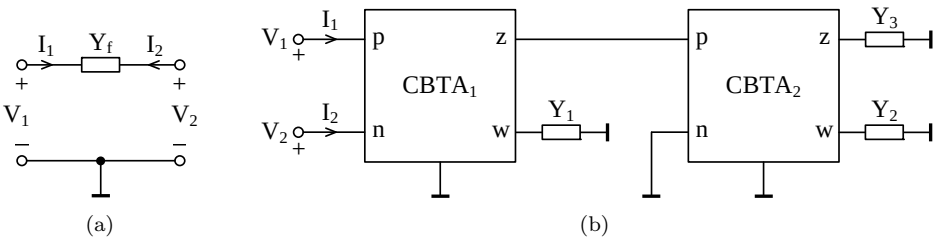


Fig. 2.15: (a) Floating admittance and (b) floating admittance simulator circuit

(iii) If $Y_1 = sC_1$, $Y_2 = G_2$, and $Y_3 = G_3$ are chosen for the circuit depicted in Fig. 2.15(b), the short circuit admittance matrix of the floating capacitor is found to be:

$$[Y_{\rm C}] = \frac{\alpha_1\mu_{\rm w1}}{\alpha_2\mu_{\rm w2}}\frac{sg_{\rm m1}C_1G_3}{g_{\rm m2}G_2}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.74}$$

where, $C_{\rm f} = \frac{\alpha_1\mu_{\rm w1}}{\alpha_2\mu_{\rm w2}}\frac{g_{\rm m1}C_1G_3}{g_{\rm m2}G_2}$. In ideal conditions, $C_{\rm f} = \frac{g_{\rm m1}C_1G_3}{g_{\rm m2}G_2}$. When the resistors and capacitor in Y_1 and Y_3 admittances are interchanged, we also obtain:

$$[Y_{\rm C}] = \frac{\alpha_1\mu_{\rm w1}}{\alpha_2\mu_{\rm w2}}\frac{sg_{\rm m1}G_1C_3}{g_{\rm m2}G_2}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.75}$$

which represents a floating capacitor whose parameter is given by $C_{\rm f} = \frac{\alpha_1\mu_{\rm w1}}{\alpha_2\mu_{\rm w2}}\frac{g_{\rm m1}G_1C_3}{g_{\rm m2}G_2}$. In ideal conditions, $C_{\rm f} = \frac{g_{\rm m1}G_1C_3}{g_{\rm m2}G_2}$.

The value of grounded capacitor C_3 can be multiplied by a constant which can be tuned electronically by changing transconductance values of the CBTAs or can be controlled through grounded resistors. Hence, the proposed circuit can be used as a floating capacitance multiplier. Moreover, the proposed circuit can be used to convert a grounded capacitor to floating one.

(iv) Finally, choosing $Y_1 = G_1$, $Y_2 = G_2$, and $Y_3 = G_3$ for the circuit depicted in Fig. 2.15(b) is described by the following short circuit admittance matrix:

$$[Y_{\rm R}] = \frac{\alpha_1\mu_{\rm w1}}{\alpha_2\mu_{\rm w2}}\frac{g_{\rm m1}G_1G_3}{g_{\rm m2}G_2}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.76}$$

which represents a floating resistor whose resistance is given by $R_{\rm f} = \frac{\alpha_2\mu_{\rm w2}}{\alpha_1\mu_{\rm w1}}\frac{g_{\rm m2}G_2}{g_{\rm m1}G_1G_3}$. In ideal conditions, $R_{\rm f} = \frac{g_{\rm m2}G_2}{g_{\rm m1}G_1G_3}$.

Normalized active and passive sensitivities of the $D_{\rm f}$, $L_{\rm f}$, $C_{\rm f}$, and $R_{\rm f}$ are given by:

$$S^{y_{ij}}_{Y_1,Y_3,\alpha_1,\mu_{\rm w1},g_{\rm m1}} = -S^{y_{ij}}_{Y_2,\alpha_2,\mu_{\rm w2},g_{\rm m2}} = 1. \tag{2.77}$$

which are not higher than unity in magnitude. Thus, the proposed simulators offer low active and passive sensitivities.

2.4.2 High-Order Floating Frequency Dependent Element Simulator

In order to realize high-order floating frequency dependent element simulator circuit, the circuit given in Fig. 2.16, which was presented in [52] is used. Its short circuit admittance matrix can be written as:

$$\begin{bmatrix} y_{ij} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{11} & y_{12} \end{bmatrix} = \alpha_1\mu_{\rm w1}\frac{g_{\rm m1}Y_1}{Y_2}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{2.78}$$

where $\alpha_{\rm p} \approx \alpha_{\rm n} = \alpha$ and $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{ij} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$.

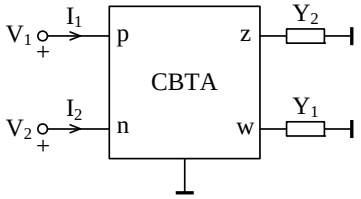


Fig. 2.16: The proposed circuit given in [52].

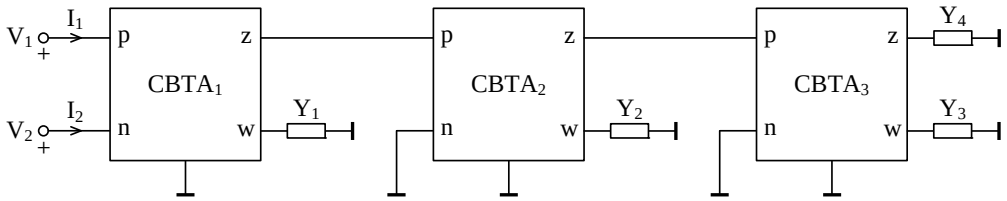


Fig. 2.17: Third-stage frequency dependent element

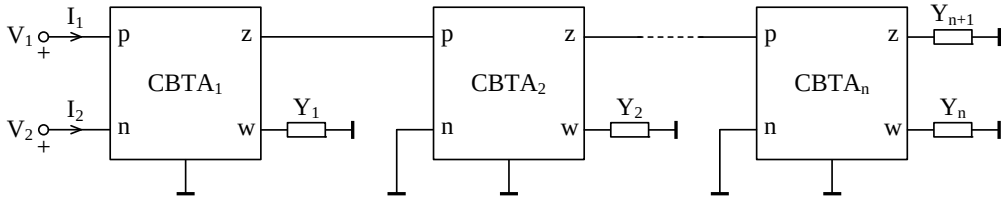


Fig. 2.18: High-order frequency dependent element

The circuit in Fig. 2.15(a) can be used to replace Y_2 in Fig. 2.16, which will result in a cascade configuration given in Fig. 2.17, leading to a third-stage frequency dependent element simulator circuit described by the short circuit admittance matrice:

$$\left[\ y_{ij}\ \right] = \left[\begin{array}{cc} y_{11} & y_{12} \\ y_{11} & y_{12} \end{array}\right] = \frac{\alpha_1\alpha_3\mu_{\mathrm{w1}}\mu_{\mathrm{w3}}}{\alpha_2\mu_{\mathrm{w2}}}\frac{g_{\mathrm{m1}}g_{\mathrm{m3}}Y_1Y_3}{g_{\mathrm{m2}}Y_2Y_4}\left[\begin{array}{cc} +1 & -1 \\ -1 & +1 \end{array}\right]. \tag{2.79}$$

The general high-order frequency dependent element simulator circuit is given in Fig. 2.18 and its generalized non-ideal short circuit admittance matrices can be written as follows [38]:

(a) If n is even:

$$\left[\ y_{ij}\ \right] = \frac{(\alpha_1\alpha_3\ldots\alpha_{n+1})(\mu_{\mathrm{w1}}\mu_{\mathrm{w3}}\ldots\mu_{\mathrm{w}(n+1)})}{(\alpha_2\alpha_4\ldots\alpha_{\mathrm{n}})(\mu_{\mathrm{w2}}\ldots\mu_{\mathrm{wn}})}\frac{(g_{\mathrm{m1}}g_{\mathrm{m3}}\ldots g_{\mathrm{m}(n+1)})(Y_1Y_3\ldots Y_{n+1})}{(g_{\mathrm{m2}}g_{\mathrm{m4}}\ldots g_{\mathrm{mn}})(Y_2Y_4\ldots Y_n)}\left[\begin{array}{cc} +1 & -1 \\ -1 & +1 \end{array}\right], \tag{2.80}$$

in ideal conditions:

$$\left[\ y_{ij}\ \right] = \frac{(g_{\mathrm{m1}}g_{\mathrm{m3}}\ldots g_{\mathrm{m}(n+1)})(Y_1Y_3\ldots Y_{n+1})}{(g_{\mathrm{m2}}g_{\mathrm{m4}}\ldots g_{\mathrm{mn}})(Y_2Y_4\ldots Y_n)}\left[\begin{array}{cc} +1 & -1 \\ -1 & +1 \end{array}\right]. \tag{2.81}$$

(b) If n is odd:

$$\left[\ y_{ij}\ \right] = \frac{(\alpha_1\alpha_3\ldots\alpha_n)(\mu_{\mathrm{w1}}\mu_{\mathrm{w3}}\ldots\mu_{\mathrm{wn}})}{(\alpha_2\alpha_4\ldots\alpha_{n-1})(\mu_{\mathrm{w2}}\ldots\mu_{\mathrm{w}(n-1)})}\frac{(g_{\mathrm{m1}}g_{\mathrm{m3}}\ldots g_{\mathrm{mn}})(Y_1Y_3\ldots Y_n)}{(g_{\mathrm{m2}}g_{\mathrm{m4}}\ldots g_{\mathrm{m}(n-1)})(Y_2Y_4\ldots Y_{n-1})}\left[\begin{array}{cc} +1 & -1 \\ -1 & +1 \end{array}\right], \tag{2.82}$$

in ideal conditions:

$$\left[\ y_{ij}\ \right] = \frac{(g_{\mathrm{m1}}g_{\mathrm{m3}}\ldots g_{\mathrm{mn}})(Y_1Y_3\ldots Y_n)}{(g_{\mathrm{m2}}g_{\mathrm{m4}}\ldots g_{\mathrm{m}(n-1)})(Y_2Y_4\ldots Y_{n-1})}\left[\begin{array}{cc} +1 & -1 \\ -1 & +1 \end{array}\right]. \tag{2.83}$$

From Eqs. (2.80)–(2.82), high-order frequency dependent element can be obtained by choosing admittances Y. For example; for $n = 5$, if the capacitors are chosen as $Y_1 = sC_1$, $Y_3 = sC_3$, $Y_5 = sC_5$ and the resistors are chosen as $Y_2 = G_2$, $Y_4 = G_4$, $Y_6 = G_6$, the short-circuit admittance matrices can be found as follows:

$$\left[\ y_{ij}\ \right] = \frac{s^3(g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m5}})(C_1C_3C_5)}{(g_{\mathrm{m2}}g_{\mathrm{m4}})(G_2G_4G_6)}\left[\begin{array}{cc} +1 & -1 \\ -1 & +1 \end{array}\right], \tag{2.84}$$

giving the third-order floating frequency dependent element simulator circuit. If n is chosen as 6, the 4^{th}-order floating frequency dependent element simulator circuit will be obtained. Hence, the circuit given in Fig. 2.18 realizes high-order floating frequency dependent resistor simulator circuit for n is even and high-order floating frequency dependent capacitor circuit for n is odd defined as $I = s^3EV$, $I = s^4FV$, ..., $I = s^nKV$.

If the resistors are chosen as $Y_1 = G_1$, $Y_3 = G_3$, $Y_5 = G_5$, and the capacitors are chosen as $Y_2 = sC_2$, $Y_4 = sC_4$, $Y_6 = sC_6$ for previous example ($n = 5$) and the short circuit admittance matrices can be found as follows:

$$\left[\ y_{ij}\ \right] = \frac{(g_{\mathrm{m}1}g_{\mathrm{m}3}g_{\mathrm{m}5})(G_1G_3G_5)}{s^3(g_{\mathrm{m}2}g_{\mathrm{m}4})(C_2C_4C_6)} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \tag{2.85}$$

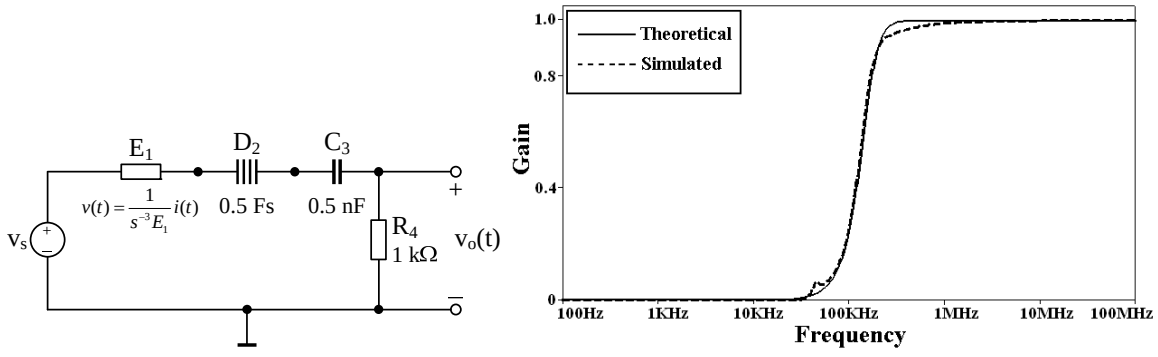
The high-order floating frequency dependent inductor is obtained when n is odd. The high-order floating frequency dependent resistor is obtained when n is even and it is defined as $V = s^3MI$, $V = s^4NI$, ..., $V = s^nZI$.

Simulation Results

The behavior of the proposed high-order frequency dependent element have been confirmed by third-order high-pass filter design shown in Fig. 2.19(a) [38]. In this circuit, the third-order floating element, defined as $V(s) = s^{-3}E_1I(s)$, was used based on the high-order simulator circuit shown in Fig. 2.18. D_2 was obtained using the FDNR circuit shown in Fig. 2.15(b). In Fig. 2.19(a), E_1 was taken as 10^{-21} Fs^2. Therefore, the transfer function of the design example can be found as follows:

$$\frac{V_{\mathrm{o}}(s)}{V_{\mathrm{s}}(s)} = \frac{s^3}{s^3 + 2\cdot 10^6 s^2 + 2\cdot 10^{12}s + 10^{18}}, \tag{2.86}$$

and the gain characteristic of the design example shown in Fig. 2.19(a) is given in Fig. 2.19(b), respectively. Note that according to used active filter synthesis method, proposed nth-order frequency dependent element circuit can be important such as the use of active and passive component count. It is the one of the most important advantages of the proposed nth-order frequency dependent element circuit. On the other hand, nth-order active filter circuit can be realized using less active and passive components with using proposed nth-order frequency dependent element circuit.



(a) (b)

Fig. 2.19: (a) Design example for high-order floating element, (b) gain-frequency characteristics of the theoretical and simulated filter

3 CONCLUSIONS

The habilitation thesis itself is composed of 38 papers having been elaborated by the author in close collaboration with his highly recognized colleagues from abroad since 2011 [1]–[38]. Note that 18 papers are published in reputed SCI-E journals with impact factor and novel ideas were presented in 20 international conference contributions, respectively. The corresponding research results have been acquired in Department of Telecommunications, Faculty of Electrical Engineering and Communication (FEEC), Brno University of Technology (BUT). Moreover, part of the results was used for education purposes and published in textbooks [53], [54]. Both study materials are used in Analogová Technika (FEKT-BANA) and Analog Technology (FEKT-CANA) courses of undergraduate degree programmes of FEEC BUT.

The presented theoretical results were verified by SPICE simulations using CMOS process technology parameters such as TSMC 0.35 μm, TSMC 0.25 μm, TSMC 0.18 μm, IBM 0.13 μm, PTM 90 nm, etc. In some cases, the behavior of the proposed applications was experimentally verified using the readily available UVC-N1C 0520 & UCC-N1B 0520 ICs developed at our department and produced in cooperation with ON Semiconductor Czech Republic, Ltd., via commercially produced chips AD844, OPA660, OPA860, AD830, LT1364, or array transistors CD4007UB. For this research the infrastructure of the SIX Research Center was used i.e. the experimental measurements have been carried out on developed printed circuit boards using network-spectrum-impedance analyzer Agilent 4395A, function generator Agilent 33521A, or four-channel oscilloscope Agilent DSOX2014A.

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CURRICULUM VITAE

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Updated: September 22, 2015

EDUCATION

2006 – 2010:	Ph.D. - Brno University of Technology, Brno, Czech Republic
2000 – 2006:	M.Sc. - Brno University of Technology, Brno, Czech Republic

ACADEMIC POSITIONS

Since 2012:	Research Fellow at the Centre of Sensor, Information and Communication Systems (SIX)
Since 2010:	Assistant Professor - Brno University of Technology, Brno, Czech Republic
2007 – 2010:	Assistant - Brno University of Technology, Brno, Czech Republic

PROFESIONAL ACTIVITIES

Research topics of interest:	Analog electronics, new active elements and their applications, low transistor count circuits, MOS-only circuits, oscillators, inductor simulators, capacitance multipliers, and FDNR design

Teaching:

Since 2013:	Analog Technology – CANA (lectures & PC laboratories)
2013 – 2015:	Communications Theory – MTSD (laboratories)
2007:	Network Architecture – BARS (PC laboratories)
2006 – 2009:	Communications Theory – MTSD (laboratories)
2006:	Construction of Electronic Equipments – BKEZ (PC laboratories)

POSTDOCTORAL / STUDENT INTERNSHIPS, TRAINING AND TEACHING MOBILITIES

09/2015:	Erasmus Staff Training Mobility at Bogazici University, Istanbul, Turkey (1 week)
05/2015:	ISCAS/MCE Conference Organizing Workshop, Lisbon, Portugal
02/2014 – 04/2014:	Postdoctoral Internship – Visiting Researcher at the Department of Electronics and Communications Engineering, Dogus University, Istanbul, Turkey
02/2013 – 05/2013:	Postdoctoral Internship – Visiting Researcher at the BETA Laboratory, Department of Electrical and Electronic Engineering, Bogazici University, Istanbul, Turkey
07/2012:	Erasmus Staff Training Mobility at Bogazici University, Istanbul, Turkey (2 weeks)
05/2011:	Erasmus Teaching Staff Mobility at Namik Kemal University, Corlu, Turkey (1 week)
09/2009 – 02/2010:	LLP Erasmus Exchange Student at the Bogazici University, Istanbul, Turkey

AWARDS

2012:	Rector Award in the University competition "Top 10 Excelence VUT 2011" for the 8$^{\text{th}}$ most productive scientist at the Brno University of Technology, category "Publications"

2011: Rector Award in the University competition "Top 10 Excelence VUT 2010" for the 9th most productive scientist at the Brno University of Technology, category "Publications"

2011: Best paper award in memory of Prof. Dr. Mustafa Bayram - 7th International Conference on Electrical Electronics Engineering - ELECO 2011, Bursa, Turkey

DEVELOPED INTEGRATED CIRCUITS

2012: JEŘÁBEK, J., VRBA, K., KOTON, J., HERENCSÁR, N., KOUDAR, I.: LNVGA – Low Noise Variable Gain Amplifier (LNVGA), in cooperation with ON Semiconductor.

2010: HERENCSÁR, N., VRBA, K., KOUDAR, I.: Universal Voltage Conveyor (UVC.N1C.IK), in cooperation with ON Semiconductor.

PARTICIPATION IN PROJECTS

Projects supported by the Czech Science Foundation (GA CR):

2011 – 2013: GPP102/11/P489: Electronically tuneable first-order allpass filters and their application to quadrature oscillators. Holder: Dr. Herencsár

2009 – 2013: GA102/09/1681: Computer automatation of methods for linear functional block synthesis and research of new active elements. Holder: Prof. K. Vrba

2006 – 2008: GA102/06/1383: Circuits with universal current and voltage conveyors and with current operational amplifiers. Holder: Prof. K. Vrba

Project supported by the European Union:

2010 – 2012: OP VK CZ.1.07/1.3.10/02.0018: Complex educational programme in the field of ICT for the employees of South-Moravian schools. Holder: Assoc. Prof. K. Molnár

Projects supported by the Ministry of Education, Youth and Sports of Czech Republic:

2005 – 2011: MSM21630513: Electronic communication systems and technologies of novel generations (ELKOM). Holders: Prof. Z. Raida, Prof. K. Vrba, Prof. J. Jan

2011: FRVS 2498/2011/F1a: Modernization of laboratory equipments and complete innovation of lectures for course Analog Circuits. Holder: Dr. Herencsár

2010: FRVS 1157/2010/F1a: Innovation of the course Analogue Circuits. Holder: Dr. Herencsár

2009: FRVS 339/2009/G1: Implementation of research results on current-mode circuits to education. Holder: Dr. Herencsár

2009: FRVS 340/2009/F1a: Experimental laboratory for bachelor and diploma theses. Holder: Prof. K. Vrba

2008: FRVS 1648/2008/G1: Support of experimental works in Bachelor Theses. Holder: Dr. Herencsár

2008: FRVS 2057/2008/F1a: Support of experimental works in Diploma Theses on study programme Telecommunications and Information Technologies. Holder: Assoc. Prof. J. Mišurec

MEMBERSHIPS / VOLUNTEERSHIP

2015: IEEE Senior Member (Institute of Electrical and Electronic Engineers)

2015: IEEE Czechoslovakia Section CAS/COM/SP Joint Chapter Chair

2015: IEEE Czechoslovakia Section Membership Development Officer

Since 2015: Member of Radionegineering Society (CZ)

Since 2015: Senior Member of the Institute of Research Engineers and Doctors (IRED)

Since 2012: IEEE Member

Since 2011: Senior Member of the International Association of Computer Science and Information Technology (IACSIT)

Since 2009: IEEE Circuits and Systems Society (CAS) Member

Since 2009: Member of the Association of Computer, Electronics and Electrical Engineers (ACEEE)

Since 2009: Committee Member of the IACSIT Electronics and Electrical Society (EES)

2009 – 2010: Member of the IACSIT

Since 2007:	Member of the International Association of Engineers (IAENG)
2007 – 2010:	IEEE Student Member

EDITORSHIPS / TPC MEMBERSHIPS & PC CHAIR

2017:	Technical Program Committee Member of the XV WASET International Conference on Electronic Trade (ICET 2017), Prague, Czech Republic
2016:	Technical Program Committee Member of the 23rd International Conference on Systems, Signals and Image Processing (IWSSIP 2016), Bratislava, Slovakia – technically co-sponsored by IEEE Czechoslovakia and IEEE Croatia Sections
2015:	Technical Program Committee Member of the 12th IEEE Region 8 AFRICON 2015 Conference, Addis Ababa, Ethiopia – technically co-sponsored by IEEE R8
2015:	Technical Program Committee Member of the 2015 International Conference on Advances in Computers, Communication, and Electronic Engineering (COMMUNE-2015), Srinagar, India
2015:	Local Arrangement Chair of 7th International Congress on Ultra Modern Telecommunications and Control Systems (ICUMT 2015), Brno, Czech Republic – technically co-sponsored by IEEE R8
Since 2014:	Associate Editor of the Journal of Circuits, Systems and Computers (JCSC) published by World Scientific Publishing (SCI-E) – http://www.worldscientific.com/worldscinet/jcsc
Since 2013:	Technical Program Committee Member of the International Conference on Electrical and Electronics Engineering (ELECO), Bursa, Turkey – technically co-sponsored by IEEE R8
2013:	Guest co-editor of the Special Issue on Low-Voltage Low-Power Analogue Devices and Their Applications published in the Radioengineering journal in June 2013 (SCI-E) (Editors: S. Minaei, O. Cicekoglu, D. Biolek, N. Herencsár, J. Koton)
Since 2012:	Co-Editor of the International Journal of Advances in Telecommunications, Electrotechnics, Signals and Systems – http://ijates.org/
2011 – 2013:	Guest co-editor of TSP10 - TSP12 Special Issues on Signal Processing published in the Radioengineering journal (SCI-E)
2011:	Guest co-editor of TSP10 Special Issue on Telecommunications published in the Telecommunication Systems journal of Springer (SCI-E)
2010 – 2012:	PC Chair of the International Conference on Computer and Automation Engineering (ICCAE): ICCAE10 Singapore; ICCAE11 Chongqing, China; ICCAE12 Mumbai, India
Since 2010:	Technical Committee Member of the International Conference on Knowledge in Telecommunication Technologies and Optics (KTTO): KTTO10 Ostrava, Czech Republic; KTTO11 Szczyrk, Poland; KTTO12: Frydlant nad Ostravici, Czech Republic; KTTO13 Hradec nad Moravici, Czech Republic; KTTO14 Malenovice, Czech Republic; KTTO15: Ostravice, Czech Republic
Since 2010:	Deputy-Chair of TSP
Since 2008:	Organizing and Technical Committee Member of the International Conference on Telecommunications and Signal Processing (TSP): TSP - 2008/Paradfurdu, Hungary; 2009/Dunakiliti, Hungary; 2010/Baden near Vienna, Austria; 2011/Budapest, Hungary; 2012/Prague, Czech Republic; 2013/Rome, Italy; 2014/Berlin, Germany; 2015/Prague, Czech Republic; 2015/Vienna, Austria – technically co-sponsored by IEEE Czechoslovakia Section

RESULTS IN TOTAL

Publications:	SCI-E Journal Papers with IF / Other Journal Papers / Conference Proc. Papers 51 / 23 / 89
h-index according to:	Web of Science / SCOPUS / Google Scholar 13 / 14 / 18
# Citations according to:	Web of Science / SCOPUS / Google Scholar 494 / 589 / 1021
# Invited SCI-E or conference papers reviews:	159

ABSTRACT

By following the most recent trend and progress in analog signal processing, this habilitation thesis deals with the latest developments in areas such as single-ended and fully-differential first-order all-pass filter design working in voltage-, current-, mixed-, or dual-mode, quadrature or multiphase oscillators, second- or higher-order frequency filters, and passive component emulator circuits such as grounded voltage controlled resistor, lossy/lossless floating/grounded inductance simulators, floating frequency dependent negative resistor, or floating capacitance multipliers. The behavior of the proposed circuits has been verified by SPICE simulations and in selected cases also by experimental measurements. The thesis consists of 38 author's selected and previously published original scientific and research papers. All presented works were done at Department of Telecommunications, Faculty of Electrical Engineering and Communication, Brno University of Technology in last 5 years (2011–2015). Some of the papers have been partially done in close collaboration with highly recognized colleagues from abroad. The papers reprints are included in exact layout of fullpaper versions at the end of the thesis. All the papers were previously reviewed for the international journals and international conferences proceeding publishing.

ABSTRAKT

Sledováním nejnovějších trendů v oblasti analogového zpracování signálů tato habilitační práce pojednává o aktuálním vývoji v dílčích oborech jako jsou nediferenční a diferenční fázovací články prvního řádu pracující v napěťovém, proudovém, smíšeném nebo duálním režimu, kvadraturní či vícefázové oscilátory, kmitočtové filtry druhého nebo vyššího řádu a emulátory pasivních komponentů jako uzemněný napětím řízený rezistor, ztrátové/bezeztrátové plovoucí/uzemněné simulátory induktoru, plovoucí kmitočtově závislý negativní rezistor nebo plovoucí násobiče kapacity. Chování navržených obvodů bylo ověřeno simulací v prostředí SPICE a ve vybraných případech také experimentálním měřením. Práce je sestavena z celkem 38 vybraných a již dříve publikovaných autorových původních vědeckých článků. Všechny uvedené práce byly realizovány na Ústavu telekomunikací Fakulty elektrotechniky a komunikačních technologií Vysokého učení technického v Brně v uplynulých 5 letech (2011–2015). Některé práce byly částečně vytvořeny ve spolupráci s vysoce uznávanými kolegy ze zahraničí. Vybrané články jsou v originálu habilitační práce vloženy v takové formě, jak byly dříve publikovány. Všechny články byly podrobeny recenznímu řízení před jejich publikováním v odborných časopisech nebo sbornících mezinárodních konferencí.