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**NEW CIRCUIT PRINCIPLES
FOR LOW-VOLTAGE
LOW-POWER
ANALOG CIRCUITS DESIGN**

BRNO UNIVERSITY OF TECHNOLOGY
Faculty of Electrical Engineering and Communication
Department of Microelectronics

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**NEW CIRCUIT PRINCIPLES FOR LOW-VOLTAGE
LOW-POWER ANALOG CIRCUITS DESIGN**

NOVÉ OBVODOVÉ PRINCIPY PRO NÁVRH
ANALOGOVÝCH OBVODŮ S NÍZKOU SPOTŘEBOU
A NÍZKÝM NAPÁJECÍM NAPĚTÍM

TEZE PŘEDNÁŠKY
K PROFESORSKÉMU JMENOVACÍMU ŘÍZENÍ
V OBORU
ELEKTROTECHNICKÁ A ELEKTRONICKÁ TECHNOLOGIE



BRNO 2014

KEYWORDS

Bulk-driven MOST, Floating-gate MOST, Quasi-floating-gate MOST, Low-voltage low-power analog circuit design

KLÍČOVÁ SLOVA

MOS tranzistor řízený substrátovým hradlem, MOS tranzistor s plovoucím hradlem, MOS tranzistor s kvazi plovoucím hradlem, návrh analogových obvodů s nízkým napájecím napětím a nízkou spotřebou.

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1 CURRICULUM VITAE

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Topic of diploma/dissertation thesis	Microsystems for Water Solution Conductivity Measurement	A Novel Technique for Low Voltage Operational Amplifiers

Dates	2000 - 2003	2004 - 2007
Title of qualification awarded	Eng. Engineering Degree in Company Management and Economics	Ph.D. Doctor of Philosophy in Economics and Management
Name and type of organisation providing education and training	Brno University of Technology, Faculty of Business and Management	
Topic of diploma/dissertation thesis	Firm Information System Design	Small and Medium-sized Enterprises: Analysing - Management - Import Export

Dates	2011
Title of qualification awarded	Assoc. Prof. Associate professor in Electrical and Electronic Technology
Name and type of organisation providing education and training	Brno University of Technology, Faculty of Electrical Engineering and Communication
Topic of habilitation thesis	Utilizing the Bulk-driven Technique in Low-voltage Low-power Integrated Circuit Design

Supervised & lectured courses

Faculty of Electrical Engineering and Communication, Brno University of Technology	Design of integrated analog circuit
	Modeling and simulation
	Analog circuit
	New circuit principles for integrated system design
Faculty of Business and Management, Brno University of Technology	Management I, II
	Company Management I, II
	Company establishment and company management
Faculty of Biomedical Engineering, Czech Technical University	Fundamentals of analog medical electronics II

Students supervision

	Bachelor program	Master program
Successfully completed	4	9

	Doctoral program
Total number of students	3
Successfully passed the state doctoral exam	2
Successfully completed the doctoral program	1

Research interests

- Analog integrated circuit design: voltage-, current-, and mixed-mode
- Low-voltage, low-power analog circuit design
- Non-conventional design techniques: Bulk-driven, floating-gate and quasi-floating-gate transistors
- Ultra-low-power low-voltage circuit design for battery-powered implantable and wearable medical devices

Research & publications

- Team member of the following projects:
 1. Sensor, Information and Communication Systems (ED2.1.00/03.0072).
 2. Novel Intelligent Submicron Structures and Microsystems for Advanced Microsensors (P102/11/1379).
 3. Complex innovation of study programs and improving the quality of teaching at FEEC BUT (CZ.1.07/2.2.00/28.0193).
 4. Devices for NeuroControl and NeuroRehabilitation (DeNeCoR).

- Inventor of the national utility model application entitled “Connection of FG MOS and QFG MOS transistors for analogous integrated circuits”. Registered by Industrial Property Office in Czech Republic under registration number 23091, for year 2011.
- Inventor of the national patent application entitled “Connection of FG MOS and QFG MOS transistors for analogous integrated circuits”. Registered by Industrial Property Office in Czech Republic under registration number 303698, for year 2013.
- Inventor of the national patent application entitled “Bulk-controlled sub-threshold MOS resistors for low-voltage applications”. Registered by Industrial Property Office in Czech Republic, for year 2014.

- Associate Editor in Circuits, Systems and Signal Processing, USA, IF: 1.264.
- Associate Editor in IET Circuits, Devices & Systems, UK, IF: 0.912.

- Reviewer for numerous scientific international journals which are indexed in Thomson Reuters Journal Citation Reports.

- Author and co-author of more than 90 journals and international conference publications.
The most recent journals publications with impact factor according to ISI are:
 - [1] **F. Khateb**, M. Kumngern, S. Vlassis, C. Psychalinos, T. Kulej, Sub- volt fully balanced differential difference amplifier, Journal of Circuits Systems and Computers, Singapore, 1-19, **IF: 0.33, 2015**. (Paper accepted for publication).
 - [2] S. Vlassis, **F. Khateb**, Automatic tuning circuit for bulk-controlled subthreshold MOS resistors, Electronics Letters, England, 432-434, **IF: 1.068, 2014**.
 - [3] **F. Khateb**, Bulk-driven floating-gate and bulk-driven quasi-floating-gate techniques for low-voltage low- power analog circuits design, AEU - International Journal of Electronics and Communications, Germany, 64-72, **IF: 0.696, 2014**.
 - [4] **F. Khateb**, M. Kumngern, S. Vlassis, C. Psychalinos, Differential difference current

- conveyor using bulk-driven technique for ultra-low-voltage applications, *Circuits Systems and Signal Processing*, USA, 159-176, **IF: 1.264, 2014.**
- [5] M. Kumngern, **F. Khateb**, P. Phasukkit, S. Tungjitkusolmun, S. Junnapiya, ECCIC- Based Current- Mode Universal Filter with Orthogonal Control of ω_0 and Q , *Radioengineering, CZ*, 687-696, **IF: 0.796, 2014.**
- [6] A. Demartinos, C. Psychalinos, **F. Khateb**, Ultra-Low Voltage CMOS Current-Mode Four-Quadrant Multiplier, *International Journal of Electronics*, England, **IF: 0.751, 2014.** (Paper accepted for publication).
- [7] **F. Khateb**, W. Jaikla, M. Kumngern, P. Prommee, Comparative study of Sub- volt Differential Difference Current Conveyors, *Microelectronics Journal*, England, 1278-1284, **IF: 0.919, 2013.**
- [8] **F. Khateb**, N. Khatib, P. Prommee, W. Jaikla, L. Fucik, Ultra-low voltage tunable transistor based on bulk-driven quasi-floating-gate technique, *Journal of Circuits Systems and Computers*, Singapore, 1350073-1-1350073-13, **IF: 0.238, 2013.**
- [9] W. Jaikla, **F. Khateb**, S. Siripongdee, P. Supavarasuwat, P. Suwanjan, Electronically Tunable Current-mode Biquad Filter Employing CCCDTAs and Grounded Capacitors with Low Input and High Output Impedance, *AEU - International Journal of Electronics and Communications*, Germany, 1005-1009, **IF: 0.551, 2013.**
- [10] **F. Khateb**, S. Vlassis, Low-voltage Bulk-driven Rectifier for Biomedical Applications, *Microelectronics Journal*, England, 642-648, **IF: 0.919, 2013.**
- [11] **F. Khateb**, W. Jaikla, D. Kubánek, N. Khatib, Electronically tunable voltage-mode quadrature oscillator based on high performance CCCDBA, *Analog Integrated Circuits and Signal Processing*, Netherlands, 499-505, **IF: 0.553, 2013.**
- [12] **F. Khateb**, S. Bay Abo Dabbous, S. Vlassis, A Survey of Non-conventional Techniques for Low-voltage Low-power Analog Circuit Design, *Radioengineering, Czech Republic*, 415-427, **IF: 0.687, 2013.**
- [13] M. Kumngern, **F. Khateb**, K. Dejhan, P. Phasukkit, S. Tungjitkusolmun, Voltage-Mode Multifunction Biquadratic Filters Using New Ultra-Low-Power Differential Difference Current Conveyors, *Radioengineering, Czech Republic*, 448-457, **IF: 0.687, 2013.**
- [14] **F. Khateb**, F. Kacar, N. Khatib, D. Kubánek, High-precision Differential-Input Buffered and External Transconductance Amplifier for Low-voltage Low-power Applications, *Circuits Systems and Signal Processing*, USA, 453-476, **IF: 0.982, 2013.**
- [15] **F. Khateb**, N. Khatib, D. Kubánek, Novel Ultra-Low-Power Class AB CCII+ Based on Floating-Gate Folded Cascode OTA, *Circuits Systems and Signal Processing*, USA, 447-464, **IF: 0.752, 2012.**
- [16] **F. Khateb**, N. Khatib, D. Kubánek, Low-voltage Ultra-Low-Power Current Conveyor Based on Quasi- Floating Gate Transistors, *Radioengineering, Czech Republic*, 725-735, **IF: 0.503, 2012.**

[17] **F. Khateb**, P. Horsky, L. Fucik, R. Vrba, M. Pavlík, Comment on “High performance low-voltage QFG-based DVCC and a novel fully differential SC integrator based on it”, IEICE Electronics Express, Japan, 1492-1493, **IF: 0.427, 2012.**

[18] **F. Khateb**, D. Biolek, Bulk-driven current differencing transconductance amplifier, Circuits Systems and Signal Processing, USA, 1071-1089, **IF: 0.752, 2011.**

[19] **F. Khateb**, N. Khatib, D. Kubánek, Novel Low-Voltage Low-Power High-Precision CCII± Based on Bulk-Driven Folded Cascode OTA, Microelectronics Journal, England, 622-631, **IF: 0.787, 2011.**

[20] **F. Khateb**, N. Khatib, J. Koton, Novel Low-Voltage Ultra-Low-Power DVCC Based on Floating- Gate Folded Cascode OTA, Microelectronics Journal, England, 1010-1017, **IF: 0.787, 2011.**

[21] **F. Khateb**, J. Vávra, D. Biolek, A Novel Current-Mode Full- Wave Rectifier Based on One CDTA and Two Diodes, Radioengineering, Czech Republic, 437-445, **IF: 0.503, 2010.**

International citations & h-index

	ISI Web of Knowledge	Scopus
Number of publications	20	25
International citations (without self-citations)	22	44
h-index	6	7

Foreign languages

	Understanding	Speaking	Writing
Czech Language	Excellent	Very good	Very good
English Language	Excellent	Very good	Very good
Arabic Language	Excellent	Excellent	Excellent

2 INTRODUCTION

Prolonging the battery life time and miniaturizing circuits are considered as basic requirements of modern portable electronics and battery-powered implantable and wearable biomedical devices. Therefore, many efforts have been exerted towards minimizing the power consumption and supply voltage of the circuits. During last decades the specific implementations of analog integrated circuits in the area of battery-powered implantable, portable and wearable biomedical applications have become very attractive [1, 2]. Applications such as implantable wearable electronics [3], physiological process monitoring [4], neural recording [5] and medical imaging systems [6] are among the most important. One of the most essential requirements of such applications is the need of extremely low-voltage (LV) supply, low-power (LP) consumption [1-7] and the small size. Many of the aforementioned applications are portable; therefore they require small battery size and lightweight with prolonged lifetime.

Biological signals processing is a challenge for circuit designer since these signals have the attributes of very low frequency and very low amplitudes as shown in Fig. 2.1. The general block diagram of battery-powered implantable and wearable biomedical devices is depicted in Fig. 2.2. By using the transducer, bioelectric potentials of the human body are collected and converted to electrical signals. These signals have small amplitudes therefore they should be amplified to an appropriate level according to application specification. To remove the noise and interferers from the amplified signal the filtering process is necessary. The next step is the rectifying process which could include half- or full-wave rectifiers depending on the signal processing specification. The next stage is signal conditioning circuit, to fit the requirements of the input of the analog-digital-converter (ADC). The ADC is followed by digital signal processing (DSP) and the output is connected to a display or transmitted by antenna. All the above mentioned circuitries are usually supplied by a battery; therefore, the LV supply and LP consumption are both very important. The research of this paper is focused on the analog signal processing part.

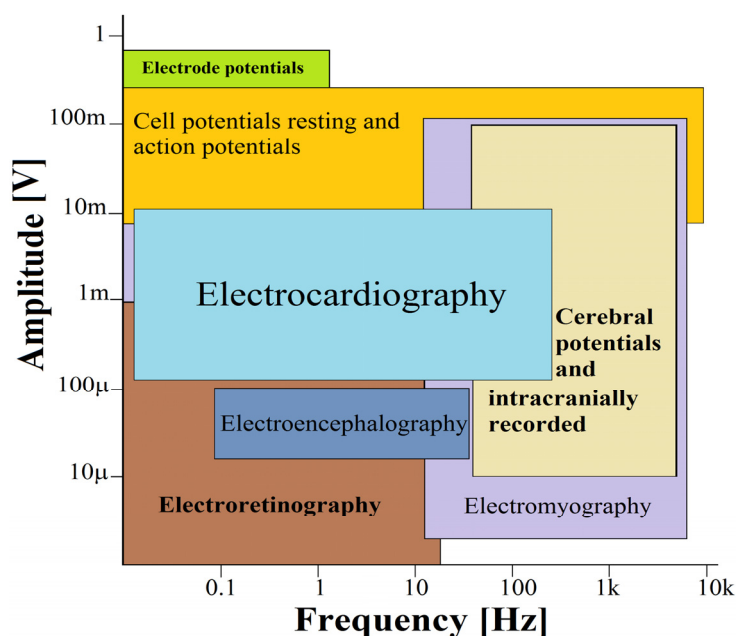


Fig. 2.1 Amplitudes and spectral ranges of the most important biological signals.

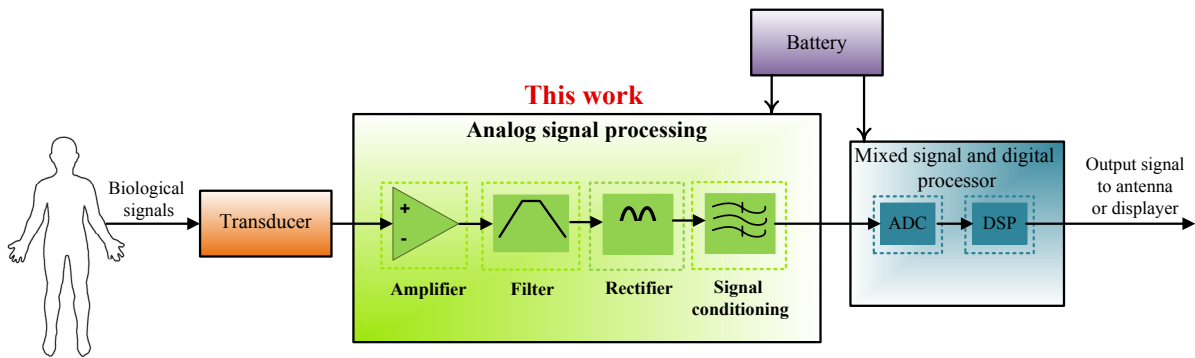


Fig. 2.2 The general block diagram of battery-powered implantable and wearable biomedical devices.

The main drawback in modern CMOS processes is that the threshold voltage remains at relatively high level compared to the supply voltage in order to minimize the leakages [8]. Thus, in analog circuits where the supply voltage decreasing is aimed, the related high threshold voltage is the main limitation. Consequently, non-conventional analog design topologies suitable for operation under LV and LP environments must be invented to get rid of this drawback.

Therefore, research of innovated LV LP analog circuit techniques suitable to be implemented in modern portable electronics, battery-powered implantable and wearable biomedical devices is provided in this work. Based on these innovated techniques various LV LP active elements were proposed to provide the necessary analog signal processing functions i.e. amplifying, filtering and rectifying of biological signals. The voltage supply of these circuits is pushed down to its minimum (1V to 0.5V) and power consumption to the minimum as well (tens of μW to tens of nW) while the other circuit performances are kept attractive, such as the input dynamic range (60% of the supply voltage range up to rail-to-rail). Moreover, to minimize chip area and to have compensation against process and technology P/T variations, innovated techniques are used to replace the passive elements by active ones. These active elements are also capable to work under LV LP. The simulation and experimental results using Cadence platform with transistor models of $0.35\mu\text{m}$ CMOS technology (AMI Semiconductor I3T25/CMOS035) prove the attractive performances of the proposed circuits.

3 NON-CONVENTIONAL TECHNIQUES

The conventional MOST is actually a four terminal device. Depending on the type of used CMOS technology (i.e. N-, P-well or twin-tub) the bulk terminal is usually connected either to negative/positive supply voltage for N-MOS/P-MOS transistor, respectively, or to the related source terminal. However, the bulk-terminal can be used as a signal input instead of connecting it to one of the supply voltages or source terminal. In such a way the threshold voltage requirement is removed from the signal path, and the device which is similar to JFET transistor with depletion characteristics is obtained [9-11]. Therefore the bulk-driven transistor can be a good solution to overcome the threshold voltage limitation and thus is capable of providing the advantage of low voltage operation to almost any analog circuit. Due to the fact that the bulk-driven N-MOST is a depletion-type device, it can work under negative, zero, or even slightly positive biasing conditions. A variety of recent publications describe various attractive implementations of the bulk-driven MOST technique in signal processing LV LP applications [12-26]. Several low-voltage active elements have been designed via this technique, such as voltage followers, Op-Amps, operational transconductance amplifiers (OTAs), second generation current conveyor CCII, current differencing transconductance amplifier (CDTA), differential-input buffered and external transconductance amplifier (DBETA), winner-take-all circuit, and other.

Likewise, floating-gate (FG) and quasi-floating-gate (QFG) MOST techniques are being also used to reduce the supply requirement in a number of new and interesting analog applications. The first well-known application of the FG-MOST was to store data in EEPROMs, EPROMs and FLASH memories [27, 28]. The FG and QFG MOST can be fabricated in all CMOS technologies, although a double poly CMOS technology is preferred. These devices show potentials for analog signal processing, where they may find many applications [29-38]. Several active elements in the analog mode have been designed using the FG and QFG techniques, such as Op Amp, OTA, transconductor, class AB output stage for CMOS Op-Amps, current mirror, differential amplifier, second-generation current conveyor, differential voltage current conveyor, and others.

In fact, the BD, FG and QFG techniques are quite suitable for ultra LV LP (ULV LP) applications mainly battery-powered implantable and wearable medical devices. Even though these non-conventional techniques offer design simplicity and good performance they still suffer from several drawbacks. The FG and QFG MOS transistors (MOST) have lower transconductances and transient frequency values than the conventional gate-driven (GD) MOST. Regarding the BD MOST, it has much lower transconductance and transient frequency values than the conventional GD MOST.

Therefore, novel non-conventional techniques, named as “bulk-driven floating-gate (BD-FG)” MOS transistor (MOST) and “bulk-driven quasi-floating-gate (BD-QFG) MOST” for low-voltage (LV) low-power (LP) analog circuit design were registered as national patent application entitled “Connection of FG MOS and QFG MOS transistors for analogous integrated circuits” by Industrial Property Office in Czech Republic under registration number 303698, for year 2013. The inventors of these techniques are Fabian Khateb and Nabhan Khatib. Also, these new techniques were presented as three interesting contributions in the following international journals: AEU - International Journal of Electronics and Communications, Microelectronics Journal and Circuits Systems and Computers [39-41]. The principle of operation is described in section 4.

4 PRINCIPLE OF NOVEL BD-FG AND BD-QFG TECHNIQUES

To demonstrate the principle of the novel BD-FG and BD-QFG, the N-MOST (P-well CMOS technology) is used. Fig. 4.1 illustrates its simplified cross section with terminals: drain “D”, gate “G”, source “S”, bulk “B” and substrate “Sub”. It is worth mentioning here that the P-well CMOS technology enables to drive separately the bulk-terminals of only N-MOS transistors, since the P-MOS transistors share the same substrate. The “Sub” terminal should be connected to the most positive supply voltage “ V_{DD} ” to guarantee a reversed biased of p-n junction between the bulk and substrate.

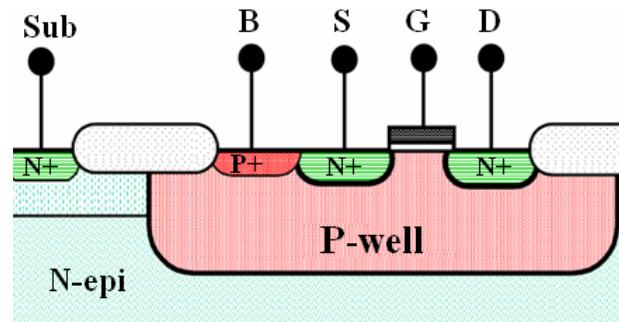


Fig. 4.1 Simplified cross section of N-MOST (P-well CMOS technology).

Fig. 4.2 shows the symbols of the novel BD-FG MOST (a) and BD-QFG MOST (b) whereas Fig. 4.3 shows the possible realization in MOS technology. The idea of utilizing the BD-FG and BD-QFG MOSTs came from the necessity of increasing the total transconductance and the transient frequency of the FG and QFG MOSTs for applications requiring these features.

As shown in Fig. 4.2 (a) the BD-FG MOST is obtained by connecting the input-gate “ G_{in} ” with the bulk-terminal “B” of the FG MOST and the bias-gate “ G_{bias} ” must be connected to a suitable bias voltage. In case of BD-QFG MOST as shown in Fig. 4.2 (b) the input-gate “ G_{in} ” is also connected to the bulk-terminal “B” of the QFG MOST and the bias-gate “ G_{bias} ” must be connected to a suitable bias voltage through a large resistor “ R_{Large} ” which is practically realized by MOST operating in the cutoff region as shown in Fig. 4.3 (b).

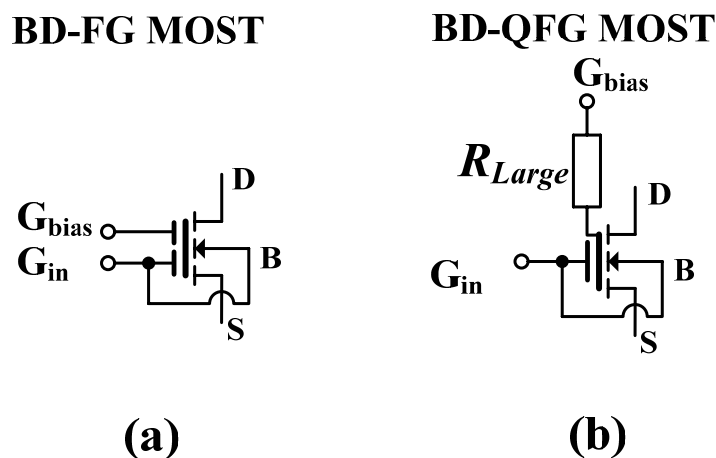


Fig. 4.2 Symbols of the BD-FG MOST (a) and BD-QFG MOST (b).

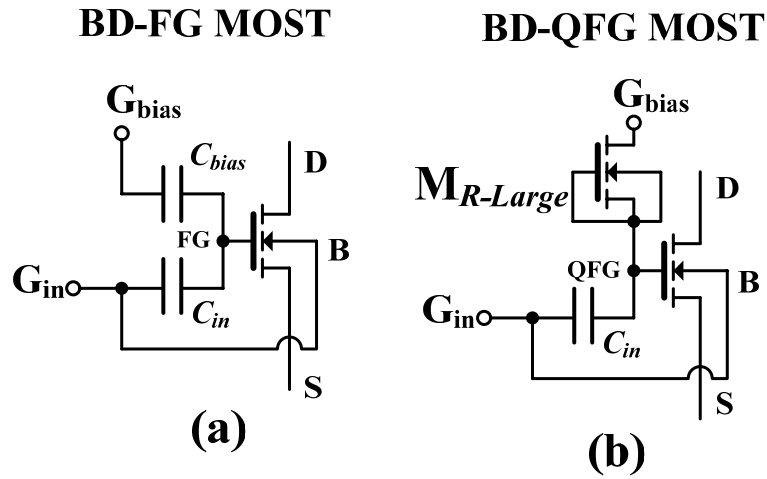


Fig. 4.3 Realization in MOS technology for BD-FG MOST (a) and BD-QFG MOST (b).

Assuming that the “S” terminals of BD-FG and BD-QFG MOSTs at Fig. 4.3 are grounded then their small-signal models are presented in Fig. 4.4 (a) and (b), respectively.

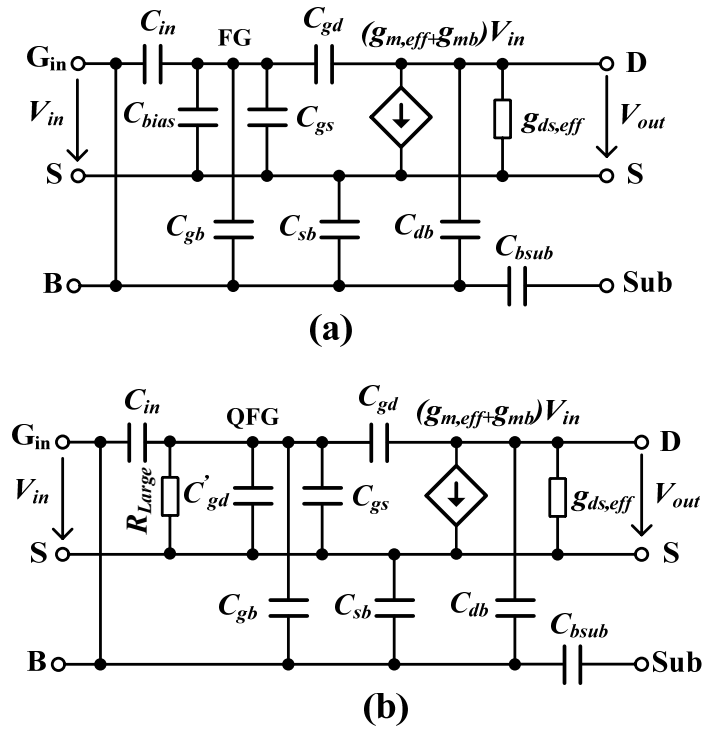


Fig. 4.4 Small-signal models for BD-FG and BD-QFG MOSTs.

Based on Fig. 4.4, Tab. 4.1 shows relations for transconductance, threshold voltage, output conductance, and transient frequency of the GD, BD, FG, QFG, BD-FG and BD-QFG MOSTs operating in saturation region.

	Transconductance	Output conductance	Threshold voltage	Transient frequency
GD	$g_m = K \frac{W}{L} (v_{gs} - V_T)$	$g_{ds} = \lambda_{ds}$	$V_T = V_{T0} \pm \gamma \left(\sqrt{2 \phi_F - \gamma_{bs}} - \sqrt{2 \phi_F } \right)$	$f_T \approx \frac{g_m}{2\pi C_{gs}}$
BD	$g_{mb} = \frac{C_{BC}}{C_{GC}} g_m \approx (0.2-0.4)g_m$	$g_{ds} = \lambda_{ds}$	removed	$f_{Tb} \approx \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} \approx (0.3-0.5)f_T$
FG and QFG	$g_{m,eff} = \frac{C_{in}}{C_{total}} g_m \approx (0.5-0.6)g_m$	$g_{ds,eff} = \frac{C_{gd}}{C_{total}} g_m + g_{ds}$ increased	$V_{T,FG,QFG} = \frac{V_T - V_{bias} k_2}{k_1}$ reduced or removed here: $k_1 = \frac{C_{in}}{C_{total}}$ and $k_2 = \frac{C_{bias}}{C_{total}}$	$f_{T,FG,QFG} \approx \frac{g_{m,eff}}{2\pi C_{gs}} \approx (0.5-0.6)f_T$
BD-FG and BD-QFG	$g_{m,BD-FG,BD-QFG} = g_{m,eff} + g_{mb} \approx (0.7-1)g_m$	$g_{ds,BD-FG,BD-QFG} \approx \frac{C_{gd}}{C_{total}} g_m + g_{ds}$ increased	removed	$f_{T,BD-FG,BD-QFG} \approx \frac{g_{m,BD-FG,BD-QFG}}{2\pi(C_{bs} + C_{bsub} + C_{gs})}$ $f_{T,EFQ} \approx (0.7-0.9)f_T$

Tab. 4.1 Relations of transconductance, threshold voltage, output conductance and transient frequency for GD, BD, FG, QFG, BD-FG, and BD-QFG MOSTs operating in saturation region.

where:

C_{sb}	Source-bulk capacitance	V_T	Threshold voltage
C_{gb}	Gate-bulk capacitance	C_{gs}	Gate-source capacitance
C_{GC}	Total gate channel capacitance	C_{BC}	Total bulk channel capacitance
C_{total}	Total capacitance seen from the floating-gate/quasi-floating-gate of the FG-MOST/QFG-MOST	V_{T0}	Threshold voltage at $V_{bs}=0$
C_{gd}	Gate-drain capacitance	V_{bs}	Bulk-source voltage
C_{bsub}	Bulk-substrate capacitance	γ	Bulk threshold parameter
C_{db}	Drain-bulk capacitance	K	Transconductance parameter
C_{in}	Input capacitance between floating-gate/quasi-floating-gate and input-terminal of the FG-MOST/QFG-MOST	Φ_F	Surface potential
C_{bias}	Bias capacitance between floating-gate- and bias-terminal of the FG-MOST	λ	Channel length modulation coefficient
f_T	Transient frequency	$g_{m,eff}$	Effective transconductance of the FG-MOST/QFG-MOST
g_m	Gate transconductance	g_{ds}	Output conductance
g_{mb}	Bulk transconductance	$g_{ds,ef}$	Effective output conductance of FG-MOST/QFG-MOST
R_{Larag}	Gate-drain resistance of $M_{R-Larag}$,	f	Gate-drain capacitance of $M_{R-Larag}$

It is clear that the BD-FG and BD-QFG MOSTs offer better parameters than the BD, FG and QFG MOSTs. Both transconductance and transient frequency are increased. However, the parasitic capacitance between the “B” and substrate “Sub” terminal i.e. $C_{b\text{sub}}$ degrades the transient frequency of the BD-FG and BD-QFG MOSTs as shown in Tab. 4.1. Therefore, for applications that require high transient frequency the Silicon on Insulator SOI technology should be used rather than bulk CMOS one.

It is worth mentioning here that that total capacitance seen from the FG MOST is higher than the one seen from QFG, because the value of C_{bias} in FG is usually larger than gate-drain capacitance of the $M_{R\text{-Large}}$ in QFG. This results in the transconductance of the QFG MOST being larger than FG MOST, also the transconductance of the BD-QFG MOST is larger than BD-FG MOST.

To demonstrate a comparison study between the previously mentioned techniques and the novel techniques Fig. 4.5 shows a principle of the common-source amplifier based on a GD MOST (a), BD MOST (b), FG MOST (c), and QFG MOST (d), in comparison with the novel BD-FG MOST (e) and BD-QFG MOST (f), as an example.

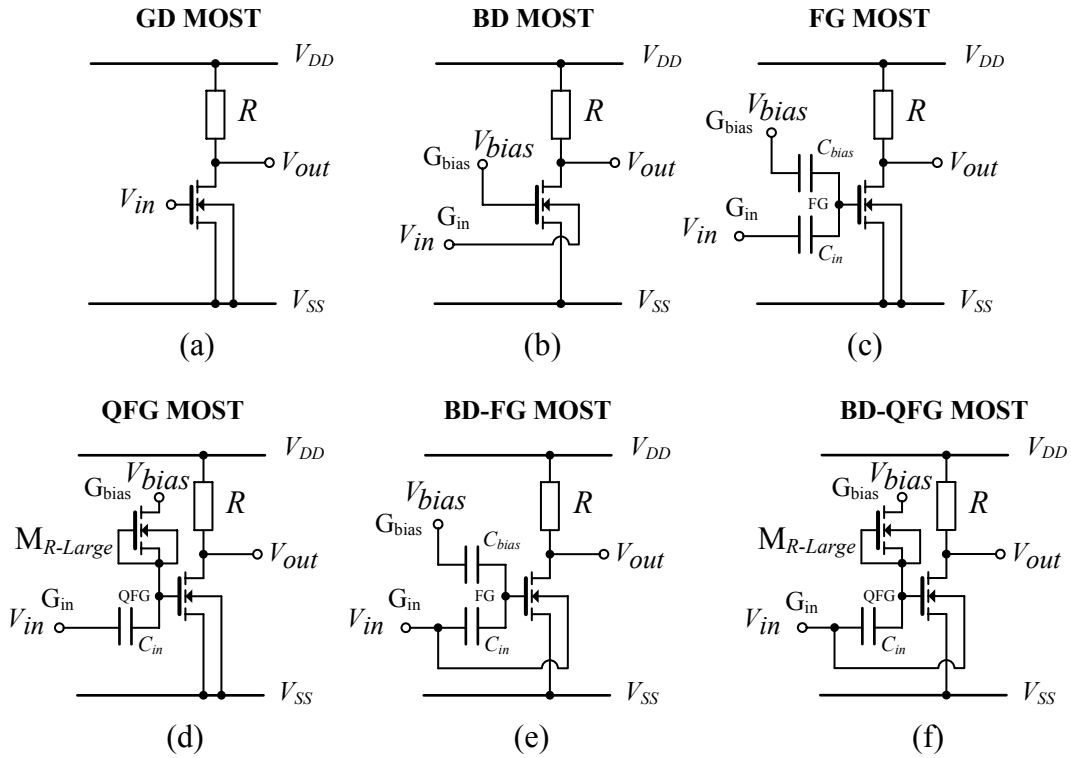


Fig. 4.5 Common-source amplifier based on: conventional GD (a), BD (b), FG (c), QFG (d), BD-FG (e), and BD-QFG (f) MOSTs.

Fig. 4.6 shows the drain currents versus gate-source of GD MOST, bulk-source of BD MOST, gate-source of FG-MOST, gate-source of QFG-MOST, gate-bulk-source of BD-FG-MOST and BD-QFG-MOST voltages of N-MOSTs from Fig. 4.5. It is obvious that the drain current in a conventional GD MOST increases when the gate-source voltage exceeds the threshold voltage. In bulk-driven MOST, the gate-source voltage is biased on a constant voltage V_{bias} and the input signal V_{in} is applied at the bulk-terminal, thus the threshold voltage in this set-up is removed from the signal path. In the FG-MOST and QFG-MOST, the bias-gate is set on bias voltage whereas the input-gate is used for the input signal; here the threshold voltage could be decreased

or completely removed from the signal path. For BD-FG MOST and BD-QFG MOST the threshold voltage is completely removed from the signal path and the transconductance value is closed or slightly lower to the conventional MOST.

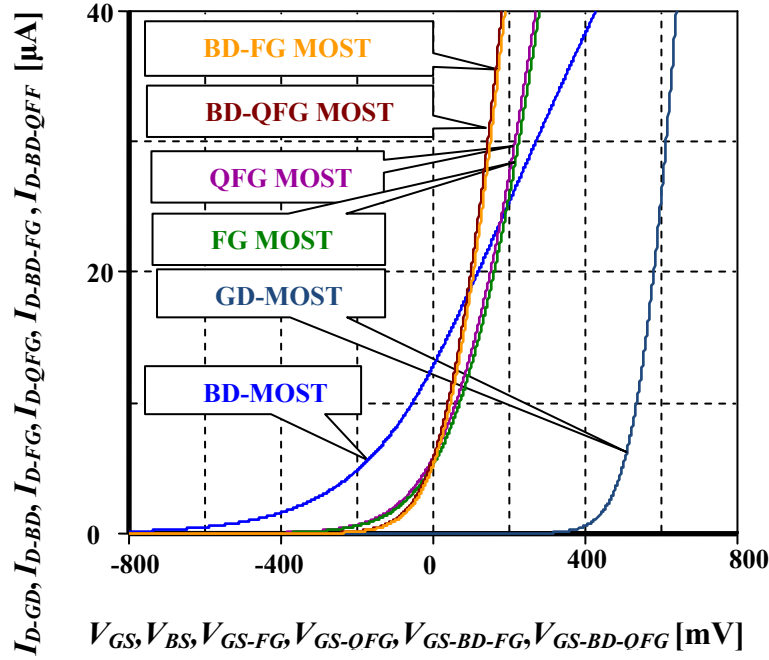


Fig. 4.6 Drain currents versus gate-source of GD MOST, bulk-source of BD MOST, gate-source of FG-MOST, gate-source of QFG-MOST, gate-bulk-source of BD-FG-MOST and BD-QFG-MOST voltages of N-MOSTs from Fig. 4.5.

4.1 COMPARATIVE STUDY OF SUB-VOLT DIFFERENTIAL DIFFERENCE CURRENT CONVEYORS BASED ON BD, QFG AND BD-QFG TECHNIQUES

This part presents a comparison study of three ULV differential difference current conveyor (DDCC) blocks based on BD, QFG and BD-QFG techniques. The significant increment of the transconductance and the bandwidth values of the BD-QFG is clearly observed. The proposed CMOS structures of the DDCCs work at ± 300 mV supply voltage and $18.5 \mu\text{W}$ power consumption. The simulation results using $0.18 \mu\text{m}$ CMOS n-Well process from TSMC show the features of the proposed circuits.

The symbol of the DDCC is shown in Fig. 4.7. The relationships between voltages and currents of the DDCC terminals can be described by the following matrix:

$$\begin{pmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \\ 0 & 0 & 0 & \alpha & 0 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \end{pmatrix} \quad (4.1)$$

where $\beta_j = 1 - \epsilon_{jv}$ for ($j=1, 2, 3$) and $\alpha = 1 - \epsilon_i$, whereas ϵ_{jv} and ϵ_i ($|\epsilon_{vj}| \ll 1$ and $|\epsilon_i| \ll 1$) represent voltage and current tracking errors of the DDCC, respectively. In ideal case $\beta_j = \alpha = 1$.

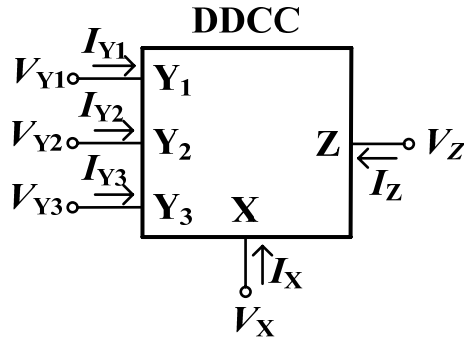


Fig. 4.7 Electrical symbol of DDCC.

Thanks to the wide applicability and attractive features of the DDCC, three ULV LP DDCCs are carried out utilizing BD, QFG and BD-QFG techniques, in order to clarify the performances of these techniques and provide feasible comparison study among them.

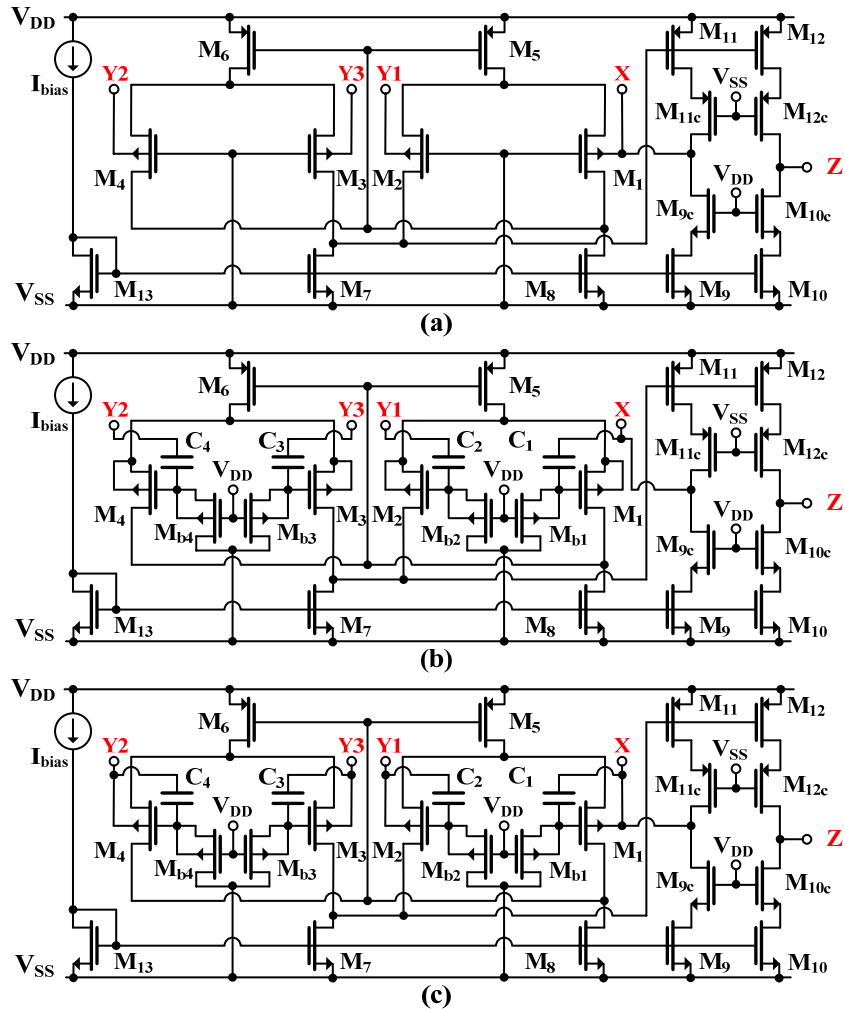


Fig. 4.8 Ultra-LV DDCCs MOS structure based on BD MOST (a), QFG MOST (b) and BD-QFG MOST (c).

The internal CMOS structure of the ULV LP BD, QFG and BD-QFG DDCCs are shown in Fig. 4.8 (a), (b) and (c), respectively. From Fig. 4.8 (a), (b) and (c) the multiple output current mirror M_{13} , M_7 , M_8 , M_9 and M_{10} provide a constant bias current I_{bias} to each branch of the circuit. Transistors M_7 and M_8 are common for both differential input stages and they form the active load for them. Transistors M_5 and M_6 act as tail current sources for the first and second differential input stages, respectively. Cascode transistors M_9 – M_{9c} and M_{11} – M_{11c} create the second stage for both differential input stages. Due to the unity gain connection between the output of the second stage and the input of M_1 the voltage transfers are ensured. Finally, cascode transistors M_{10} – M_{10c} and M_{12} – M_{12c} create the output stage for DDCC and they provide a current copy from the X terminal to Z.

Regarding the differential pairs, they were designed as follow:

BD DDCC in Fig. 4.8 (a): two couples BD MOSTs M_1 , M_2 and M_3 , M_4 are utilized to build the two differential input stages. The gates of these transistors are connected directly to the negative supply voltage to create the conductive channel under the gates and the input signals are connected directly to the bulk terminals of these transistors.

QFG DDCC in Fig. 4.8 (b): two couples QFG MOSTs M_1 , M_2 and M_3 , M_4 are utilized to build the two differential input stages. The gates of these transistors are connected to the negative supply voltage through a high value resistors created by transistors that operate in cutoff region M_{b1} , M_{b2} , M_{b3} and M_{b4} , respectively. Thus the conductive channels are created under the gates. The input terminals of M_1 , M_2 , M_3 and M_4 are capacitively coupled via C_1 , C_2 , C_3 and C_4 , respectively, to their quasi-floating gate terminals.

BD-QFG DDCC in Fig. 4.8 (c): two couples BD-QFG MOSTs M_1 , M_2 and M_3 , M_4 are utilized to build the two differential input stages. The gates of these transistors are connected to the negative supply voltage through high value resistors created by transistors operating in cutoff region M_{b1} , M_{b2} , M_{b3} and M_{b4} , respectively. Thus the conductive channels are created under the gates. The input terminals of M_1 , M_2 , M_3 and M_4 are capacitively coupled via C_1 , C_2 , C_3 and C_4 , respectively, to their quasi-floating gate terminals from one side and directly coupled to their bulk terminals from other side.

A straightforward analysis of a small-signal equivalent circuit of the DDCCs brings the following expressions for β_j and α . The voltage transfer ratios β_j can be expressed as following:

For the BD DDCC:

$$\beta_{1,\text{BD}} = \frac{V_X}{V_{Y1}} = \frac{g_{\text{mb},M1}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}}{1 + g_{\text{mb},M2}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}} \approx \frac{g_{\text{mb},M1}}{g_{\text{mb},M2}} \approx 1 \quad (4.2)$$

$$\beta_{2,\text{BD}} = \frac{V_X}{V_{Y2}} = \frac{g_{\text{mb},M1}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}}{1 + g_{\text{mb},M4}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}} \approx \frac{g_{\text{mb},M1}}{g_{\text{mb},M4}} \approx 1 \quad (4.3)$$

$$\beta_{3,\text{BD}} = \frac{V_X}{V_{Y3}} = \frac{g_{\text{mb},M1}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}}{1 + g_{\text{mb},M3}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}} \approx \frac{g_{\text{mb},M1}}{g_{\text{mb},M3}} \approx 1 \quad (4.4)$$

For the QFG DDCC:

$$\beta_{1,\text{QFG}} = \frac{V_X}{V_{Y1}} = \frac{g_{\text{m},\text{QFG},M1}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}}{1 + g_{\text{m},\text{QFG},M2}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}} \approx \frac{g_{\text{m},\text{QFG},M1}}{g_{\text{m},\text{QFG},M2}} \approx 1 \quad (4.5)$$

$$\beta_{2,\text{QFG}} = \frac{V_X}{V_{Y2}} = \frac{g_{\text{m},\text{QFG},M1}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}}{1 + g_{\text{m},\text{QFG},M4}r_{\text{out1}}g_{\text{m},M11}r_{\text{out2}}} \approx \frac{g_{\text{m},\text{QFG},M1}}{g_{\text{m},\text{QFG},M4}} \approx 1 \quad (4.6)$$

$$\beta_{3,\text{QFG}} = \frac{V_X}{V_{Y3}} = \frac{g_{m,\text{QFG},M1} r_{\text{out1}} g_{m,M11} r_{\text{out2}}}{1 + g_{m,\text{QFG},M3} r_{\text{out1}} g_{m,M11} r_{\text{out2}}} \approx \frac{g_{m,\text{QFG},M1}}{g_{m,\text{QFG},M3}} \approx 1 \quad (4.7)$$

For the BD-QFG DDCC:

$$\beta_{1,\text{BD-QFG}} = \frac{V_X}{V_{Y1}} = \frac{g_{m,\text{BD-QFG},M1} r_{\text{out1}} g_{m,M11} r_{\text{out2}}}{1 + g_{m,\text{BD-QFG},M2} r_{\text{out1}} g_{m,M11} r_{\text{out2}}} \approx \frac{g_{m,\text{BD-QFG},M1}}{g_{m,\text{BD-QFG},M2}} \approx 1 \quad (4.8)$$

$$\beta_{2,\text{BD-QFG}} = \frac{V_X}{V_{Y2}} = \frac{g_{m,\text{BD-QFG},M1} r_{\text{out1}} g_{m,M11} r_{\text{out2}}}{1 + g_{m,\text{BD-QFG},M4} r_{\text{out1}} g_{m,M11} r_{\text{out2}}} \approx \frac{g_{m,\text{BD-QFG},M1}}{g_{m,\text{BD-QFG},M4}} \approx 1 \quad (4.9)$$

$$\beta_{3,\text{BD-QFG}} = \frac{V_X}{V_{Y3}} = \frac{g_{m,\text{BD-QFG},M1} r_{\text{out1}} g_{m,M11} r_{\text{out2}}}{1 + g_{m,\text{BD-QFG},M3} r_{\text{out1}} g_{m,M11} r_{\text{out2}}} \approx \frac{g_{m,\text{BD-QFG},M1}}{g_{m,\text{BD-QFG},M3}} \approx 1 \quad (4.10)$$

where r_{out1} and r_{out2} are the output impedances of the first and second stages of all DDCCs, respectively, and are given by:

$$r_{\text{out1}} = \frac{1}{g_{o,M2} + g_{o,M7}} \quad (4.11)$$

$$r_{\text{out2}} = \frac{1}{\frac{g_{o,M9} g_{o,M9c}}{g_{m,M9c} + g_{mb,M9c}} + \frac{g_{o,M11} g_{o,M11c}}{g_{m,M11c} + g_{mb,M11c}}} \quad (4.12)$$

where the g_m and g_{mb} denote the gate and bulk transconductance of MOST, g_o is the transistor output conductance.

The current transfer ratio α is the same for the three DDCCs and is given by:

$$\alpha \approx \frac{g_{m,M12}}{g_{m,M11}} \approx 1 \quad (4.13)$$

The resistance of the X terminal is:

For the BD DDCC:

$$R_{X,b} \approx \frac{1}{g_{mb,M1} r_{\text{out1}} g_{m,M11}} \quad (4.14)$$

For the QFG DDCC:

$$R_{X,\text{QFG}} \approx \frac{1}{g_{m,\text{QFG},M1} r_{\text{out1}} g_{m,M11}} \quad (4.15)$$

For the BD-QFG DDCC:

$$R_{X,\text{BD-QFG}} \approx \frac{1}{g_{m,\text{BD-QFG},M1} r_{\text{out1}} g_{m,M11}} \quad (4.16)$$

It is notable from Eqs. (4.14)-(4.16) that the smallest resistance of X terminal is obtained by utilizing the BD-QFG technique, thanks to the higher transconductance value $g_{m, \text{BD-QFG}, M1}$ in comparison to BD and QFG techniques.

Finally, resistance of the Z terminal of the proposed DDCCs can be expressed as:

$$R_Z \approx \frac{1}{\frac{g_{o, M10} g_{o, M10c}}{g_{m, M10c} + g_{mb, M10c}} + \frac{g_{o, M12} g_{o, M12c}}{g_{m, M12c} + g_{mb, M12c}}} \quad (4.17)$$

The cascode transistors M_{10} – M_{10c} and M_{12} – M_{12c} are used to achieve significantly high value of R_Z as shown in Eq. (4.17).

The differential input stages use the BD, QFG and BD-QFG flipped voltage follower, thus the minimum power supply voltage is expressed by:

$$V_{\text{Sup}}^{\min} = V_{\text{GS}, M5, M6} + V_{\text{DS}, M7, M8} \quad (4.18)$$

Eq. (4.18) shows the capability of the proposed BD, QFG and BD-QFG DDCCs structures of operating under same ULV supply.

The most important features of the BD, QFG, and BD-QFG DDCC are listed in Tab. 4.2. Note that these DDCCs were simulated under the same conditions of supply voltage ± 0.3 V and power consumption of $18.5 \mu\text{W}$. This facilitates the comparison among other parameters. Hence, it is notable from Tab. 4.2 that the BD-QFG technique offers extended bandwidth thanks to its higher transconductance value in comparison to the BD and QFG techniques. Moreover, The BD-QFG DDCC can process DC and AC, unlike the QFG DDCC which blocks the DC signals.

Tab. 4.2 Simulation results of the ULV LP BD, QFG and BD-QFG DDCCs.

Characteristics	BD	QFG	BD-QFG
Supply voltage	± 0.3 V	± 0.3 V	± 0.3 V
Power consumption	$18.5 \mu\text{W}$	$18.5 \mu\text{W}$	$18.5 \mu\text{W}$
-3 dB bandwidth: $I_Z/I_X, V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3}$	27 MHz	24 MHz	42 MHz
Current gain I_Z/I_X and voltage gains: $V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3}$	1	1	1
DC current range	-8 to 8 μA	blocked	-8 to 8 μA
Current error range	< 3 nA	-	< 3 nA
DC voltage range	-150 to 150 mV	blocked	-150 to 150 mV
Voltage error range	< 130 μV	-	< 130 μV
Node X parasitic impedances: R/L	1.6 k Ω / 270 μH	1.7 k Ω / 103 μH	1 k Ω / 65 μH
Node Z parasitic impedance: R/C	10.2 M Ω /0.12 pF	0.22 M Ω /0.9 pF	10.2 M Ω /0.12 pF
Node Y_1, Y_2, Y_3 parasitic impedances: R_Y/C_Y	0.12 T Ω / 5 fF	1.6 T Ω / 500 fF	0.12 T Ω / 100 fF
CMOS technology	0.18 μm	0.18 μm	0.18 μm

5 NOVEL AUTOMATIC TUNING CIRCUIT FOR BULK-CONTROLLED SUB-THRESHOLD MOS RESISTORS

In this part, a simple automatic tuning circuit is proposed which is suitable for controlling the very large channel resistance of weak-inverted transistors operated in the linear regime. The channel resistance for 1.2M Ω nominal value presents about $\pm 0.6\%$ variation for -20°C to 80°C temperature range, $\pm 5\%$ variation at process/temperature (P/T) corners and Total Harmonic Distortion $THD=-42\text{dB}$ for differential signals. The supply voltage is $V_{DD}=1\text{V}$ and the current consumption is about 470nA. The proposed concept and the performance were confirmed and evaluated by simulations using standard 0.35 μm CMOS process.

It's worth mentioning here that this new and attractive principle entitled "sub-threshold MOS resistors for low-voltage supply applications" was registered as national patent application by the Industrial Property Office in Czech Republic in year 2014. The inventors of this principle are Spyridon Vlassis and Fabian Khateb. Also, this principle was presented in the international journal Electronics Letters in year 2014 [42].

The usage of channel resistance R_{mos} of a MOS device in linear regime finds many applications in analog integrated circuits/systems such in MOSFET-C filters topologies and linearly tunable transconductors. The main benefit is that R_{mos} can be automatically controlled and therefore the bandwidth of a MOSFET-C filter can be tuned, R_{mos} can be compensated against P/T variations or an amplifier gain can be programmable. Last years the emerging area of biomedical circuits and signal processing was requiring very high resistor values to realize very low cut-off frequency for high-pass filtering along with low voltage/power specifications. Therefore, MOS device in the sub-threshold is the best choice to meet these requirements.

All relative publications employing the gate terminal of a weak-inverted MOS for tuning purposes present very small headroom for low supplies limiting the R_{mos} tuning range and P/T compensation capabilities. Also, the non-linearity of MOS devices can be compensated using voltage and/or current division between linear polysilicon resistors and MOS devices and employing differential topologies as well.

The drain current of a pMOS in weak inversion assuming that the gate (V_G), source (V_S) and drain (V_D) voltages are referred to the bulk (or well) voltage V_W is given by

$$I_D = A I_o e^{\frac{(k-1)V_W - V_G}{U_t}} \left(\frac{V_S}{e^{U_t}} - \frac{V_D}{e^{-U_t}} \right) \quad (5.1)$$

where I_o is a process and temperature dependent current, $A=W/L$ the device aspect ratio, k is the gate coupling factor and $U_t=kT/q$. The other factors have their usual meanings. Assuming that $V_S=V_{CM}+V_R/2$ and $V_D=V_{CM}-V_R/2$, Eq. (5.1) is converted to

$$I_D = A I_{Do}(V_W) 2 \sinh\left(\frac{V_R}{2U_t}\right) \quad (5.2)$$

where $I_{Do}(V_W)=I_o \exp\{[(k-1)V_W - V_G + V_{CM}]/U_t\}$, V_{CM} is a common-mode voltage of V_S and V_D , and V_R is a differential voltage with relatively small value which bias the pMOS device in the linear regime. Using Taylor series approximation around zero and neglecting the third and higher odd order terms, I_D will be given by

$$I_D \approx A I_{Do}(V_W) \frac{V_R}{U_t} \quad (5.3)$$

It should be mentioned that the function $\sinh(x)$ doesn't contain even order terms. Thus, the channel resistance R_{mos} will be given by

$$R_{mos} = \frac{V_R}{I_D} = \frac{U_t}{AI_{D0}(V_W)} \quad (5.4)$$

and it is obvious that it can be controlled by the bulk-voltage V_W . Fig. 5.1 (a) presents the topology that actually implements Eq. (5.4) and it can automatically control R_{mos} using the bulk terminal of M_m . Using current mirrors $M_{1,2,3}$ and $M_{4,5}$ the current I_R is forced to be equal to the drain current of M_m . As it will be explained later, two opamps (OA1, OA2) apply the differential voltage V_R across source and drain terminals of M_m with $V_{CM} = V_{DD}/2$. Both opamps's topology are based on two-stage Miller opamp configuration in which the input stage, as it is shown in Fig. 5.1 (b), which is based on bulk-driven pMOS differential pair. Bulk-driven topologies are more efficient for small supply-to-threshold voltage ratios (V_{DD}/V_T). In addition, unbalanced bulk-driven pairs are employed in order to generate V_R without additional circuits. Based on Fig. 5.1 (b) and using Eq. (5.1), the input offset voltage $V^{(+)} - V^{(-)}$ between differential inputs of opamps will be: $V^{(+)} - V^{(-)} = V_{WS7} - V_{WS6} = [1/(k-1)]U_t \ln(A_7/A_6)$, where A_6 and A_7 are the aspect ratios of M_6 and M_7 , respectively. According to the aforementioned analysis and employing Eq. (5.4), $R_{mos,m}$ will be given by:

$$R_{mos,m} = \frac{V_R}{I_R} = \frac{2}{k-1} \frac{U_t \ln(A_7/A_6)}{I_R} \quad (5.5)$$

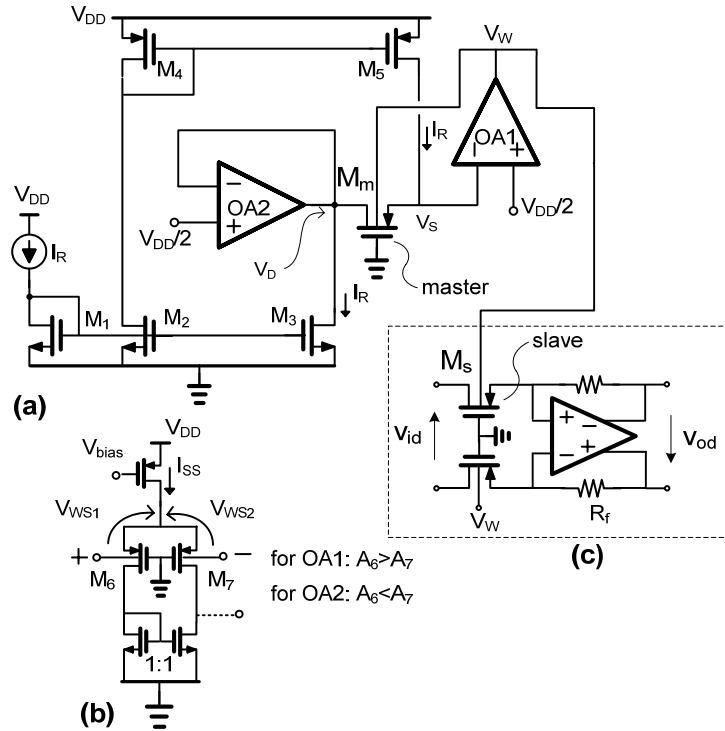


Fig. 5.1 (a) Proposed bulk-controlled sub-threshold MOS resistor automatic tuning circuit (b) Input stage of two-stage Miller OA1,2 with unbalanced bulk-driven pMOS differential pair and (c) inverting amplifier with sub-threshold MOS resistors and linear resistance (R_f) feedback elements.

A short explanation of the operation is that OA1 modifies V_W according to Eq. (5.4) in order to satisfy that $I_D = I_R$ for a specific V_R . Both OA1, OA2 are also used for the application of $2V_R$ between drain and source of M_m . Therefore, by choosing V_R and I_R we can define the value of $R_{mos,m}$. The benefit of the proposed structure is larger headroom for the bulk control voltage compared with a gate control voltage for keeping the M_m in the sub-threshold and linear regime.

Eq. (5.5) shows also the $R_{mos.m}$ dependency from temperature and process through factors U_t and I_R , respectively. The temperature dependency can be compensated using a proportional to absolute temperature (PTAT) current, e.g. $I_R=I_{PTAT} \sim U_t/R$, assuming that R features small temperature coefficient. In case we need to compensate both temperature and process variations we can employ $I_R=I_{PTAT}$ along with a very accurate off-chip resistor R .

Using the master/slave technique we can control the channel resistance $R_{mos.s}$ of a slave pMOS (M_s) using M_m which acts as the master device, as it is presented in Fig. 5.1 (c). The slave device M_s is a part of the inverting amplifier which acts as resistor. The automatic tuning circuit adjusts simultaneously the bulk voltage of both M_s and M_m producing an $R_{mos.s}$ which is given by

$$R_{mos.s} = \frac{A_m}{A_s} R_{mos.m} \quad (5.6)$$

in which it is obvious that $R_{mos.s}$ can be controlled by the aspect ratios of the master and slave devices.

The proposed tuning circuit was designed and tested in Cadence Platform using transistor models of 0.35 μ m CMOS AMIS process. The threshold voltage of the pMOS devices is $V_{T0}=0.6$ V, the current consumption is 470nA and the supply voltage is $V_{DD}=1$ V. The nominal aspect ratio of the master device is $A_m=60/12$. The nominal R_{mos} is defined around 1.2M Ω using $I_R=I_{PTAT}(27^\circ\text{C})=40$ nA, $A_6=28/4$ and $A_7=32/4$. Using the last aspect ratios, the unbalanced differential pair Fig. 5.1 (b) produces about 50mV input offset.

The stability of the $R_{mos.s}$ over temperature was tested also for values 2.4M Ω and 0.6M Ω using the aspect ratios $A_s=0.5A_m$ and $A_s=2A_m$, respectively, using a PTAT current. As shown in Fig. 5.2 the $R_{mos.s}$ for temperatures between -20°C and 80°C exhibit about $\pm 0.6\%$ variation. Also, the worst case variation of $R_{mos.s}$ for both process and temperature corners was $\pm 5\%$.

The linearity was tested using the simulation setup of Fig. 5.1 (c). The bulk voltage of the MOS under test device M_s is equal to V_W and both input and output common-mode of the differential amplifier are equal to 0.5V. The THD is less than -42 dB for 30mV input amplitude at 10kHz.

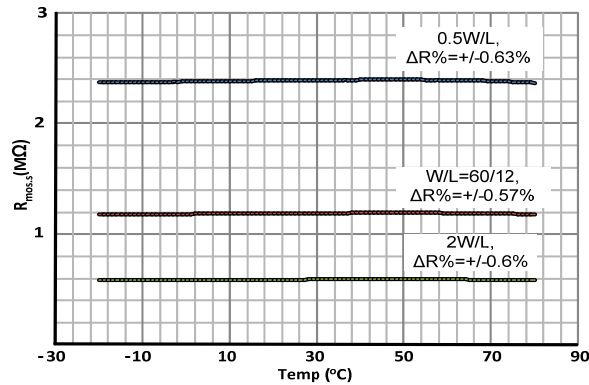


Fig. 5.2 $R_{mos.s}$ variation for 2.4, 1.2 and 0.6M Ω over temperature.

6 CONCLUSION

Enhancing the performances of analog circuits with sub-volt supplies becomes a great challenge for circuit designers. Techniques such as bulk-driven (BD), floating-gate (FG) and quasi-floating gate (QFG) count among the suitable ones for ultra-low voltage (ULV) operation capability with extended input voltage range and simple CMOS circuitry. However, in comparison to the conventional gate-driven (GD) MOS transistor (MOST), these techniques suffer from several disadvantages such as low transconductance value and bandwidth that limits their applicability for many applications. Therefore, this work deals with research of new low-voltage low-power analog circuits design techniques for battery-powered implantable and wearable biomedical devices. The voltage supply of these circuits is then pushed down to the minimum (1V to 0.5V) and the power consumption to the minimum as well (tens of μW to tens of nW) while the other circuit performances are kept attractive, such as the input dynamic range (60% of the supply voltage range up to rail-to-rail). The simulation and experimental results using Cadence platform with transistor models of 0.35 μm CMOS AMIS process prove the attractive performances of the proposed circuits.

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ABSTRAKT

V dnešní době je prodlužování životnosti baterie a zmenšování plochy integrovaných obvodů považováno za základní požadavky, které jsou kladeny na moderní přenosnou elektroniku a implementované a nositelné biomedicínské přístroje, jež jsou napájeny baterií. V posledních letech bylo vynaloženo mnoho úsilí k minimalizování napájecího napětí obvodů a jejich celkové spotřeby. Nicméně návrháři analogových obvodů naráží na problém zachovat spolehlivé fungování analogových obvodů při snížení napájecího napětí, jelikož prahové napětí MOS tranzistorů a napájecí napětí není sníženo úměrně. Proto je třeba zvolit inovativní techniky, aby byla překonána poměrně vysoká hodnota prahového napětí MOS tranzistorů. Z tohoto důvodu se tato práce zabývá výzkumem nových technik pro navrhování analogových obvodů s nízkým napájecím napětím a nízkou spotřebou, které budou používány v implementovaných a nositelných biomedicínských přístrojích, jež jsou napájeny baterií.

Na základě těchto nových technik bylo navrženo několik analogových obvodů s nízkým napájecím napětím a nízkou spotřebou potřebných pro zpracování vybraných biologických signálů, tj. zesilování, filtrování a usměrňování. Napájecí napětí těchto obvodů bylo sníženo na minimum (hodnota v rozmezí 1 V až 0,5 V) a celková spotřeba též na minimum (hodnota v rozmezí desítek μW do desítek nW), zatímco ostatní parametry obvodů jsou stále atraktivní, jako například dynamický rozsah vstupního napětí (60 % z rozsahu napájecího napětí až do rail-to-rail). Pro dosažení minimalizace rozměru čipu a procesních a technologických odchylek byly inovativní techniky použity k nahrazení pasivních prvků aktivními, které jsou rovněž schopny pracovat při nízkém napájecím napětí a nízké spotřebě.

Experimentální část tohoto výzkumu zahrnuje realizaci funkčních vzorků těchto obvodů na čip s použitím dostupných technologií CMOS (0.35 μm AMIS I3T25/CMOS035). Výsledky experimentálního měření dokazují atraktivní vlastnosti těchto obvodů.

ABSTRACT

Nowadays prolonging the battery life time and miniaturizing integrated circuits are considered as basic requirements of modern portable electronics and battery-powered implantable and wearable biomedical devices. Many efforts have been exerted towards minimizing the power consumption and supply voltage of the circuits. However, analog circuit designers encounter difficulties to preserve reliable performance of the analog circuits with scaling down their supply voltage, owing to the fact that the threshold voltage of MOS transistor and supply voltage are not decreased proportionally. Hence, various novel techniques must be adopted to overcome the rather high threshold voltage problem of MOS transistors. Therefore, this work deals with research of new low-voltage low-power analog circuits design principles for battery-powered implantable and wearable biomedical devices.

Based on these innovated techniques various low-voltage low-power active elements were proposed to provide the necessary analog signal processing i.e. amplifying, filtering and rectifying of selected biological signals. The voltage supply of these circuits is pushed down to the minimum (1V to 0.5V) and the power consumption to the minimum as well (tens of μW to tens of nW) while the other circuit performances are kept attractive, such as the input dynamic range (60% of the supply voltage range up to rail-to-rail). Also, to minimize chip area and to have compensation against process and technology P/T variations, innovated techniques are used to replace the passive elements by active ones. These active elements are also capable to work under low-voltage low-power condition.

Finally the experimental part of the research includes the realization of functional samples of these structures on chip by using Cadence platform (0.35 μm AMIS I3T25/CMOS035). The experimental results prove the attractive performances of the proposed circuits.