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**Evolutionary Synthesis
of Analog Electronic Circuits
Using EDA Algorithms**

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ
ÚSTAV RADIOELEKTRONIKY

Ing. Josef Slezák

**EVOLUTIONARY SYNTHESIS OF ANALOG
ELECTRONIC CIRCUITS USING EDA ALGORITHMS**

EVOLUČNÍ SYNTÉZA
ANALOGOVÝCH ELEKTRONICKÝCH OBVODŮ
S VYUŽITÍM ALGORITMŮ EDA

Zkrácená verze Ph.D. Thesis

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1 INTRODUCTION

Although there is a trend of using digital processing in most areas of the modern electronics, analog electronic circuits are still important part of today's electronic integrated chips. There is variety of applications where using of analog circuits is advantageous compared to digital solutions or such digital solutions even do not exist.

Design of analog circuits is traditionally domain of experienced designers and usually is viewed as a kind of art where designer's intuition is important part of the design process.

With increasing performance of modern computing and advances in the area of artificial intelligence, machine learning and optimization there is possibility to take over considerable amount of the time consuming procedures required for design of analog electronics to modern computer methods called automated analog circuits design or evolutionary electronics.

Another motivation for usage of the evolutionary electronics methods is demand of synthesis of analog circuits for which no methods of classical analog design exist.

2 EVOLUTIONARY ELECTRONICS

Evolutionary electronics system is approach based on methods of local and global optimization, machine learning and artificial intelligence which is able to synthesize electronic circuits based on their desired characteristics (transfer function, input impedance, etc.).

There have been presented variety of different methods for solving automated analog circuit synthesis problem.

In [1] Harjani described tool OASYS which uses design plans to successively select topologies and translate specifications in a knowledge based synthesis framework.

The pioneer of genetic programming (GP) J. Koza employed GP in automated analog circuits synthesis system where analog electronic circuits were encoded using tree structures [2].

Another research line of the earliest works was focused on analog circuit design automation based on genetic algorithms (GA). Grimbly have published several papers focused on employing of hybrid GA and direct encoding method for synthesis of passive analog circuits [3].

Another attempt to handle analog circuit synthesis automation problem by means of GA was presented by Lohn and Colombano in [4]. The method uses simultaneous synthesis of the topology and the parameters approach. Compared to

the previous work presented by Grimbleby analog circuits are encoded using developmental encoding.

More advanced approach of synthesis of passive and also active analog circuits was proposed by Zebulum who employed GA with variable chromosome representation [5].

Mattiussi proposed method called analog genetic encoding (AGE) which is able to synthesize analog circuits and neural networks [6]. The system employs encoding method based on principles of biological chromosomes.

Das and Vemuri have proposed several methods for automated analog circuit synthesis. The first method called GAPSYS was able to synthesize only passive analog circuits [7]. In the method presented in [8] the selection of the topology is realized using adaptively generated building blocks. Evolutionary electronics synthesis method using graph grammar based approach was presented in [9].

Recently Estimation of Distribution Algorithms (EDA) [10] have shown their superior performance compared to classical genetic algorithms. Univariate Marginal Distribution Algorithm (UMDA) [11] was employed in evolutionary electronics system presented by Zinchenko [12]. Another application of UMDA in automated analog circuits synthesis system was presented by Torres in [13].

The goal of the thesis is to design and verify three types of automated analog circuits synthesis methods based on Estimation of Distribution Algorithms. Synthesis capability of every method will be verified on an example of analog circuit synthesis problem. The goals of the thesis are:

- Design and verify automated passive analog circuit synthesis method based on pure UMDA. Synthesis of the topology and determination of the parameters (values of the components) are solved using UMDA algorithm.
- Design and verify hybrid automated passive analog circuit synthesis method based on UMDA [11] and local search method. The topology of the desired circuit is synthesized using UMDA. The parameters of the desired circuit are determined using the local search method.
- Design hybrid automated active analog circuit synthesis method based on employing of Univariate Probabilistic Model. The Topology of the desired analog circuit is synthesized using EDA and the parameters of the desired circuit are determined using a local search algorithm.

3 AUTONOMOUS CIRCUITS

Analog circuit design using autonomous circuits was described in [14]. The design method can be used for synthesis of different types of analog circuits as frequency filters or oscillators.

Given number of nodes n_n autonomous circuit (AC) is defined as fully connected network where generalized admittances are connected between all possible combinations of the nodes. Generalized admittance is component with no defined type and can be replaced by any component or theirs parallel combination. Example of autonomous circuit for $n_n = 5$ (nodes 0 to 4) with 2 ports generalized admittances is presented in Fig. 3.1a.

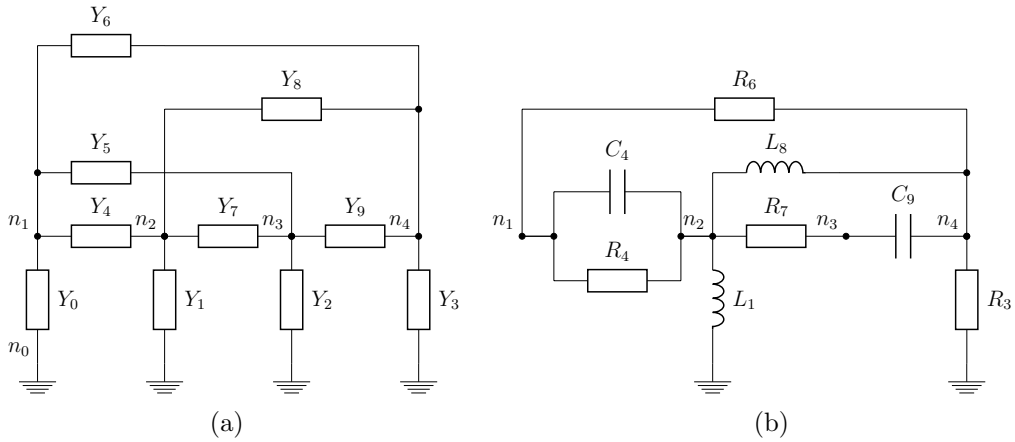


Fig. 3.1: a) Example of autonomous circuit b) Example of replacement of generalized admittances of the autonomous circuit by real components.

Design of analog circuits using autonomous circuits as was presented in [14] is briefly reviewed bellow.

In the first step generalized admittances are manually replaced by real components, their parallel combination or open circuit. The replacement is performed randomly or based on some initial requirements (all capacitors grounded). Also previous experience of the designer or intuition is incorporated in the process. An example of such replacement is presented in Fig 3.1b. As you can see the replacement is as follows: $Y_0 \rightarrow open, Y_1 \rightarrow L_1, Y_2 \rightarrow open, Y_3 \rightarrow R_3, Y_4 \rightarrow R_4 || C_4, Y_5 \rightarrow open, Y_6 \rightarrow R_6, Y_7 \rightarrow R_7, Y_8 \rightarrow L_8, Y_9 \rightarrow C_9$.

After obtaining of a new structure of analog circuit (3.1b) characteristic equation in symbolic form is obtained. For different input and output connection nodes various impedance and transfer functions can be obtained. Choosing of input and output nodes is determined by desired function of the designed analog circuit.

For selected configuration of input and output nodes and resulting impedance or transfer function values of the components are calculated.

4 ENCODING OF ANALOG CIRCUITS

Graphs are the most straightforward method of representation of the topology of analog circuits. There is direct relation between graph structures and the topology of analog circuits. Therefore graphs and hypergraphs were chosen for representation of the topology of analog circuits in the automated analog circuit synthesis methods proposed in the thesis.

Passive analog circuits are represented using multigraphs G_p which are encoded by binary characteristic vectors e_p . Every single bit of e_p corresponds to including or not including of the corresponding edge in multigraph G_p . Every edge of multigraph G_p corresponds to a single passive component of the encoded analog circuit.

Analog circuits consisting of transistors are represented using labeled 3-uniform hypergraphs G_t which are encoded by binary characteristic vectors e_t . Every single bit of e_t corresponds to including or not including of the corresponding hyperedge in hypergraph G_t . Every hyperedge of hypergraph G_t corresponds to a single transistor of the encoded analog circuit.

Since number of the components of the encoded analog circuit is determined by number of "ones" of vectors e_p and e_t using of the proposed encoding method leads to problem with unitation constraints and used EDA algorithms has to be modified to enable dealing with this type of problem.

5 EDA AND UMDA

Estimation of Distribution Algorithms (EDA) are evolutionary optimization techniques employing probabilistic models to generate new solutions.

The aim of using EDA is to avoid the use of recombination operators (mutation, crossover) in favor of explicitly modeling and exploiting the distribution of promising individuals.

The main idea of EDA is to replace recombination phase of genetic algorithms by probabilistic modeling of promising areas of solution space. The motivation for developing EDA was demand to overcome some drawbacks of genetic algorithms such as requirement of tight linkage or problems with deceptive functions.

Univariate Marginal Distribution Algorithm (UMDA) [11] is the simplest variant of EDA algorithm. The basic principle of building of the probabilistic model is to count the marginal frequencies of occurrence of the components (the univariate marginal probability) in the population of the candidate solutions. After that the computed marginal frequencies of the components are used for generation of new solutions during sampling phase of the algorithm. The probabilistic model is

constructed under assumption that the components of the solution vector are independent of each other.

As was mentioned in section 4 for the used type of encoding method the problem of automated analog circuit synthesis has to be viewed as problem with unitation constraints [15]. Therefore modified version of UMDA algorithm which is able to handle problems with unitation constraints has to be used. Modification of Factorized Distribution Algorithm (FDA) algorithm which allows to solve problems with unitation constraints was described in [15]. To enable UMDA to solve problems with unitation constrains, generation phase of UMDA was modified. After generation of new samples repairing function which ensures satisfying of unitation constrains is applied. Implementation of the repairing function was inspired by the principles presented in [15].

6 CIRCUIT SYNTHESIS USING EDA

The main principle of the proposed automated analog circuit synthesis method is to utilize manual autonomous circuits design approach as was described in section 3 in connection with Estimation of Distribution Algorithm. This way the intuition and the previous experience of the designer will be replaced by probabilistic modeling of the promising areas of the design search space and generating of high probable solutions. Using powerful computation and probabilistic modeling approach allow to explore extensive solution space of large number of different combinations of suitable topologies of analog circuits.

7 SYNTHESIS OF CHAOTIC DYNAMICS USING UMDA

The section is focused on the synthesis of the topology and the parameters of analog impedance network with desired input impedance function using the univariate marginal distribution algorithm. As a test problem design of chaotic oscillator circuit is adopted.

7.1 Definition of the Problem

The proposed realization of the chaotic oscillator consists of parallel connection of PWL resistor and admittance network.

The three-segment PWL resistor is realized by diode limiter and impedance converters [16]. Its PSpice implementation and its DC input characteristic are presented in Fig. 7.1.

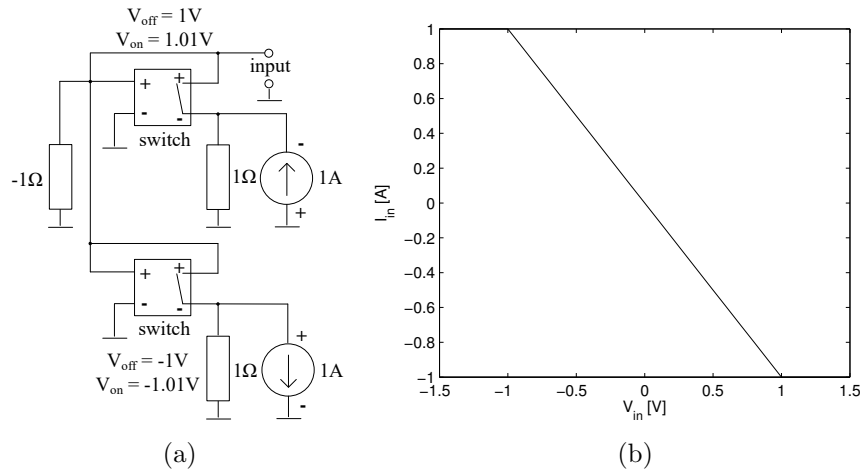


Fig. 7.1: a) Schematic of PWL resistor b) Input DC characteristic of PWL resistor.

The second part, admittance network, will be synthesized using pure UMDA algorithm as will be described in the next sections. Two sets of parameters are given (see dissertation thesis). Two corresponding input impedance functions of the admittance network are (7.1) for the first set of the parameters and (7.2) for the second set of the parameters.

$$Z_{in1} = \frac{10.6s^2 - 2.26s + 2.99}{s^3 + 10.2s^2 - 1.2s + 2.71} \quad (7.1) \quad Z_{in2} = \frac{3.2s^2 - 100.9s + 23.2}{s^3 + 2.4s^2 - 0.71s + 3.27} \quad (7.2)$$

7.2 Used Encoding And Objective Function

As a encoding method characteristic vector approach is used (section 4). Number of the nodes of used AC (section 3) was chosen $n_n = 10$. Modified UMDA (section 5) is used for the topological part of the encoding vector e (bits $b1$ to $b135$). Values of the components are represented in mantissa-exponent form where every single mantissa is encoded using 7 bits and every single exponent is encoded using 3 bits (Fig. 7.2).

$$e = [\overbrace{b1 \ b2 \ b3 \ \dots \ b135}^{\text{topology}}] [\overbrace{b136 \ b137 \ b138 \ \dots \ b180}^{\text{exponents}}] [\overbrace{b181 \ b182 \ b183 \ \dots \ b285}^{\text{mantissas}}]$$

Fig. 7.2: Schematic diagram of the used encoding vector e .

Cost value $cost$ is according to (7.3) calculated as weighted summation of the magnitude and phase differences. Difference of magnitude is calculated as weighted absolute value of differences of desired magnitude function f_{md} and magnitude of current solution f_{mc} over $m = 101$ frequency points in the range 0.001 rad/s to 10 rad/s. Similarly difference of phase is calculated as weighted absolute value of differences of desired phase function f_{pd} and phase of current solution f_{pc} . Frequency response (f_{mc} and f_{pc}) of the current solution was obtained using nodal analysis function implemented in Matlab.

$$cost = \frac{w_{cm}}{m} \sum_{i=1}^m w_{dm}(i) |f_{md}(i) - f_{mc}(i)| + \frac{w_{cp}}{m} \sum_{i=1}^m w_{dp}(i) |f_{pd}(i) - f_{pc}(i)| \quad (7.3)$$

7.3 Experiments and Solutions

Only passive RLC components were used. Values of the resistors can be also negative. Complexity of the evolved analog circuit is restricted to use AC of $n_n = 10$ nodes and 15 components ($n_c = 15$) at the most. Population size is set to 200 individuals. Number of generations per run was set to 500.

There were performed 20 runs of the proposed algorithm for each input impedance function (7.1) and (7.2). Average run time of the algorithm was 4 minutes and 27 seconds.

Schematic, magnitude and phase responses of the best solutions for input impedance functions (7.1) and (7.2) are presented in Fig. 7.3 and Fig. 7.4 respectively.

For the verification of the synthesized admittance networks the resulting structures are employed in the proposed chaotic oscillator circuit. State projections of the output signals of the oscillator for the best synthesized circuits for parameters 1 and parameters 2 (input impedance functions (7.1) and (7.2)) are presented in Fig. 7.5.

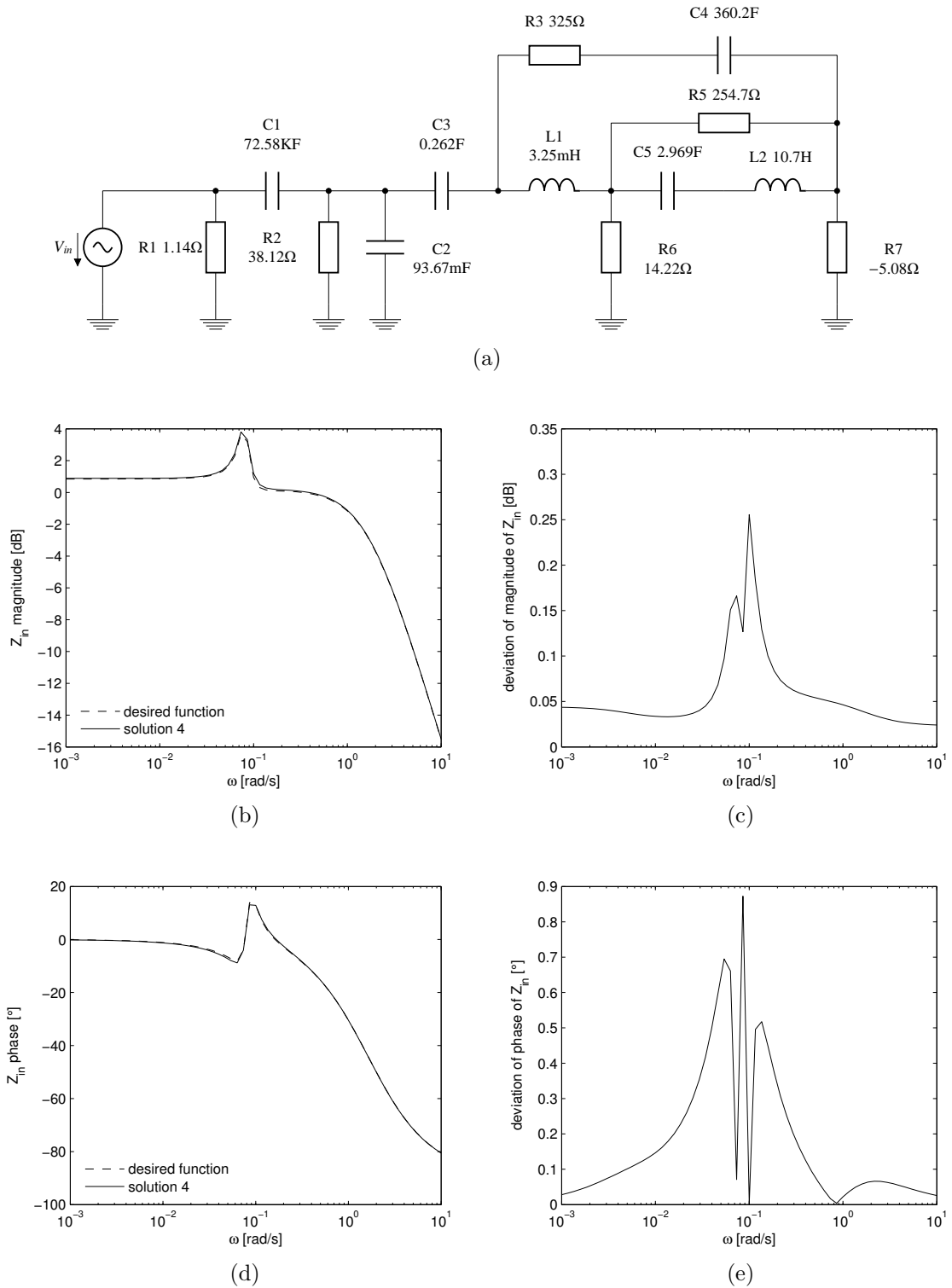
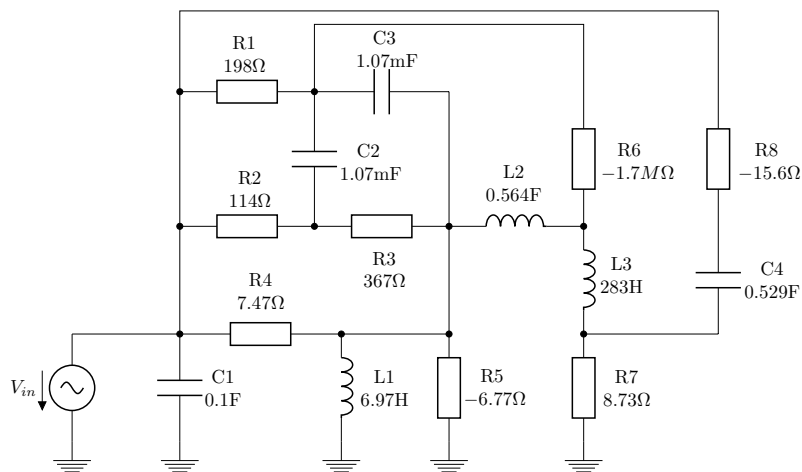
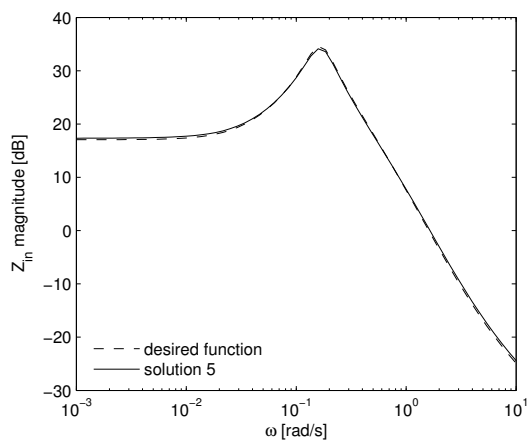


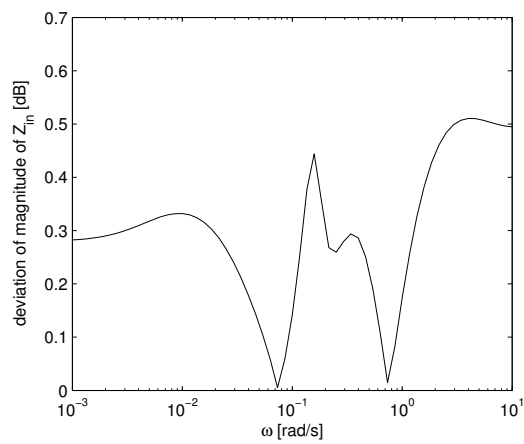
Fig. 7.3: Parameters 1 (function (7.1)): schematic of the best solution (a), magnitude of Z_{in} (b), deviation of magnitude Z_{in} and desired function (7.1)(c), phase of Z_{in} (d), deviation of phase Z_{in} and desired function (7.1)(e)



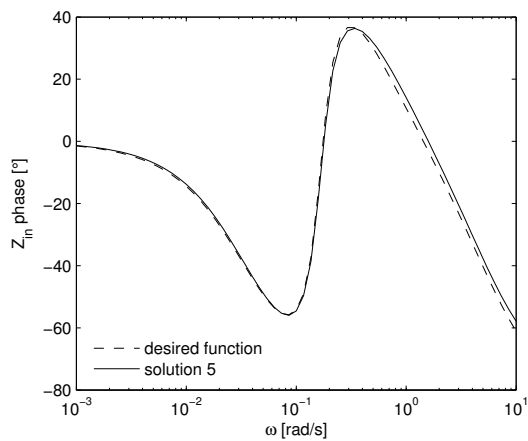
(a)



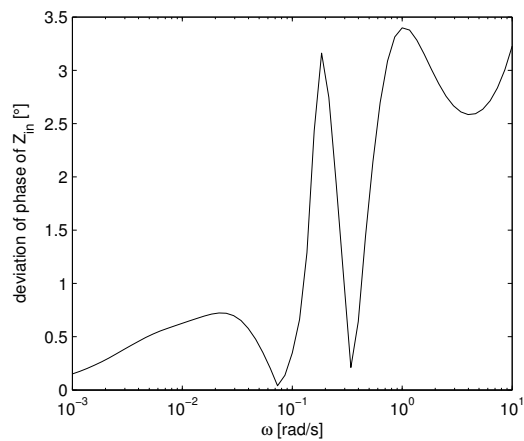
(b)



(c)



(d)



(e)

Fig. 7.4: Parameters 2 (function (7.2)): schematic of the best solution (a), magnitude of Z_{in} (b), deviation of magnitude Z_{in} and desired function (7.2)(c), phase of Z_{in} (d), deviation of phase Z_{in} and desired function (7.2)(e)

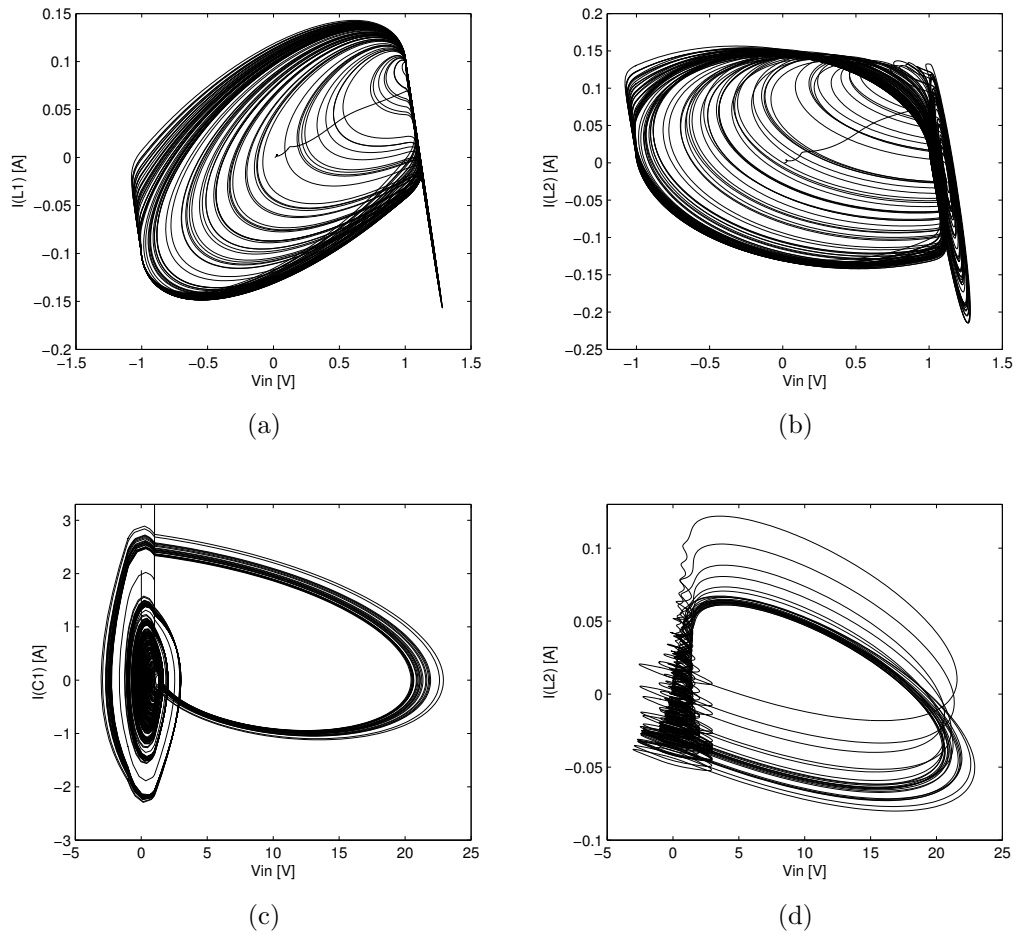


Fig. 7.5: State projections for the best solution for parameters 1: $I(L1)$ vs. V_{in} (a), $I(L2)$ vs. V_{in} (b), State projections for the best solution and parameters 2: $I(C1)$ vs. V_{in} (c), $I(L2)$ vs V_{in} (d).

7.4 Conclusion

Method of evolutionary synthesis of passive analog networks with desired input impedance characteristic using pure UMDA algorithm was presented. The UMDA algorithm was modified to enable solving problems with unitation constraints.

Compared to the approach in [12] the proposed method allows encoding of parallel connection of the components and synthesis of circuits of higher complexity.

Several analog networks for two sets of parameters were synthesized. Comparison of magnitude and phase characteristics of the synthesized circuits and desired function shows very good accuracy of the synthesized solutions. The synthesized circuits were verified in the chaos oscillator circuit and resulting state projections were presented.

8 SYNTHESIS OF FRACTIONAL CAPACITOR USING HYBRID UMDA ALGORITHM

8.1 Definition of the Problem

Authors of [17] describe approximation of fractional capacitors $(1/s)^{1/n}$ by a regular newton process and they present its RLC network representations which are obtained using classical method of analog circuit synthesis. The problem of synthesis of fractional capacitor was adopted from the mentioned paper and will be used for demonstration of the synthesis capability of the proposed method. In [17] function (8.1) was approximated using 5th order function (8.2).

$$Z_{in} = s^{-0.6} \quad (8.1)$$

$$Z_{in} = \frac{8.58s^4 + 255s^3 + 405s^2 + 35.9s + 0.169}{1s^5 + 94.2s^4 + 472s^3 + 134.8s^2 + 2.627s + 9.8 \times 10^{-3}} \quad (8.2)$$

In Fig. 8.1 there is circuit realization of function (8.1) as presented in [17]. For the rest of the section the circuit will be called original approximation circuit.

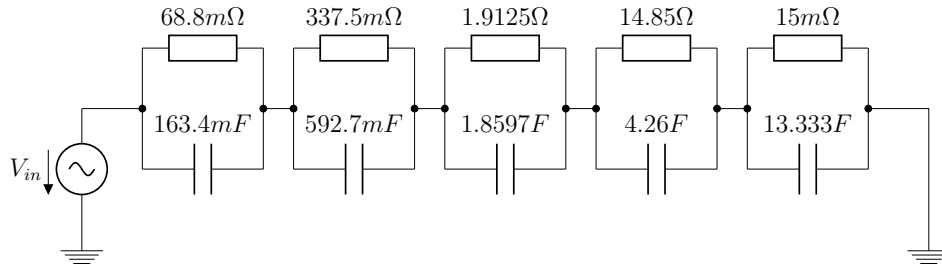


Fig. 8.1: Schematic of the original approximation circuit.

Comparison of magnitude of Z_{in} for original approximation circuit and for (8.1) is presented in Fig. 8.2a. The broken line represents function (8.1) and the solid line represents original approximation circuit. Since the deviation is not clear from the picture absolute value of difference of both curves presented in Fig. 8.2a is presented in Fig. 8.2b. Comparison of phase of Z_{in} for original approximation circuit and for (8.1) is presented in Fig. 8.2c. The absolute value of difference of both curves plotted in Fig. 8.2c is presented in Fig. 8.2d.

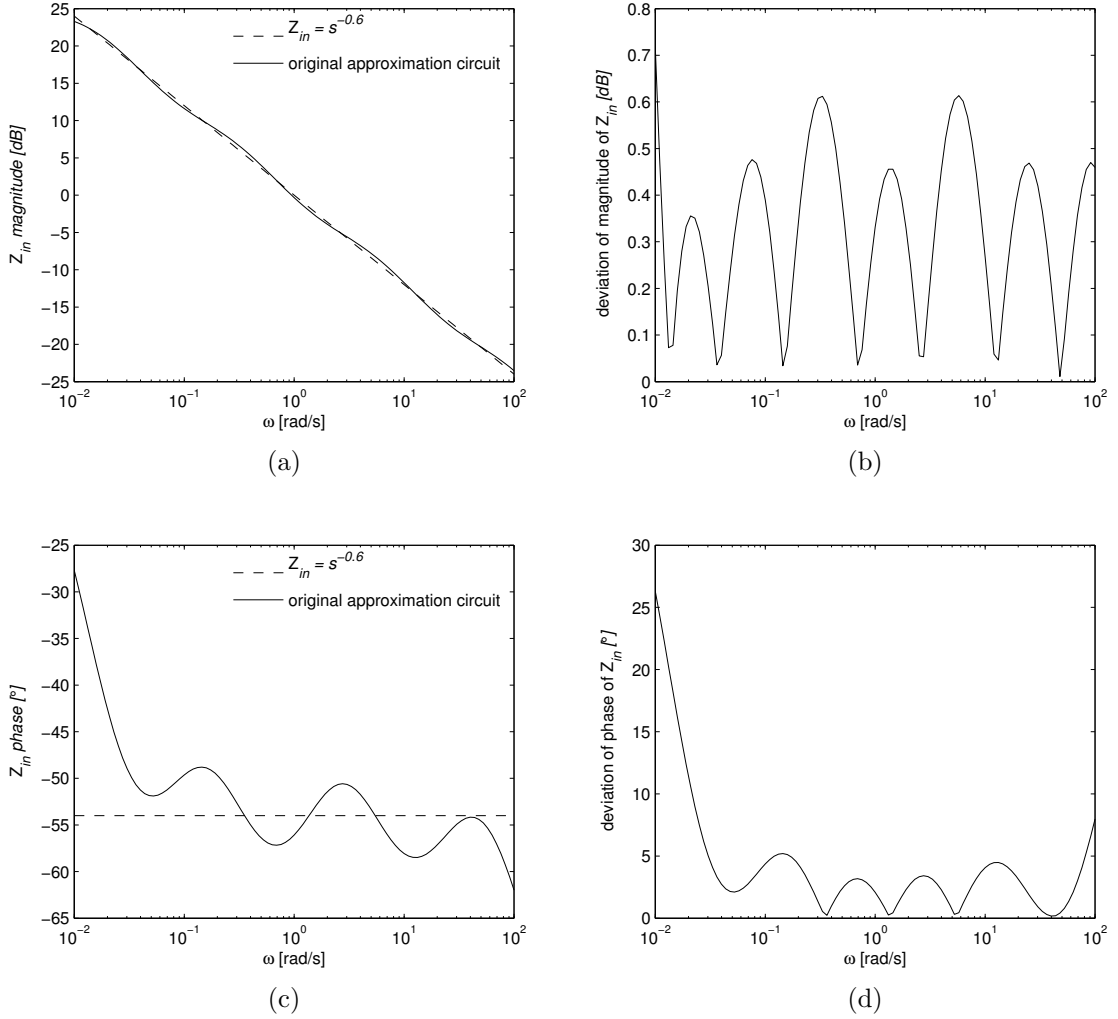


Fig. 8.2: a) Comparison of magnitude of Z_{in} for ideal function (8.1) and for original approximation circuit b) Deviation of magnitude of Z_{in} c) Comparison of phase of Z_{in} for ideal function (8.1) and for original approximation circuit d) Deviation of phase of Z_{in} .

The highest deviations of magnitude and phase of the original approximation circuit are presented in Tab. 8.1.

Magnitude				Phase			
ω [rad/s]	0.01	100	0.3311	ω [rad/s]	0.01	100	0.14
Δ_m [dB]	0.71	0.46	0.61	Δ_p [°]	26.3	7.98	5.2

Tab. 8.1: The highest deviations of magnitude and phase of the original approximation circuit.

The following sections will be focused on synthesis of the presented fractional capacitor circuit using hybrid UMDA algorithm.

8.2 Hybrid UMDA Algorithm

The proposed method is based on combination of UMDA and a local search algorithm. Its pseudo code is presented in Fig. 8.3.

- step0:** Initialization of population P .
- step1:** Select population S .
- step2:** Build probabilistic model M of selected population S .
- step3:** Using probabilistic model M generate new samples G .
- step4:** Evaluate cost of samples G and execute local search algorithm.
- step5:** Based on P and G create new population P_{new} and replace old population ($P := P_{new}$). If termination criteria not met go to **step1**.

Fig. 8.3: Pseudo code of the proposed method.

Population P is formed of binary vectors of length 135 bits which are initialized randomly with seeding of 10 bits ($n_c = 10$). Parameters storage e_{ps} is formed of vector of length 135 consisting of real numbers in the range $\langle 0,1 \rangle$. Parameters storage vector e_{ps} is dynamically optimized during the whole synthesis process and it is adapted to selected topologies in the selection phase of the algorithm. The vector includes a component value for every single admittance of used AC. During initialization phase e_{ps} is set randomly with uniform distribution.

In the next step good individuals are selected using truncation selection method and selected population S is created.

Probabilistic model M of selected population S is built. The goal of the learning process is to capture the features of the good individuals of selected population S .

Probabilistic model M is used for generation of new samples of solutions G . New samples are generated and unitation constraints repaired function (section 5) is applied.

Cost values of the generated samples are evaluated using the topological information stored in N and using the parameters stored in e_{ps} . If the condition of execution of the local search algorithm is fulfilled, the local search algorithm tries to optimize the parameters of the current solution. If accuracy of the current solution is improved then parameters storage e_{ps} is updated according to the results of the local search algorithm.

In the last step new population P is formed of the best individuals of G and selected population S . Described process is repeated until some of the termination criteria of the algorithm is met.

8.3 Encoding Method And Objective Function

As a encoding method characteristic vector approach (section 4) is used. Number of the nodes of used AC (section 3) was chosen $n_n = 10$.

Schematic of the used encoding vector e is presented in Fig. 8.4. The topology is encoded using set of binary variables $TOP = \{b1, b2, b3, \dots, b135\}$ and the parameters (values of the components) are encoded using set of real numbers $PAR = \{dbl1, dbl2, db3, \dots, dbl10\}$.

$$e = \left[\begin{array}{c} \text{topology} \\ b1 \ b2 \ b3 \ \dots \ b135 \end{array} \right] \left[\begin{array}{c} \text{parameters} \\ dbl1 \ dbl2 \ dbl3 \ \dots \ dbl10 \end{array} \right]$$

Fig. 8.4: Schematic diagram of the encoding vector e .

Based on the admittances selected in the topological part of the information (set TOP) corresponding parameters values are loaded from parameters storage e_{ps} and copied to the parameters part of the encoding vector e (set PAR).

According to (8.3) cost value $cost$ is calculated as weighted summation of the magnitude and phase differences. Difference of magnitude is calculated as weighted absolute value of differences of desired magnitude function f_{md} and magnitude of current solution f_{mc} over $m = 101$ frequency points in the range 0.01 rad/s to 100 rad/s. Similarly difference of phase is calculated as weighted absolute value of differences of desired phase function f_{pd} and phase of current solution f_{pc} . Frequency response (f_{mc} and f_{pc}) of the current solution was obtained using nodal analysis function implemented in Matlab.

$$cost = \frac{w_{cm}}{m} \sum_{i=1}^m w_{dm}(i) |f_{md}(i) - f_{mc}(i)| + \frac{w_{cp}}{m} \sum_{i=1}^m w_{dp}(i) |f_{pd}(i) - f_{pc}(i)| \quad (8.3)$$

8.4 Experiments and Solutions

To allow direct comparison of the original approximation circuit presented in [17] and approximation circuits obtained using the proposed method maximal number of the components of the synthesized circuits was set $n_c = 10$.

The synthesis method is configured to use only passive components resistors, capacitors and inductors. Population size was set $PopSize = 200$, number of generations was set $MaxGen = 200$.

There were executed 20 instances of the proposed algorithm. Average running time of a single execution was 11 min. Schematic of the best solution and its magnitude and phase characteristics are presented in Fig. 8.5.

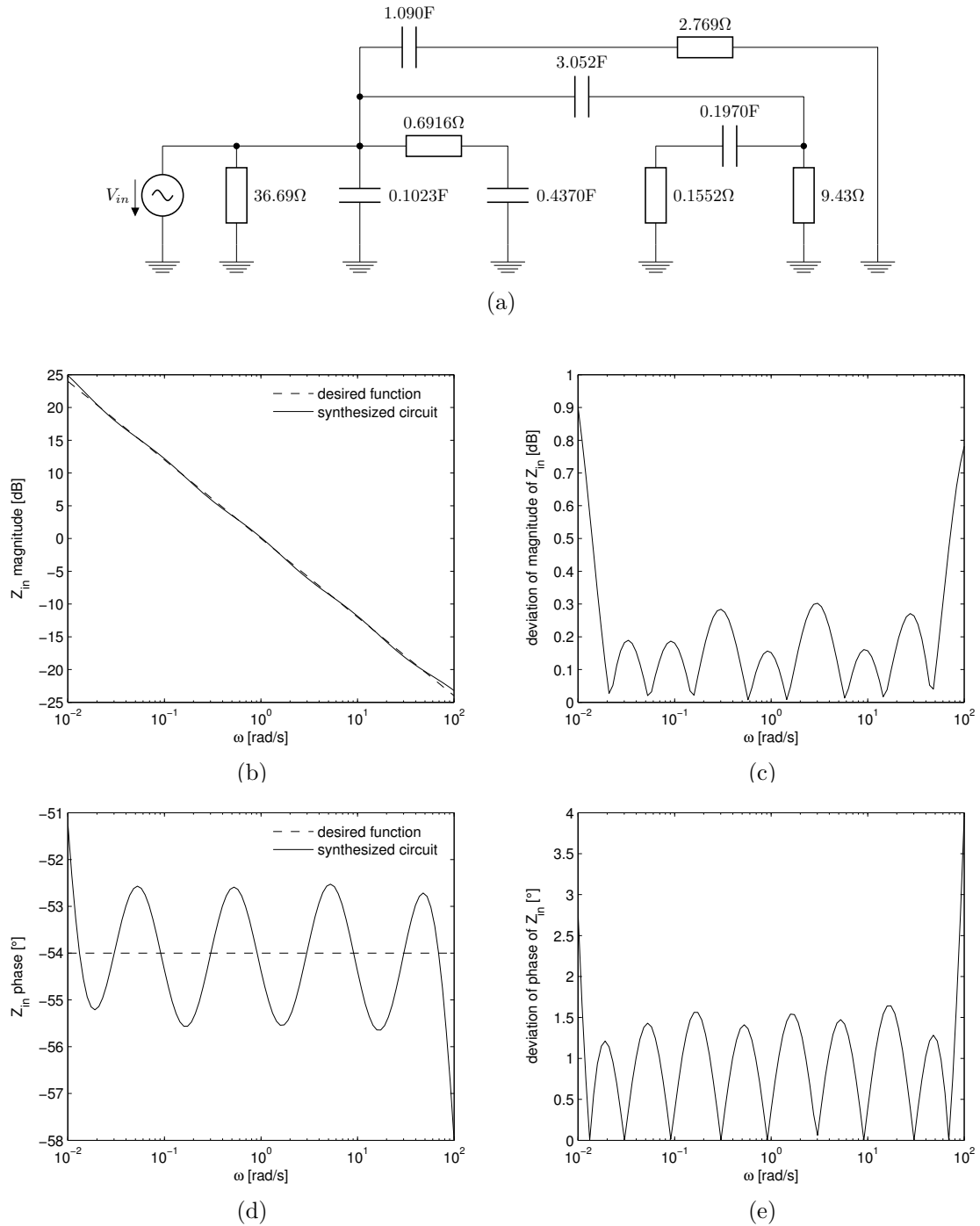


Fig. 8.5: a) Schematic of the best found solution b) Comparison of magnitude of Z_{in} of the best circuit and (8.1) c) Deviation of magnitude of Z_{in} of the best circuit d) Comparison of phase of Z_{in} of the best circuit and (8.1) e) Deviation of phase of Z_{in} of the best circuit.

Comparison of magnitude and phase deviations of the original approximation circuit and the best synthesized solution is presented in Tab. 8.2.

Magnitude					Phase				
original	$\omega[rad/s]$	0.01	100	0.33	original	$\omega[rad/s]$	0.01	100	0.14
circuit	$\Delta_m[dB]$	0.71	0.46	0.61	circuit	$\Delta_p[^\circ]$	26.3	7.98	5.2
synthesized	$\omega[rad/s]$	0.01	100	0.30	synthesized	$\omega[rad/s]$	0.01	100	0.58
circuit	$\Delta_m[dB]$	0.93	0.92	0.27	circuit	$\Delta_p[^\circ]$	3.0	4.2	1.5

Tab. 8.2: Comparison of the highest magnitude and phase deviations of the original approximation circuit and the best synthesized circuit.

Inside of the used frequency range the highest deviations of magnitude of original approximation circuit and the best synthesized circuits were $\Delta_m = 0.61\text{db}$ and $\Delta_m = 0.27$ respectively.

Highest deviations of phase of original approximation circuit and the best synthesized circuits were $\Delta_p = 5.2^\circ$ and $\Delta_p = 1.5^\circ$ respectively.

8.5 Conclusion

Automated analog circuits synthesis method based on hybrid approach employing UMDA and local search algorithm was presented. Used hybrid approach enables to employ specialized methods for both sub problems of different nature (synthesis of the topology and determination of the parameters). Synthesis of the topology which is combinational optimization problem was solved using UMDA. Synthesis of the parameters which is continuous optimization problem was solved using local search algorithm. The principle of the method is based on mutual interaction of synthesis of the topology (UMDA) and determination of the parameters (local search algorithm) of the desired solution. Note that modified version of UMDA which allows to solve problems with uniteration constrains was used.

The proposed method was verified on the problem of synthesis of fractional capacitor circuit introduced in [17]. Presented experiments have shown that the proposed algorithm is capable to synthesize solutions whose accuracy overperform solutions obtained using classical method of analog circuit design given in [17]. Accuracy of magnitude of the best obtained solution was more than twice better then the original approximation circuit. Accuracy of phase of the best obtained solution was more than three times better then the original approximation circuit.

9 SYNTHESIS OF CUBE ROOT FUNCTION USING GRAPH EDA METHOD

9.1 Definition of the Problem

The problem of synthesis of circuit realization of cube root function was introduced by John Koza in [18]. The target voltage response of the desired circuit is (9.1).

$$U_2 = \sqrt[3]{U_1} \quad (9.1)$$

9.2 Graph Estimation of Distribution Algorithm

Synthesis capability of the proposed GhEDA method will be demonstrated on the problem of circuit realization of cube root function which consists of bipolar transistors NPN and PNP, resistors and positive and negative voltage sources. The goal of the synthesis is to design topology of connection of the transistors NPN and PNP, topology of connection of the resistors, the parameters of the resistors (the values of the resistors) and define nodes of connection of the positive and the negative voltage sources. Pseudo-code of the proposed method is presented in Fig. 9.1.

- step0:** Initialize population P of m individuals.
- step1:** According to selection method select population S .
- step2:** Build probabilistic model M of selected population S .
- step3:** Based on probabilistic model M generate set of new samples G consisting of d individuals.
- step4:** Using objective function evaluate cost values of set of newly generated samples G .
- step5:** Based on P and G create new population P_{new} and replace old population ($P := P_{new}$).
- step6:** According to topologies of n_{opt} randomly selected individuals of P optimize values of parameters storage e_{ps} . If termination criteria not met go to **step1**.

Fig. 9.1: Pseudo-code of the proposed method.

Initial population P consisting of m individuals is set randomly respecting maximal number of components of every type n_{nnpn} , n_{pnp} , n_{res} , n_{vccp} and n_{vccn} . Parameters storage e_{ps} is initialized randomly with uniform distribution. Variables n_{vccp}

and n_{vccp} denote maximal numbers of the nodes of the encoded circuit connected to the positive and negative voltage sources.

After evaluation of cost values of population P , selected population S is formed. Tournament selection method with tournament size 2 is used.

In the learning phase probabilistic model M of selected population S is created. Marginal frequencies of the components included in selected population S are calculated. Every single component connected to specific connection nodes is represented by corresponding edge of graph (resistors and positive and negative voltage sources) or hyperedge of hypergraph (transistors NPN and PNP). Therefore marginal frequencies of the components correspond to the marginal frequencies of the edges of graphs and the hyperedges of hypergraphs encoded in the individuals of selected population S .

In the next phase probabilistic model M is used to generate population of new samples of solutions G which consists of d individuals.

New individuals are simulated and their cost values are calculated using objective function presented below.

In the replacement phase new population P_{new} is formed of best $m - d$ individuals of current population P and whole population of new samples G . Afterwards current population P is replaced by new population P_{new} ($P := P_{new}$).

In the optimization phase the local search algorithm tries to improve (decrease) cost values of n_{opt} randomly selected individuals of population P .

9.3 Encoding Method And Objective Function

Every individual of population P includes information about the topology of connection of the resistors (multigraph G_{res}), topology of connection of the NPN transistors (3-uniform hypergraph G_{nnp}), topology of connection of the transistors PNP (3-uniform hypergraph G_{pnp}), connection of the positive voltage sources (graph G_{vccp}) and connection of the negative voltage sources (graph G_{vccn}). These graphs and hypergraph are encoded by characteristic vectors e_{res} , e_{nnp} , e_{pnp} , e_{vccp} and e_{vccn} respectively.

To enable direct comparison of the results obtained using the proposed method and the results of other authors the objective function is defined exactly the same way as was presented in original paper [18].

$$cost = \sum_{i=1}^m w_v(i) |f_{vd}(i) - f_{vc}(i)| \quad (9.2)$$

According to (9.2) cost value $cost$ is defined as weighted summation of absolute values of differences between voltage response of desired solution f_{vd} and voltage response of current solution f_{vc} over $m = 21$ equidistant voltage values in the range -250 mV to 250mV. There is penalization of the cost value by 10 if the output voltage response is not within 1% deviation of the target voltage characteristic. In such case weight w_v is set to 10, otherwise $w_v = 1$. Voltage response of the current solution is obtained using circuit simulator ngspice.

9.4 Experiments and Solutions

Population size was set to 400 individuals. Number of generations per single run of the algorithm was set to 3000. Maximal number of the nodes of the desired circuit was set to 17. There were performed 20 runs of the proposed algorithm. Average run time of a single run was 14 hours. Average time of single evaluation of the objective function was 0.0336 second.

Comparison of the output characteristics of the best synthesized solution and desired function (9.1) is presented in Fig. 9.2.

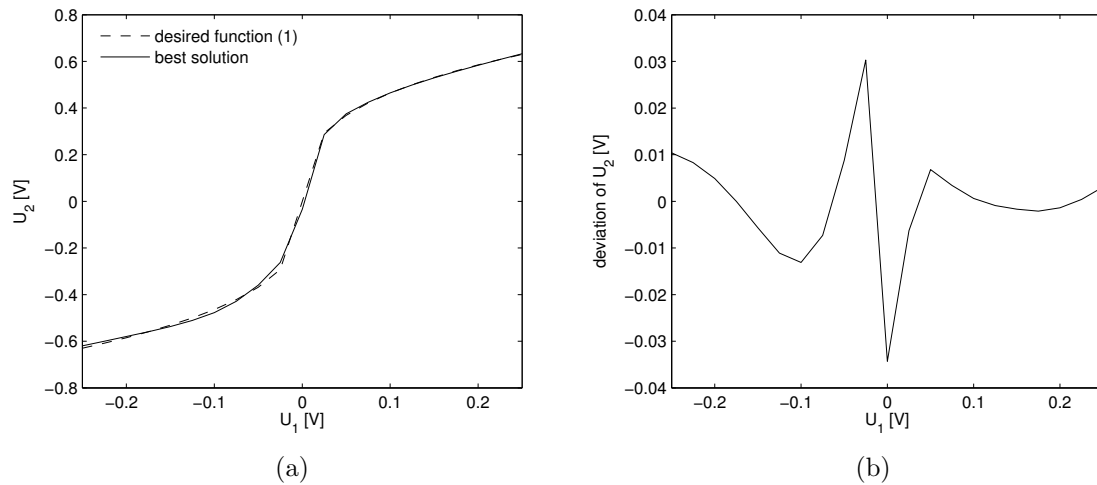


Fig. 9.2: a) Comparison of output voltage characteristic $U_2 = f(U_1)$ of the best synthesized circuit and desired function (9.1) b) deviation of output voltage characteristic $U_2 = f(U_1)$ of the best synthesized circuit and function (9.1).

As was stated above the problem of circuit realization of cube root function was introduced by Koza et al. in [18] where Genetic Programming (GP) was used. The problem was also solved using unconstrained genetic algorithm with oscillating length representation (GA OLG) by Sapargaliyev et al. in [19]. Comparison of the

best solutions of both authors and the best solution of the proposed method GhEDA is presented in Table 9.1.

method	best cost	objective function evaluations
GP (Koza et al. in [18])	1.68	37e6
GA OLG (Sapargaliyev et al. in [19])	2.27	4e6
GhEDA	1.44	1.5e6

Tab. 9.1: Comparison of the solutions of proposed method GhEDA to GP and GA OLG.

As can be seen in Table 9.1 proposed method GhEDA overperforms other two methods in terms of accuracy of the solution and number of required objective function evaluations as well.

9.5 Conclusion

There was presented graph based hybrid estimation of distribution algorithm (GhEDA) whose synthesis capability was demonstrated on the problem of circuit realization of cube root function. Results of the proposed method were compared to results of Koza et al. (GP) [18] and Sapargaliyev et al. (GA OLG) [19] who adopted the same problem of synthesis of analog circuit realization of cube root function. Experiments have shown that in terms of accuracy of the solution and number of required objective function evaluations the proposed method overperforms both other methods.

The proposed method employs simple univariate probabilistic model based on the assumption that there are no dependencies between variables of the solution vector. Although the experiments have shown that the used probabilistic model was suitable for the proposed method this model could be replaced by more advanced multivariate probabilistic model which is capable to capture higher order dependencies between the variables of the solution vector. This could be interesting and promising area of another research. Since some multivariate models can incorporate some portion of previous knowledge (prior) another interesting area of the research could be usage of different priors based on the target application of the synthesized circuit.

Since the proposed method is population based evolutionary algorithm, multi-objective approach as pareto ranking can be incorporated into the method. Also parallel computation of the cost values of the individuals of the population can be applied.

10 SUMMARY AND FUTURE DIRECTIONS

Three different methods of automated analog circuit synthesis based on EDA algorithms were proposed, described and verified. The two tasks of analog circuit synthesis problem - synthesis of the topology and determination of the parameters can be solved separately or simultaneously. While synthesis of the topology is combinational optimization problem determination of the parameters is continuous optimization problem in nature.

Simultaneous solving of the problem brings a demand of careful design of the encoding method which allows to combine different requirements of both parts of the problem (synthesis of the topology and determination of the parameters).

The first proposed method employs simultaneous solving of the problem. To enable UMDA to solve analog circuit synthesis problem continuous part of the problem (parameters of the components) is discretized. Another possibility is employing of probabilistic models of mixed type as Bayesian networks for variables of mixed discrete/continuous type. Probabilistic model for variables of mixed type was used in algorithm MBOA however experimentation with using MBOA for problems of analog circuit synthesis has not brought satisfactory results. However there are some other possibilities of solving problems of mixed discrete/continuous type (mixtures of distributions, clustering, heterogeneous factorized models (some factors are continuous and some are discrete)). This is one of the areas of possible future research.

The second approach to the automated analog circuit synthesis - separate solving of the topology and the parameters was used in the last two proposed methods. In the first step the candidate topology is chosen using EDA method. In the second step the parameters (the values of the components) of the selected topology were determined using local optimization algorithm. Strong advantage of the separate solving is that this approach allows to use completely different and independent methods for the topology selection and for the parameters determination. From the viewpoint of easy implementation and variability the separate solving approach is advantageous compared to the simultaneous solving.

Another interesting area of the possible future research is utilization of multivariate probabilistic models which are capable to capture higher order dependencies between the variables of the solution vectors.

Some of the probabilistic models allow to incorporate some portion of previous knowledge about the problem (priors). Experiments in the area of utilization of different prior informations based on the type of the target application of the analog circuit can be another interesting area of another future research.

REFERENCES

- [1] HARJANI, R. OASYS: a framework for analog circuit synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 1989, vol. 8, no. 12, pp. 1247-1266. ISSN 0278-0070.
- [2] KOZA, J. R., BENETT III, F. H., ANDRE, D., KEANE, M. A. Automated WYSIWYG Design of both the topology and component values of electrical circuits using genetic programming. *In Proceedings of the First Annual Conference on Genetic Programming*, 1996, pp. 123-131.
- [3] GRIMBLEBY, J. B. Automatic analogue network synthesis using genetic algorithms. *In Proceeding of First International Conference on Genetic Algorithms in Engineering Systems: Innovations and Applications (GALESIA)*, Sheffield, 1995, pp. 5358.
- [4] LOHN, J. D., COLOMBANO, S. P. A circuit representation technique for automated circuit design. *IEEE Transactions on Evolutionary Computation*, 1999, vol. 3, no. 3, pp. 205-219.
- [5] ZEBULUM, R. S., PACHECO, M. A., VELLASCO, M. M. *Evolutionary Electronics: Automatic Design of Electronic Circuits and Systems by Genetic Algorithms*, Florida: CRC Press, 2001, ISBN 0-8493-0865-8.
- [6] MATTIUSI, C., FLOREANO, D. Analog Genetic Encoding for the Evolution of Circuits and Networks, *IEEE Transactions on Evolutionary Computation*, 2007, Vol. 11, No. 5, pp. 596-607.
- [7] DAS, A., VEMURI, R. GAPSYS: A GA-Based tool for automated passive analog circuit synthesis. *in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2007, pp. 2702-2705.
- [8] DAS, A., VEMURI, R. Topology synthesis of analog circuits based on adaptively generated building blocks. *in Proc. of IEEE/ACM Design Automation Conference (DAC)*, CA: Anaheim, 2008, pp. 44-49, ISBN 978-1-60558-115-6.
- [9] DAS, A., VEMURI, R. A Graph Grammar Based Approach to Automated Multi-Objective Analog Circuit Design. *In Proc. of Design, Automation, and Test in Europe (DATE)*, France: Nice, 2009, pp. 700-705, ISBN 978-1-4244-3781-8 .
- [10] LARRAÑAGA, P., LOZANO, J. *Estimation of Distribution Algorithms: A New Tool for Evolutionary Computation*, Kluwer Academic Publishers, 2002.
- [11] MÜHLENBEIN, H., PAAß, G. From Recombination of Genes to the Estimation of Distributions I. Binary Parameters, *In Lecture Notes in Computer Science 1411: Parallel Problem Solving from Nature - PPSN IV*, pp. 178-187.
- [12] ZINCHENKO, L., MÜHLENBEIN, H., KUREICHIK, V., MAHNING, T. Application of the univariate marginal distribution algorithm to analog circuit design. *Proceedings of NASA/DoD Conference on Evolvable Hardware*, 2002, pp. 93-101.

- [13] TORRES, A., PONCE, E. E., TORRES, M. D., DIAZ, E., PADILLA, F. Comparison of Two Evolvable Systems in the Automated Analog Circuit Synthesis. *Eighth Mexican International Conference on Artificial Intelligence (MICAI 2009)*, Guanajuato, 2009, pp. 3-8, ISBN 978-0-7695-3933-1.
- [14] KOTON, J., VRBA, K. Method for Designing Frequency Filters using Universal Current Conveyors. *International Transactions on Computer Science and Engineering*, 2005, Vol. 13, No. 1, pp. 144-154.
- [15] SANTANA, R., OCHOA, A., SOTO, M. R. Factorized Distribution Algorithms for functions with unitation constraints. *In Proceedings of the Third Symposium on Adaptive Systems (ISAS-2001)*, 2001, pp. 158-165.
- [16] TOH, M. Synthesis of electronic circuits for simulating nonlinear dynamics. *International Journal of Bifurcation and Chaos*, 2001, vol. 11, no. 3, pp. 605653.
- [17] CARLSON, G. E., HALIJAK, C. A. Approximation of Fractional Capacitors $(1/s)^{1/n}$ by a Regular Newton Process. *IEEE Trans. On Circuit Theory*, 1964, Vol. 11, No. 2, pp. 210-213, ISSN 0018-9324.
- [18] KOZA, J. R., BENNETT, F. H., FORREST, H., LOHN, J., DUNLAP, F., ANDRE, D., KEANE, M. A. Automated synthesis of computational circuits using genetic programming. *In: IEEE conference on evolutionary computation*, IN: Indianapolis, 1997, pp. 447452, ISBN 0-7803-3949-5.
- [19] SAPARGALIYEV, Y., KALGANOVA, T. Unconstrained Evolution of Analogue Computational QR Circuit with Oscillating Length Representation. *In proceeding of: Evolvable Systems: From Biology to Hardware ICES 2008*, Czech Republic: Prague, 2008, pp. 1-10.

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SLEZÁK, J., PETRŽELA, J., ŠOTNER, R. On the derivation of Piecewise-Linear Chaotic Oscillators using Simulated Annealing Method and Hspice. *Przeglad Elektrotechniczny*, 2011, vol. 87, no. 1, pp. 262-265, ISSN 0033-2097.

SLEZÁK, J., ŠOTNER, R. Circuit synthesis using admittance network modification in MATLAB. In *Proceedings of Conference on Mixed Design of Integrated Circuits and Systems (MIXDES'09)*, Poland: Lodz, 2009, pp. 613-617, ISBN 978-1-4244-4798-5.

SLEZÁK, J., PETRŽELA, J., ŠOTNER, R. Designing of arc oscillator using CFA amplifier. In *Proceedings of 17th International Electrotechnical Conference*, Slovenija: Portorož, 2008, pp. 47-50, ISBN 1-58145-720-0.

ABSTRAKT

Disertační práce je zameřena na návrh analogových elektronických obvodů pomocí algoritmů s pravděpodobnostními modely (algoritmy EDA). Prezentované metody jsou na základě požadovaných charakteristik cílových obvodů schopny navrhnout jak parametry použitých komponent tak také jejich topologii zapojení. Tři různé metody využití EDA algoritmů jsou navrženy a otestovány na příkladech skutečných problémů z oblasti návrhu analogových elektronických obvodů.

První metoda je určena pro návrh pasivních analogových obvodů a využívá algoritmus UMDA pro návrh jak topologie zapojení tak také hodnot parametrů použitých komponent. Metoda je použita pro návrh admitanční sítě s požadovanou vstupní impedancí pro účely chaotického oscilátoru.

Druhá metoda je také určena pro návrh pasivních analogových obvodů a využívá hybridní přístup - UMDA pro návrh topologie a metodu lokální optimalizace pro návrh parametrů komponent.

Třetí metoda umožňuje návrh analogových obvodů obsahujících také tranzistory. Metoda využívá hybridní přístup - EDA algoritmus pro syntézu topologie a metoda lokální optimalizace pro určení parametrů použitých komponent. Informace o topologii je v jednotlivých jedincích populace vyjádřena pomocí grafů a hypergrafů.

ABSTRACT

Dissertation thesis is focused on design of analog electronic circuits using Estimation of Distribution Algorithms (EDA). Based on the desired characteristics of the target circuits the proposed methods are able to design the parameters of the used components and their topology of connection as well. Three different methods employing EDA algorithms are proposed and verified on examples of real problems from the area of analog circuits design.

The first method is capable to design passive analog circuits. The method employs UMDA algorithm which is used for determination of the parameters of the used components and synthesis of the topology of their connection as well. The method is verified on the problem of design of admittance network with desired input impedance function which is used as a part of chaotic oscillator circuit.

The second method is also capable to design passive analog circuits. The method employs hybrid approach - UMDA for synthesis of the topology and local optimization method for determination of the parameters of the components.

The third method is capable to design analog circuits which include also active components such as transistors. Hybrid approach is used. The topology is synthesized using EDA algorithm and the parameters are determined using a local optimization method. In the individuals of the population information about the topology is represented using graphs and hypergraphs.