VĚDECKÉ SPISY VYSOKÉHO UČENÍ TECHNICKÉHO V BRNĚ

Edice PhD Thesis, sv. 893

ISSN 1213-4198

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High-Voltage Structures for Galvanic Isolation in Integrated Circuits

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DEPARTMENT OF MICROELECTRONICS

HIGH-VOLTAGE STRUCTURES FOR GALVANIC ISOLATION IN INTEGRATED CIRCUITS

VYSOKONAPĚŤOVÉ STRUKTURY PRO GALVANICKOU IZIOLACI V INTEGROVANÝCH OBVODECH

ABRIDGED DOCTORAL THESIS

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DATE OF DEFENSE	14. 7. 2020

Brno 2020

Keywords:
Integrated circuit, high voltage, switch mode power supply, galvanic isolation, very large scale integration, high voltage translator, level shifter.

Klíčová slova:
Integrovaný obvod, vysoké napětí, spínaný zdroj napájení, galvanické oddělení, vysokonapěťový posunovač úrovně.

Archived in
Department of Science and International Relations
Faculty of Electrical Engineering and Communication
Technická 3058/10, 616 00 Brno

ISBN 978-80-214-5887-1
ISSN 1213-4198

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1 SIGNIFICANCE AND MOTIVATIONS OF THE THESIS

1) Design of 800 V Galvanically Isolated Translator

The first aim of this Thesis is to develop a design of galvanic isolation which can be incorporated in HV applications that require either measuring high voltages or communicating between different voltage domains. In order to simplify the evaluation of the galvanic isolator, the development is divided into two consecutive steps:

- Design of galvanically isolated translator.
- Design of galvanically isolated HB driver for industrial applications.

The design of the galvanically isolated translator must be both cost-effective and easy to apply for follow-up development of fully galvanically isolated half-bridge drivers. The design is divided into three basic blocks:

- Transmission line,
- transmitter,
- receiver.

Transmission Line
The aim of this work is to introduce a novel design of a galvanically isolated translator using adjacently coupled resonators instead of the typical vertical transformer or a high voltage capacitor. In order to achieve low signal attenuation, all transmission line components, such as the adjacently coupled resonators, need to be tuned precisely to the same resonant frequency. In order to evaluate the signal attenuation, extra test structures must be designed:

- Capacitor value skews of the coupled resonators.
- Reduced transmission line with one coupled resonator removed.
- Transmitter generating pulse bursts.
- Transmitter generating continuous signal.
- Receiver outputting digital signal.
- Receiver outputting analog signal corresponding to received signal strength.

As a plus, as soon as the translator is tuned, it can be re-used in various designs with no changes.

Transmitter
The resonant frequency of the transmission line LC components is in the order of Gigaherz. The aim is to connect the transmitter oscillator directly to the first coupled resonator of the transmission line, thereby avoiding the need of using extra on-chip inductors.

Receiver
The low current consumption requirement disqualifies the commonly used low noise amplifier (LNA) from this application. Another design of an RF detector needs to be introduced.

Communication through the Galvanically Isolated Translator
The galvanically isolated domains need to communicate with each other via the means of digital signals. For that purpose, an AC carrier technique relying on modulation and demodulation needs to be used. Therefore, two blocks providing the communication must be designed:

- Modulator: In a modulator, the amplified input voltage modulates the carrier which passes the band-pass galvanic isolator.
- Demodulator: The carrier is demodulated after it passes the isolator. The modulation is filtered out and further amplified.

The important aspect here is current consumption and the resulting power loss of the system.

Physical embodiment of galvanic isolation and the design of both the modulator and the demodulator are the objectives of this work. To send and receive signals at frequencies in the order of GHz while keeping a very low level of transmitted energy, communication on discrete basis must be employed.

Design of Galvanically Isolated Half Bridge Driver for Industrial Applications
A multi-die approach has been chosen as the most suitable solution. Two parts of the half bridge driver must be designed:

- Low voltage die employing the transmitter,
- high voltage die employing the receiver.

For the very first experiment, only a one-way direction – from a low to a high voltage signaling – is intended.

2) Design of GI Translator for HV Applications Complying with the Safety Standards

In order to achieve as high galvanic isolation level as possible, as its second goal, this Thesis aims to introduce the design of a galvanically isolated translator utilizing two vertical transformers connected in series. In order to evaluate this concept, two structures are intended to be designed:

- Bidirectional digital galvanic isolator,
- analog galvanic isolator.

The aim of the bidirectional digital isolator is to investigate the possibility of using only one galvanic isolator for communication in both, low-to-high and high-to-low, directions.

The motivation to the analog isolator design is to enable full integration of primary and secondary side controllers in one single package.

2 DESIGN OF 800 V GALVANICALLY ISOLATED TRANSLATOR

2.1 Galvanically Isolated Translator

The galvanically isolated translator utilizes lateral resonant coupling instead of stacked (vertical) coupling for CMOS galvanic isolators. The oxide thickness between the two inductors is not limited by the ONC25BCD technology IMD thickness, but is instead determined by the horizontal spacing of the inductors determined by the layout. Although lateral coupling has been used in transmission line power couplers and RF power amplifier combiners, to the best of the author's knowledge, this case of CMOS lateral resonant coupling being utilized and investigated in chip-to-chip communication is yet unprecedented [1], [2].

The fundamental concept has been prototyped as an integrated die-to-die system as shown in Fig. 2.1. The system includes two chips interconnected through two bond wires. The transmitter chip (Low Side Chip) is the low voltage die which may be integrated together with a controller. The receiver chip (High Side Chip) can be integrated with high voltage gate drivers and is immune to high voltage transients.

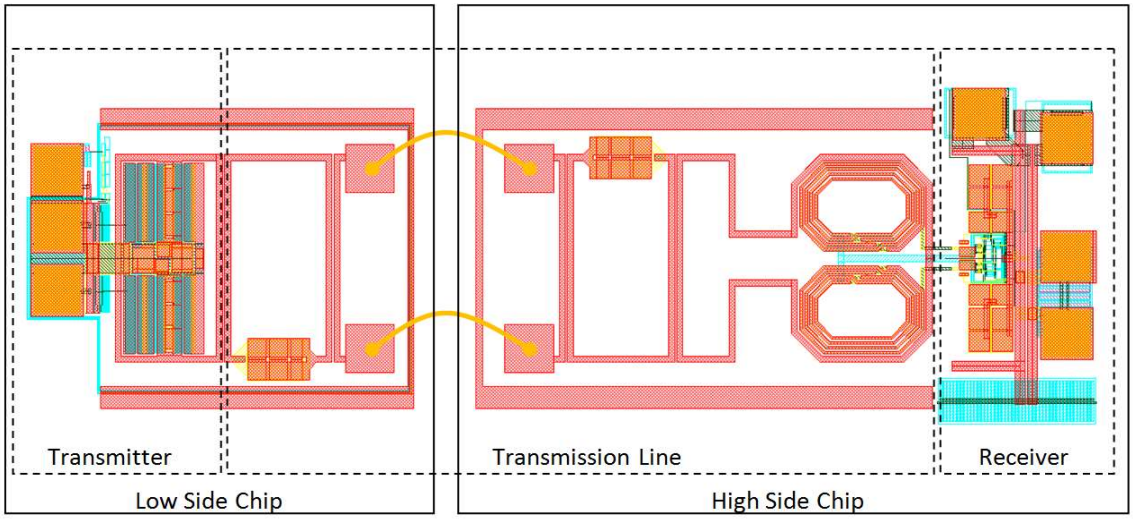

Fig. 2.1. Layout of galvanically isolated die-to-die translator.

The coupling of laterally positioned structures is weaker than vertical coupling therefore resonantly coupled inductors are employed in order to maximize the signal strength from the transmitter to the receiver. Generally, a weakly coupled transformer with primary and secondary coils having a coupling factor of k, equivalent inductance of L, series resistance of R, and quality factor of Q can be resonated with a shunt capacitance (C) to increase the transformer coupling to more than k, as derived [1]:

$$\left|\frac{V_o}{V_i}\right| \cong \frac{k}{\left|CL\omega^2\left(1-k^2\right)+\frac{R}{L\omega}j-1\right|} = \frac{k}{\left|\frac{1}{Q}j-k^2\right|} \cong kQ \qquad (1)$$

2.2 Physical test structures

The galvanically isolated translator is divided into the low side chip and the high-side chip, both interconnected by bonding wires. Therefore, the model of the transmission line is also divided into three model's subsets:

- Low-side part of the transmission line model,
- high-side part of the transmission line model, and
- bond-wire connection model.

An s-parameter-based model of each transmission line component has been extracted by employing an EM simulator. The s-parameter-based models have been then utilized in order to synthetize lump-element models which have been tuned according to the measurement results on the physical structures. The lump-element models of the low-side part and the high-side part of the transmission line are illustrated in Fig. 2.2. Each of the magnetically coupled blocks of the transmission line is represented by a separate lump-element model in order to simplify the model tuning and to provide greater insight into the system relations.

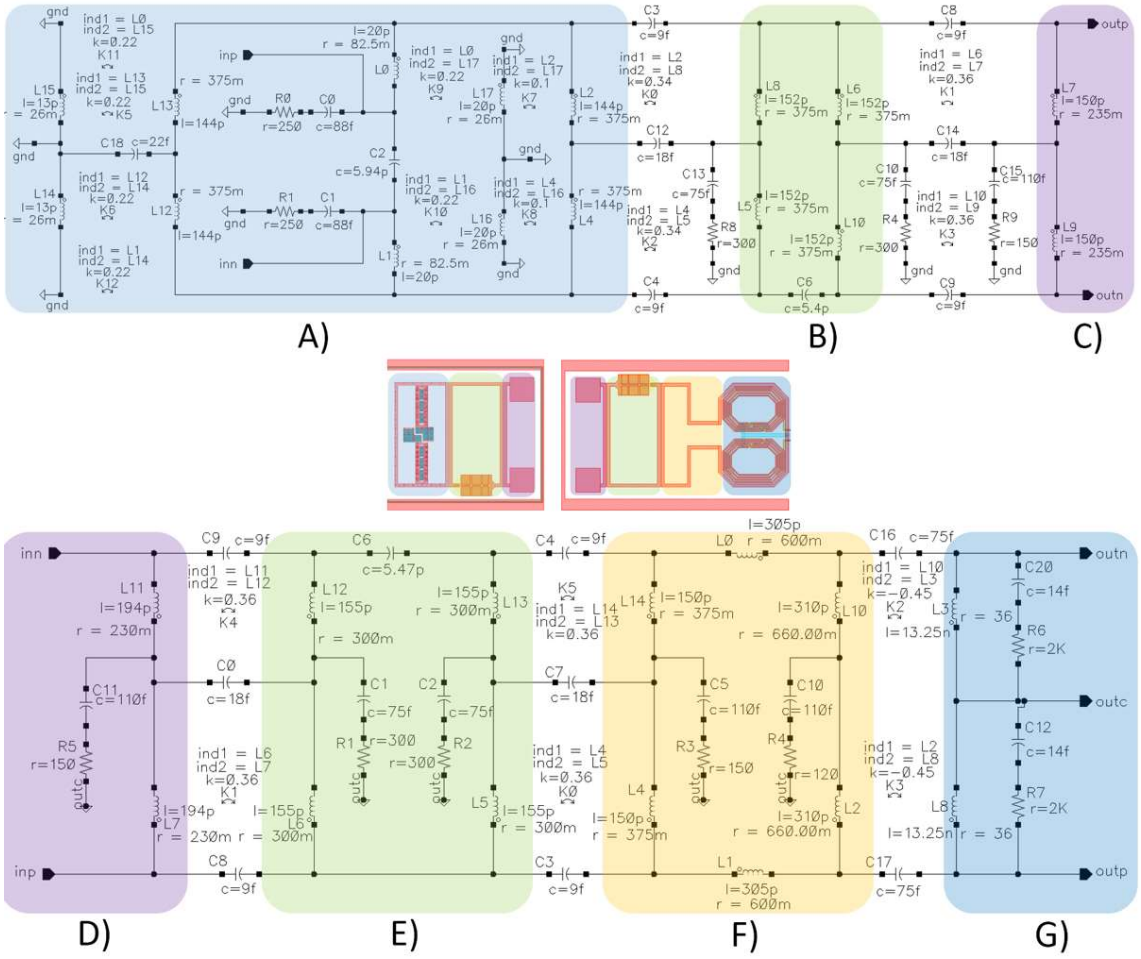

Fig. 2.2. Lump-element models of low-side and high-side part of transmission line. Individual parts of transmission line are highlighted: A) Oscillator loop. B) Fundamental resonator. C) Low-side half of bond-wire connection loop. D) High-side half of bond-wire connection loop. E) Fundamental resonator. F) Primary side of center-taped transformer. G) Secondary side of center-taped transformer.

All transmission line components need to be tuned precisely to the identical resonant frequency. Also a digital-to-RF scheme must be considered, since it represents the major contributor to current consumption of the galvanically isolated translator system. In order to evaluate the signal attenuation, as well as the viable communication scheme, extra test structures have been designed:

- Capacitor value skews of the coupled resonators,
- reduced transmission line with one coupled resonator removed,
- a transmitter generating pulse bursts,
- a transmitter generating a continuous signal,
- a receiver outputting a digital signal, and
- a receiver outputting an analog signal corresponding to received signal strength.

2.2.1 Receiver Outputting Analog Signal

Since on-chip direct measurement of RF signal attenuation is not possible, a dedicated receiver outputting analog signal representing the RF signal strength has been designed.

2.2.2 Transmitter Generating Pulse Bursts

Various applications require transmitting of pulses or pulse bursts in response to the input digital signal. In order to generate pulse bursts possessing a defined width, the transmitter generating a continuous signal is enhanced by an edge detector which detects the rising and falling edges of the digital control signal and activates the oscillator only during these events. The rising or falling edge of the input digital signal is represented by a different pulse burst width.

2.2.3 Capacitor Value Skews of the Coupled Resonators

The resonant frequency of the coupled resonators must be tuned precisely to the oscillator frequency in order to attain minimal signal attenuation of the received signal. Although both the fundamental resonator structure and the transmitter layout have been optimized by utilizing an EM simulator, various parasitic elements are typically not considered, and hence the final resonant frequency of either the oscillator or the fundamental resonator may differ.

It has been discovered in former designs of RF test structures that the typical parametric mismatch between the EM simulation and the physical structure does not exceed 5%. That implies that if the oscillator frequency was shifted by 5% and the fundamental resonator frequency was shifted by -5%, the total shift would come to 10%. The probability of such scenario is negligible; nevertheless, four structures with altered resonant frequency of the fundamental resonator have been designed. Since the resonant frequency of the fundamental resonator is given by the loop inductance and the parallel capacitance, the value of the MIM capacitors is altered to -10%, -5%, +5% and +10%.

2.2.4 Reduced Transmission Line

In order to thoroughly investigate the concept of resonantly coupled lateral structures, a test structure with the high-side fundamental resonator eliminated has been designed. The aim of this experiment is to demonstrate that the fundamental resonator does not

attenuate the transmitted signal, but conversely, the resonating element improves the coupling factor, thus reducing the signal attenuation. Since the lump-element model of the complete transmission line has been obtained, only the high side fundamental resonator is removed from the schematic diagram, as illustrated in Fig. 2.3.

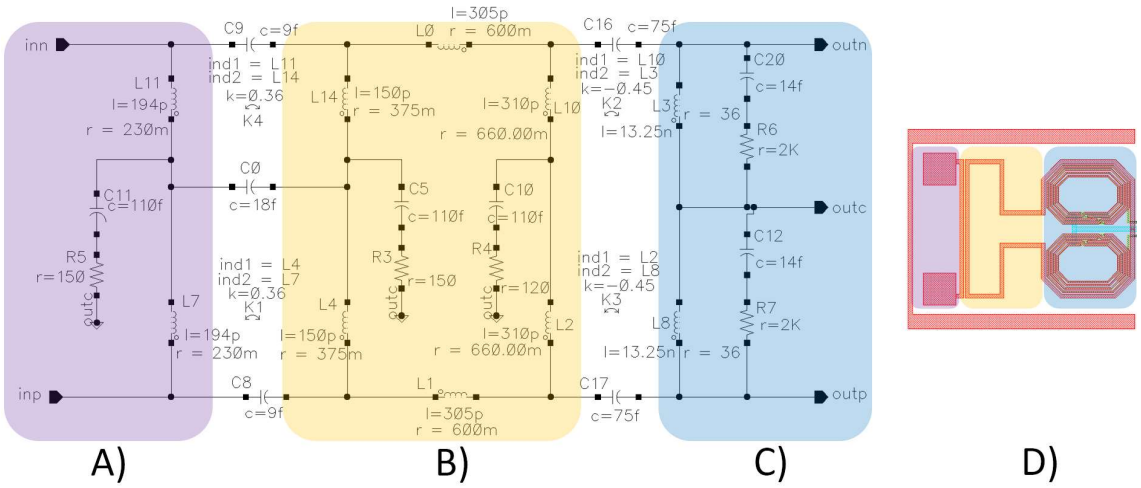

Fig. 2.3. Lump-element model of high side part of reduced transmission line. A) High-side half of bond-wire connection loop. B) Primary side of center-taped transformer. C) Secondary side of center-taped transformer. D) Layout of reduced transmission line.

The simulation outcome comparing the complete and reduced transmission line connected to the receiver outputting the analog signal are depicted in Fig. 2.4. The results illustrate that the presence of the resonating element on the high side part of the transmission line leads to 31% less signal attenuation.

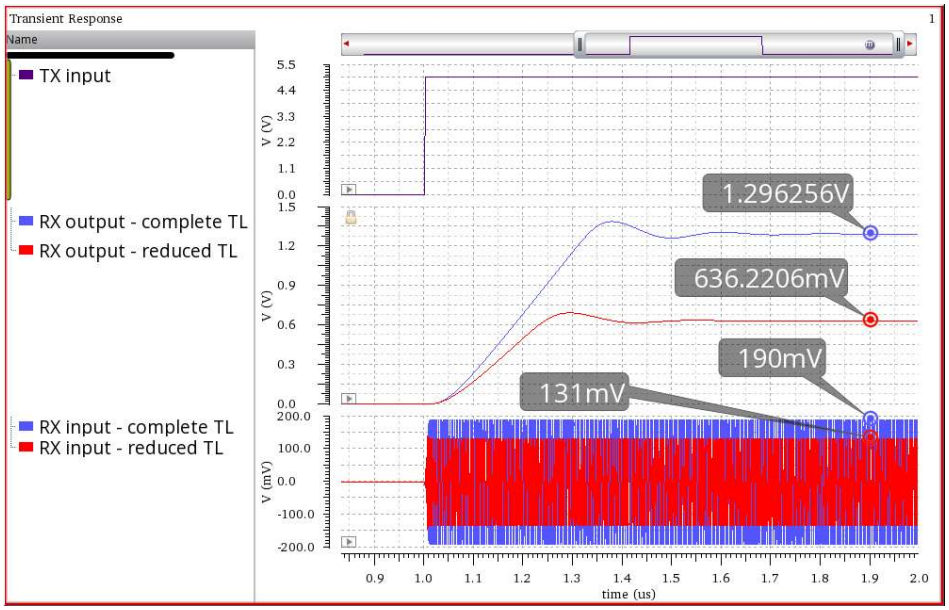

Fig. 2.4. Simulation results comparing complete and reduced transmission line. RX output voltage is measured as differential value between quiescent and active mode.

2.2.5 Evaluation of the Test Structures

The design is realized in the ONC25BCD process technology. The low side and high side chips are assembled as a multi-chip module in a SOIC-16 Dual Flag package utilizing the standard bond-wire assembly design as demonstrated in Fig. 2.5. Both the low side and high side chips are housed on separated flags of the lead frame as illustrated in Fig. 2.5 A), thereby allowing for HV bias between their reference potentials.

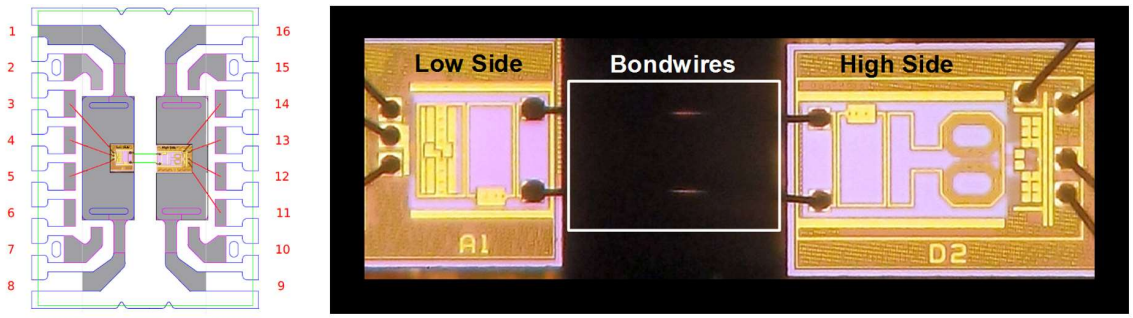

Fig. 2.5. Galvanically isolated translator system module. A) High side and low side chips assembly in SOIC-16 Dual Flag package. B) System micrograph.

The EM simulations and the lump-element model for the entire system was employed to design and predict the transmitter-to-receiver channel's voltage gain and resonance frequency. The combination of the above-listed test structures was further utilized in order to:

- Tune the lump-element model of the transmission line, and
- identify the specific parameter values for achieving the optimal system performance.

The measured average parameters of the physical test structures utilizing the receiver outputting the analog signal are listed in Table 2.1. The signal strength of the complete transmission line, the reduced transmission line and four capacitor skews of the fundamental resonator is expressed as the V_X differential voltage on the output of the receiver. The simulated results of the tuned transmission line lump-element model are also included for comparison. As can be seen from Table 2.1, the simulation and measured results reveal the identical trend.

Table 2.1. Measured parameters of the transmission line test structures at V_{TX} = 5 V.

		Measured			Simulated		
T-Line	V_{TX} [V]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]
Complete	5.0	346	2.86	1133	366	2.76	1296
Reduced	5.0	364	2.84	749	366	2.76	636
Complete_C-10 %	5.0	339	2.81	643	338	2.78	666
Complete _C-5 %	5.0	356	2.81	1193	350	2.76	1021
Complete _C+5 %	5.0	361	2.88	633	369	2.95	544
Complete _C+10 %	5.0	337	2.90	310	357	2.98	297

The high variation of the I_{TX} transmitter current consumption among the test structures is influenced by the structure-to-structure process variation and the self-heating mechanism. In order to significantly suppress the self-heating, the duty cycle of the transmitter activating signal was reduced to 1% during the measurement. The I_{TX} values in Table 2.1 have been recalculated to a 100% duty cycle, thus indicating the steady-state current consumption of the transmitter in the active mode.

Since the transmitter oscillator is not current limited, the I_{TX} current consumption depends on the supply voltage to a large extent. The measurement results with the V_{TX} supply voltage reduced to 4 V are listed in Table 2.2.

Table 2.2. Measured parameters of the transmission line test structures at V_{TX} = 4 V.

		Measured			Simulated		
T-Line	V_{TX} [V]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]	I_{TX} [mA]	f_{OSC} [GHz]	V_X [mV]
Complete	4.0	234	2.91	368	250	2.84	736
Reduced	4.0	244	2.90	288	250	2.84	417
Complete_C-10 %	4.0	232	2.85	417	232	2.80	492
Complete _C-5 %	4.0	240	2.86	640	240	2.79	731
Complete _C+5 %	4.0	242	2.93	191	243	3.01	216
Complete _C+10 %	4.0	228	2.94	95	239	3.02	130

Table 2.2 indicates that the current consumption of the transmitter is reduced by approximately 30 % at 4 V supply. The simulation has shown that the oscillator amplitude is also reduced, leading to the signal amplitude on the receiver input decreased by approximately 30 % as well, confirming that the intensity of the received signal remains well within the range detectable by the receiver. The comparison of the measured and simulated differential voltage on the receiver output is depicted in Fig. 2.6, which plots the V_X differential voltage waveforms over the variation of the fundamental resonator capacitor. The fundamental resonator is designed so that the resonant frequency reaches 2.75 GHz. As illustrated in Table 2.1 and Table 2.2, at 5 V supply, the oscillator frequency is shifted by approximately 3.5 %, which conveniently corresponds with the V_{TX} peak position in Fig. 2.6 A). At 4 V supply, the oscillator frequency is shifted by 6 %, which also corresponds with the V_{TX} peak position in Fig. 2.6 B).

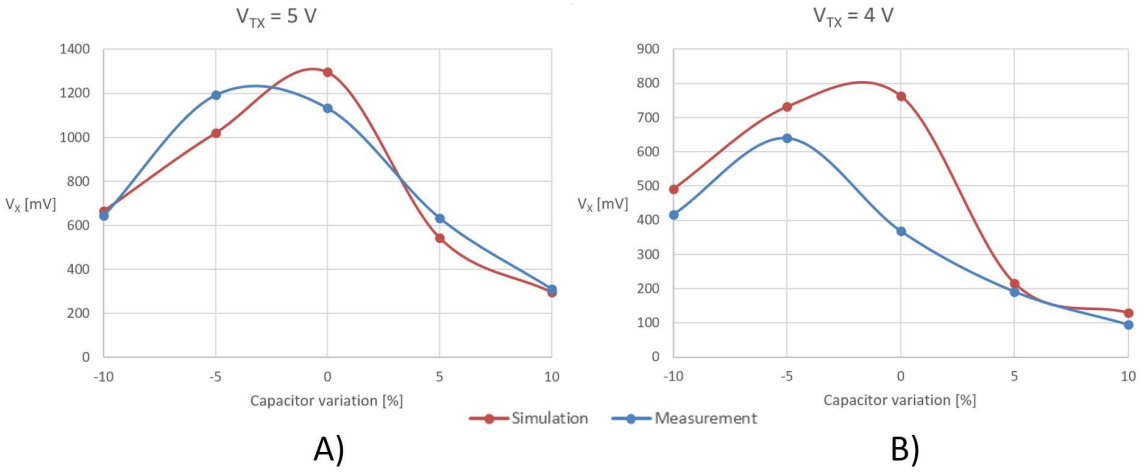

Fig. 2.6. Measured and simulated differential voltage on receiver output. A) Transmitter supply voltage 5 V. B) Transmitter supply voltage 4 V.

2.3 Communication through the Isolator

The communication through the transmission line introduced in Chapter 2 may be established by utilizing an RF signal detector only. Therefore two possible modulation schemes are considered for employment:

- ON-OFF Keying (OOK) digital modulation, or
- Pulse Width Modulation (PWM).

Both modulation schemes have been evaluated on physical test structures. The results achieved are discussed in the following sections.

2.3.1 ON-OFF Keying Digital Modulation

The principle underlying the OOK digital modulation is that the digital data is represented as either the presence or absence of a carrier signal. It does not matter whether the presence of the transmitted signal is assigned to the logic high state and the absence of the signal is assigned to the logic low state or vice versa. Depending on a concrete application, one of the assignment is usually more beneficial, particularly in the aspect of the system current consumption.

The merits of the OOK coding comprise high data rate as well as high robustness against an error. The major handicap is represented by the high current consumption due to continuous transmission of the carrier signal. The current consumption is therefore given by the duty cycle of the input digital signal only; it is not dependent on the input signal frequency.

The physical structures introduced in Section 2.2 have been characterized and the measured waveforms are depicted in Fig. 2.7. The output signal is inverted.

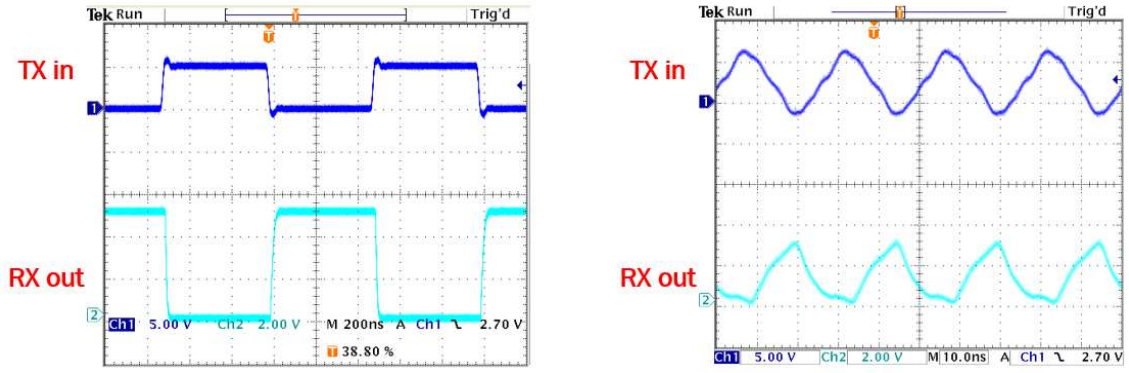

Fig. 2.7. Measured results of communication through the isolator using OOK modulation: A) 2 Mbps (1 MHz). B) 80 Mbps (40 MHz).

2.3.2 Pulse Width Modulation

In order to significantly reduce the current consumption of the translator, the PWM has also been evaluated. The principle of the PWM lies in the digital data being represented as a distinct width of a pulse, or pulse bursts, of a carrier signal. Similarly to the OOK modulation, it is of no substantiality whether the logic high is assigned to the wider pulse while the logic low is assigned to the narrower pulse, or vice versa.

In the half bridge driver application, it must be ensured that in the event of an erroneous reception, no serious damage of the application arises. Owing to that, it is beneficial to assign the narrow pulse to the logic low state (representing the deactivation of the driver) and the wider pulse to the logic high state (activation of the driver).

The current consumption of the transmitter is reduced, since the transmitter is activated only when the digital input signal alters its logic state. But the penalty of the lesser current consumption is that the transmitted data rate is limited, since two pulses are generated, one for each input signal transition. The width of the transmitted pulse must be decoded exactly, and hence the robustness against an error is also impacted. The test structures employing the transmitter discussed in 2.2.2 have been characterized and the measured waveforms are depicted in Fig. 2.8.

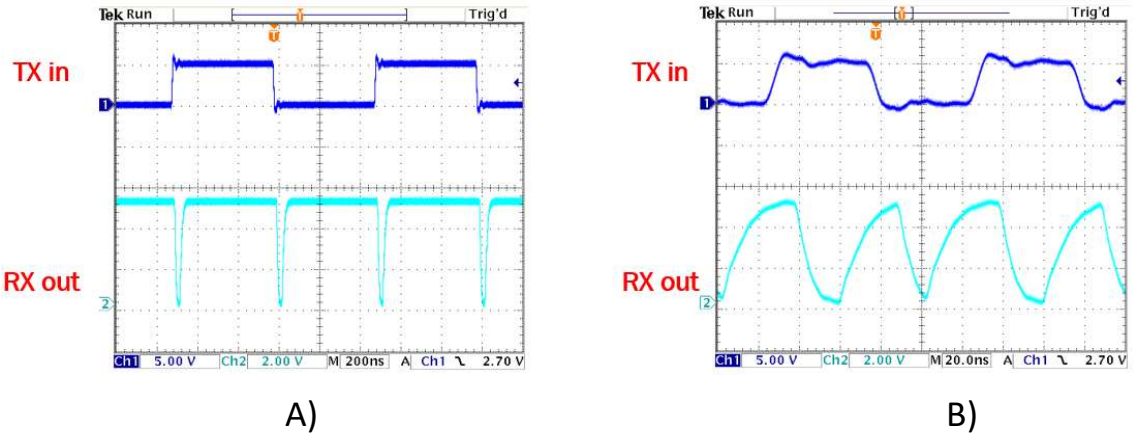

Fig. 2.8. Measured results of communication through the isolator using PWM coding: A) 2 Mbps (1 MHz). B) 20 Mbps (10 MHz).

The measured waveforms are distorted by the input capacitance of the oscilloscope probe. The waveform depicted in Fig. 2.9 shows that the physical measurement is in great conformity with the simulation if the identical load capacitance on the receiver output is incorporated.

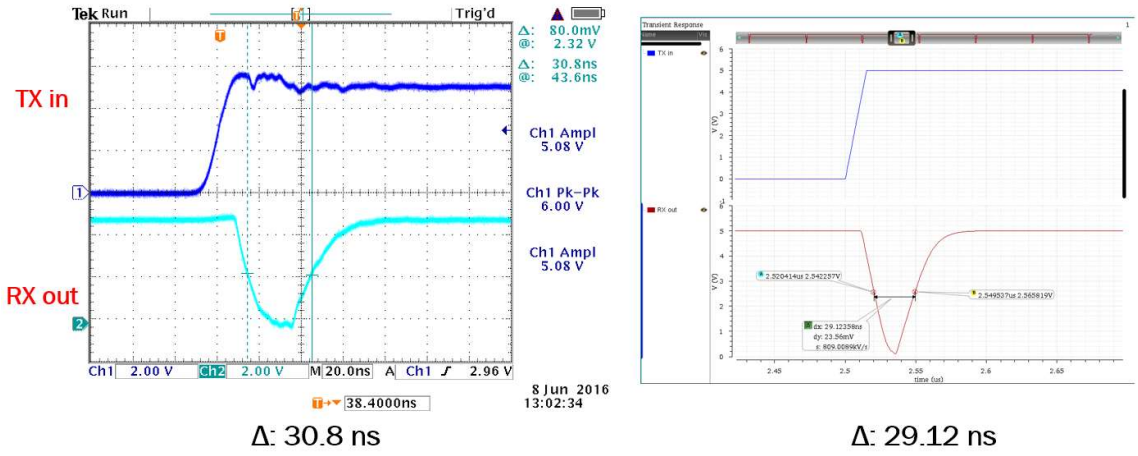

Fig. 2.9. Measured and simulated waveforms on receiver output. Test structure of the galvanically isolated translator utilizes transmitter generating pulse bursts.

The results of the signal pulse width and the propagation delay from the transmitter digital control input to the receiver output are listed in Table 2.3. The comparison of the measures between OOK and PWM schemes are shown in Table 2.4.

Table 2.3. Signal pulse width and propagation delay.

	Propagation delay [ns]		Pulse width [ns]	
	Low to High	High to Low	Low to High	High to Low
Measured	13.6	17.6	30.8	27.6
Simulated	12.7	17.6	29.1	24.6

Table 2.4. Comparison between OOK and PWM measures at 1 MHz input signal frequency.

Parameter	**OOK**	**PWM**
Power consumption I_{TX}	117 mA @ V_{TX} = 4 V	4.7 mA @ V_{TX} = 4 V
Power consumption I_{RX}	160 µA @ V_{RX} = 5 V	160 µA @ V_{RX} = 5 V
Data rates	High	Intermediate
Error robustness	High	Intermediate

2.4 Results and Discussion

The concept of the lateral resonant coupling introduced in this chapter has been prototyped and investigated using the test structures. This technique has been proved as a viable solution to increase the maximum achievable isolation rating in fully-integrated CMOS galvanic isolation designs. The proposed method utilizes the lateral on-chip spacing between resonant structures to provide galvanic isolation. The high sensitivity and low power receiver has been designed in order to guarantee reliable communication over process variation. The key parameters of the galvanically isolated translator are listed below:

- ONC25BCD, 4 metal process option.
- No high voltage process extension.
- Silicon area of the translator: 0.94 mm^2.
- Attained RMS isolation: 3.3 kV.

The lump-element model of the transmission line has been obtained in order to enable the simulation of complex systems integrated in this concept of the galvanically isolated translator.

3 DESIGN OF 800 V GALVANICALLY ISOLATED HALF BRIDGE DRIVER FOR INDUSTRIAL APPLICATIONS

Among industrial applications, safety requirements are not the driving reasons for which the galvanic isolation is required. The galvanically isolated translator introduced in Chapter 2 which has been developed in the first phase of the development replaces the standard junction-isolated high voltage level shifter in order to provide:

- Advanced noise immunity, specifically against high dV/dt transitions,
- negative transient immunity, and
- higher operating voltage.

Fig. 3.1 depicts the segmentation of the half bridge driver for industrial applications in the package. All the low voltage signals are processed by the low voltage die. The high voltage die is responsible for driving the high side external MOSFET only.

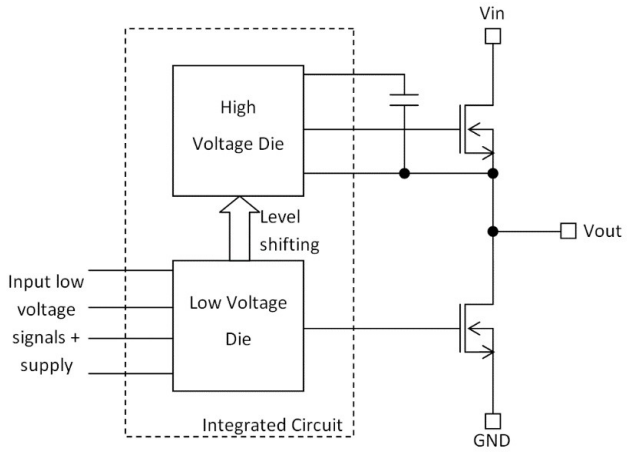

Fig. 3.1. Proposed multi-die concept of half bridge driver for industrial applications.

Both high and low voltage dice have been fabricated in ONC25BCD technology. The design introduced in Chapter 2 has been employed as the galvanically isolated translator. It has been proven on the test structures that employing four metal layers guaranties 3.3 kV RMS isolation. Such value is sufficiently high for 800 V reliable operation. The device also complies with the HBM ESD JEDEC standard [3], since the 3.3 kV RMS offers higher breakdown value than required by the HBM ESD standards.

3.1 Communication through the Isolator

Due to the current consumption constrains, the PWM has been chosen as the sensible candidate for the half bridge driver design. The input control signal is modulated by the edge detector, discussed in Section 2.2.2, in order to provide 40 ns and 20 ns pulses representing the leading and the falling edge of the input signal respectively. The pulse bursts are transmitted to the high voltage die, where they are demodulated to obtain the high side driver control signal.

3.2 Low Voltage Die

The low voltage die houses several circuits responsible for the low side driver operation and the transmission of the high side driver control signal. The layout overview of the low voltage die is illustrated in Fig. 3.2. The die size amounts to 1.3 × 1.2 mm.

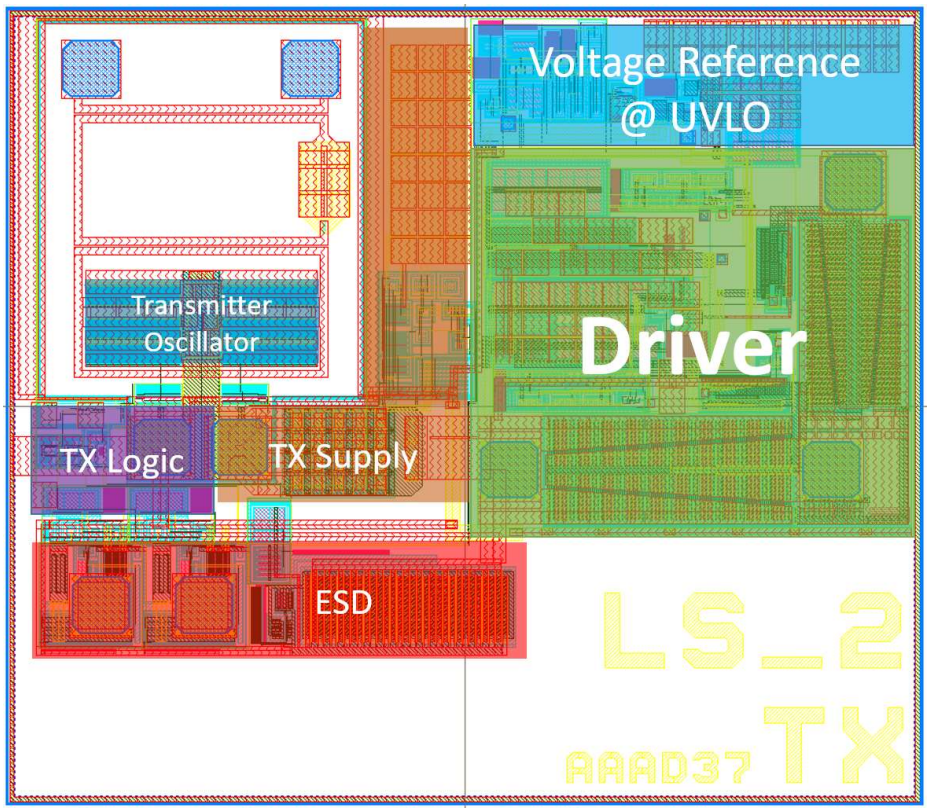

Fig. 3.2. Layout of low voltage die of half bridge driver for industrial applications.

3.2.1 Transmitter with Oscillator

The transmitter with oscillator from Chapter 2 has been utilized in order to drive the transmission line. As discussed in Section 2.2.5, its reliable operation is provided if the supply voltage is higher than 4 V. Nevertheless, at 5 V supply, the current consumption of the transmitter increases significantly. Therefore, the 4.5 V value has been chosen as the compromise ensuring sensible voltage margin for stable operation.

3.2.2 Transmitter Power Supply

During pulse transmission, the transmitter current consumption increases from substantially zero current to its maximum value. The transmitter power supply is capable to deliver approximately 300 mA current in an extremely short time.

3.2.3 Transmitter Logic

The transmitter logic translates the input control signal into pulses which are transmitted to the high side die. In order to enhance noise immunity and to normalize the input control signal to the internal 5 V supply domain, the input signal is initially processed by the Schmitt Trigger.

3.2.4 Voltage Reference and Under-Voltage Lock-Out (UVLO)

The low voltage die features the under-voltage lock-out (UVLO) function to disable the output gate driver during low supply voltage conditions. The UVLO circuit includes a hysteresis in order to prevent cyclic turn on and off of the device due to supply voltage instability.

3.2.5 ESD Protection

In order to protect the low voltage die against the Electro-Static Discharge (ESD), the ESD protection has been implemented. In this design, the central clamp architecture is utilized.

3.2.6 Output Driver

The output driver is responsible for driving an external MOSFET. In this design, the output driver possess 2 A source and sink capability, which is an ample value for target half bridge applications.

3.3 High Voltage Die

The high voltage die houses circuits responsible for the high side driver operation and the reception of the high side driver control signal. The layout overview of the high voltage die is shown in Fig. 3.3.

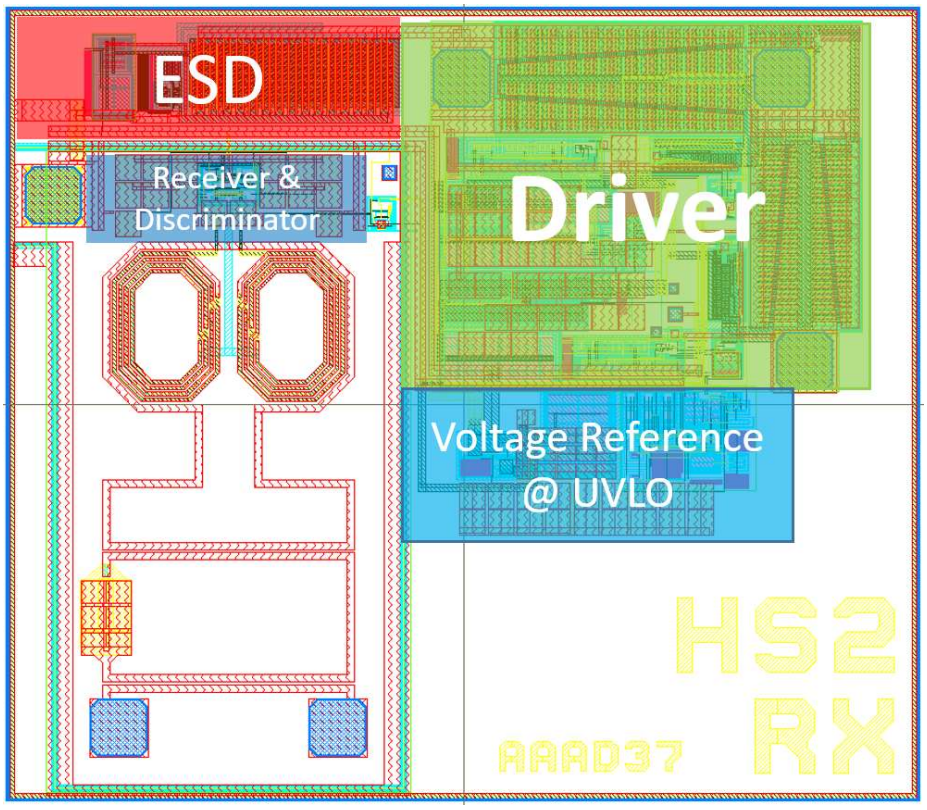

Fig. 3.3. Layout of high voltage die of 800 V half bridge driver for industrial applications.

Since the high side gate driver must possess the same electrical characteristics as the low side gate driver, several circuits designed for the low voltage die are also utilized on the high voltage die. The identical circuits are listed below:

- Voltage Reference and Under-voltage Lock-out (UVLO),
- output driver, and
- ESD protection.

3.3.1 Receiver with Discriminator

The received signal on the high side part of the transmission line is processed by the receiver. The width of the pulses on the receiver output is practically identical to those generated by the transmitter logic. The output of the receiver is connected to the discriminator which demodulates the pulses, thereby generating the gate driver control signal.

3.4 Evaluation of the Half Bridge Driver

The design of the 800V galvanically isolated half bridge driver for industrial applications has been prototyped and encapsulated in a fashion similar to the galvanically isolated translator discussed in Chapter 2. The SOIC-16 Dual Flag package utilizing the standard bond-wire assembly approach has been utilized to assembly low voltage and high voltage dice as a multi-chip module, as illustrated in Fig. 3.4.

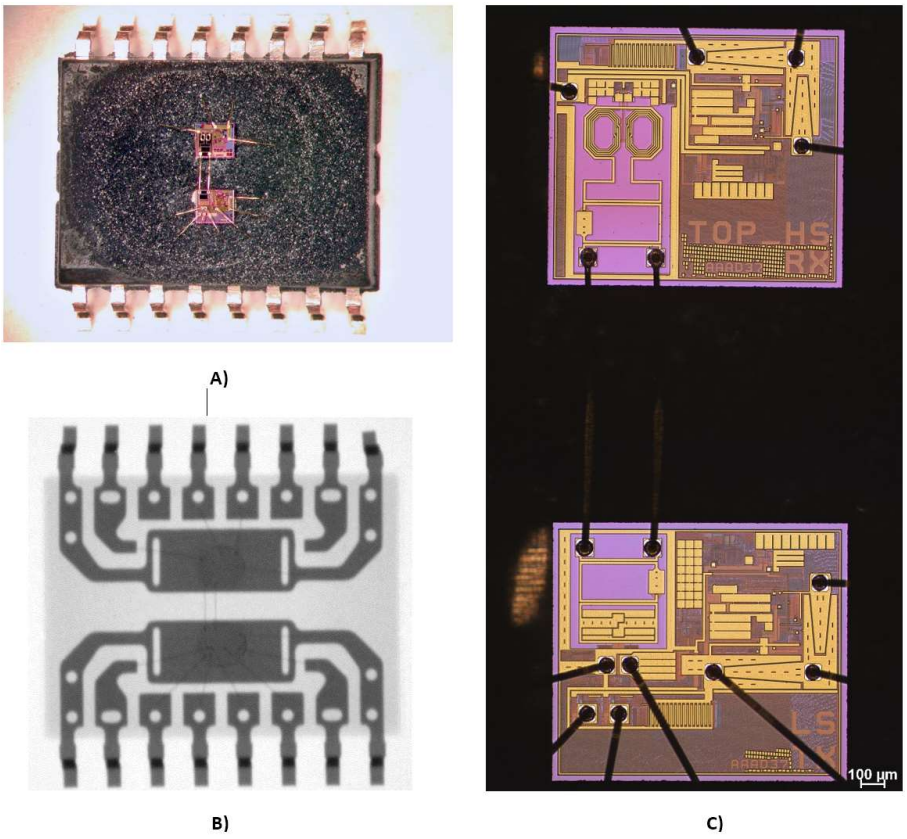

Fig. 3.4. Half bridge driver for industrial applications. A) Locally de-capsulated IC. B) X-ray photo of the IC depicting two galvanically isolated flags of the lead frame. C) Zoom-in on low voltage and high voltage dice (lower and upper respectively).

3.4.1 Input to Output Propagation Delay

The input-to-output propagation delay of both the high side and low side gate drivers has been evaluated by employing the test configurations illustrated in Fig. 3.5. The high side ground is DC biased to +/-1600 V in the test configuration depicted in Fig. 3.5 B).

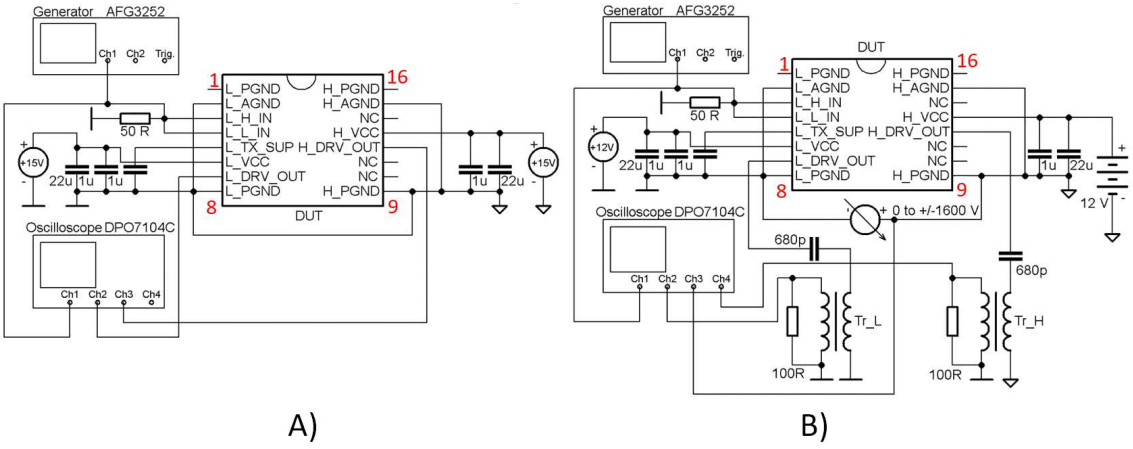

Fig. 3.5. Schematic diagram of test configuration for propagation delay measurement. A) Both low side and high side drivers grounded. B) High side driver ground biased to +/-1600 V. Pulse transformers (Tr_L and Tr_H) are utilized to transfer output driver edges to oscilloscope.

In order to evaluate the designed half bridge driver under dynamic conditions, the test configuration has been further modified as depicted in Fig. 3.6 A). The high side ground oscillation is controlled by the NCP1399 application board [4]. The continuous measurement results are demonstrated in Fig. 3.6 B). The fluctuation of the high side propagation delay does not exceed 0.5 ns, and is most likely induced by the noise generated by the applied dynamic signal. The oscilloscope is synchronized to the low side driver output signal, thus the depicted fluctuation of the high side propagation delay is effectively the sum of the high side and low side propagation delay variations.

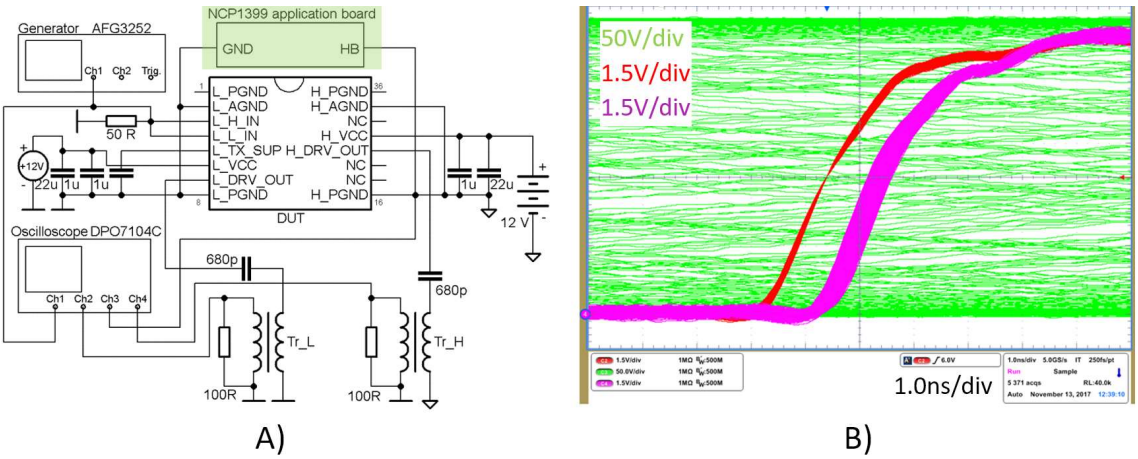

Fig. 3.6. Test configuration for the dynamic measurement. A) Schematic diagram. High side ground is dynamically biased by NCP1399 application board. B) Continuous measurement illustrating propagation delay variation. Red – low side driver output, violet – high side driver output, green – high side ground.

The results of the propagation delay measurement are listed in Table 3.1 and demonstrate that the propagation delay of the high side driver is not dependent on the high-side ground bias.

Table 3.1. Results of propagation delay measurement.

	Grounds shorted		High Side ground biased	
	Rising edge [ns]	Falling edge [ns]	Rising edge [ns]	Falling edge [ns]
Low Side	54.1	50.4	54.1	50.4
High Side	55	51.7	55	51.7
Matching (HS - LS)	0.9	1.3	0.9	1.3

3.4.2 Gate Driver Current Capability

The measured values of the gate driver current sink and current source driving capability are listed in Table 3.2. The rise time and fall time values are measured on the 1 nF load capacitor.

Table 3.2. High side and low side gate driver current capability.

	Rise time [ns]	Fall time [ns]	Source [A]	Sink [A]
Low Side	5.9	5.5	2.9	2.6
High Side	5.9	5.4	2.6	2.7

3.4.3 Common Mode Transient Immunity

The CMTI of the high side driver has been evaluated in the test configuration depicted in Fig. 3.7 A). The NCP1392 controller [5] has been utilized as a floating pulse generator to provide driver control signals. In order to minimize potential parasitic capacitance of a power supply, 12 V batteries have been employed as the power sources. An example of the waveform in Fig. 3.7 B) illustrates the 160 V/ns slope of the CMTI test signal applied between the low side and high side grounds. The probe of the oscilloscope is referred to the high side ground.

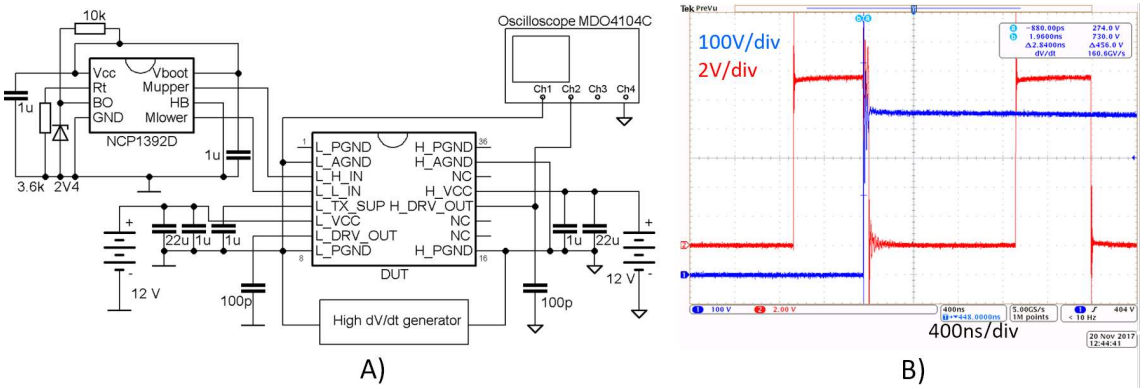

Fig. 3.7. CMTI measurement. A) Schematic diagram of CMTI test configuration. B) CMTI test waveform demonstrating 160 V/ns slope applied between high side and low side ground terminals (blue).

Two sets of the CMTI test signals have been applied by the 600 V high-dV/dt generator in order to evaluate the CMTI:

- 160 V/ns,
- 650 V/ns.

Examples of the 650 V/ns CMTI test waveforms are depicted in Fig. 3.8.

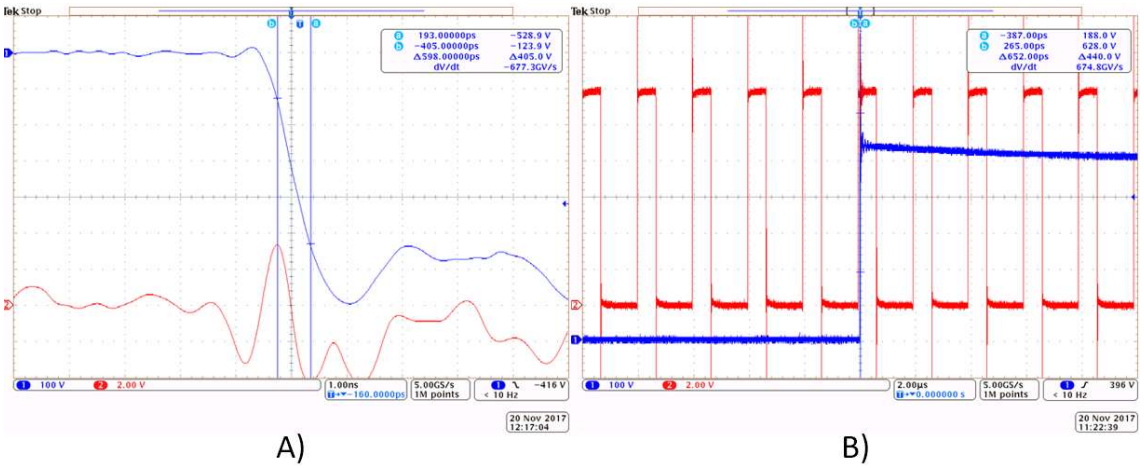

Fig. 3.8. CMTI test waveforms. A) Detail of the high-dV/dt signal demonstrating blue waveform possessing 677 V/ns slope. B) Example of CMTI test signal (blue) interfering with driver output.

The CMTI measurement has proved that the designed galvanically isolated half bridge driver is immune to the common mode transients sloping up to 650 V/ns.

3.4.4 LLC Resonant Converter Application

In this test, the designed half bridge driver has been employed in the LLC resonant converter. The NCP1395 controller [6] has been utilized, since it requires an external half bridge gate driver. The LLC application has been tested under full-range load conditions. As illustrated in Fig. 3.9, no gate driver malfunction has been observed.

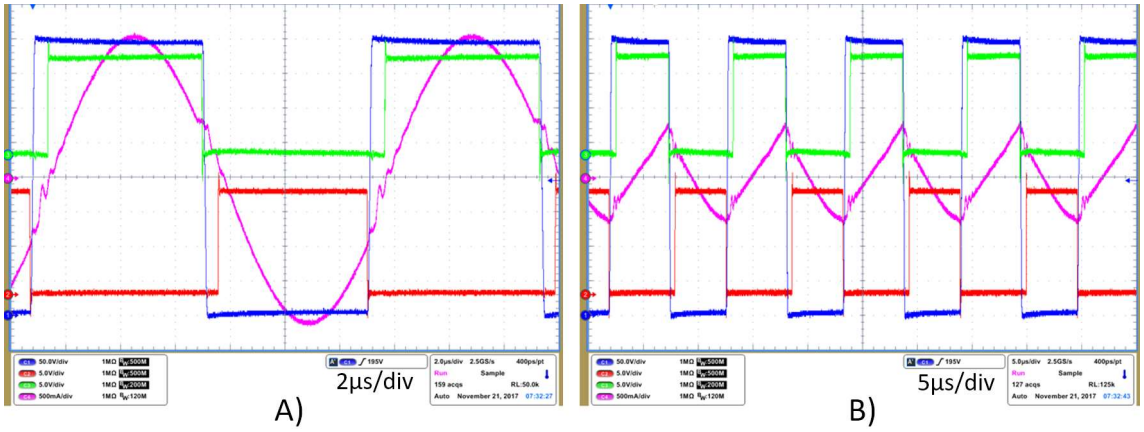

Fig. 3.9. Measured waveforms of LLC application. Blue – bridge node voltage, green – high side MOSFET gate voltage, red – low side MOSFET gate voltage, violet – primary side current. A) Full load. B) Light load.

3.4.5 Current Consumption

The measured current consumption is listed in Table 3.3. Three sets of the load capacitors have been evaluated. The measurement results indicate that the maximum operating frequency of the half bridge driver amounts to 500 kHz, since the current consumption increases rapidly at 1 MHz.

Table 3.3. Measured current consumption of the low side (I_{LS}) and high side (I_{HS}) driver.

Frequency	C_{LOAD} = 0		C_{LOAD} = 100 pF		C_{LOAD} = 1 nF	
	I_{LS} [mA]	I_{HS} [mA]	I_{LS} [mA]	I_{HS} [mA]	I_{LS} [mA]	I_{HS} [mA]
No switching	0.18	0.13	0.18	0.13	0.18	0.13
100 kHz	2.75	0.30	3.00	0.54	4.26	1.58
500 kHz	12.8	0.88	13.9	2.09	20.2	7.20
1 MHz	25.1	1.59	27.3	3.83	39.9	14.2

3.5 Results and Discussion

The galvanically isolated half bridge driver for industrial applications has proved itself a viable target application for galvanically isolated translators utilizing lateral resonant coupling. The presented design of the half bridge driver amply satisfies the listed industrial application requirements:

- High breakdown voltage,
- high negative transient immunity, and
- high CMTI.

The half bridge driver has been tested in LLC resonant converter application under both normal operation and heavy overload conditions. No gate driver malfunction has been observed. The measured high side and low side propagation delay equals 50 ns with perfect matching between the drivers. The propagation delay is not sensitive to the high voltage bias, either under static or dynamic conditions. The current consumption measurement revealed that the maximum operating frequency of the presented half bridge driver design is 500 kHz. Such value is adequate for target applications utilizing MOSFET devices. The driver current capability is also equivalent for the target applications.

4 DESIGN OF GALVANICALLY ISOLATED TRANSLATOR FOR HV APPLICATIONS

In the second phase of the development, a different coupling device has been employed in order to attain a higher value of the isolation voltage. The target isolation voltage is at least 4 kV_{rms}, applied and measured on the galvanic isolator over the time interval of one minute, as required by the international standards [7], [8]. Similarly to the design discussed in Chapter 2, the multi-die system is utilized.

4.1 Transformer Design

The layout of the differential coreless transformer with a center-tapped primary coil is depicted in Fig. 4.1. The primary side coil is formed by the 1st and 2nd metal layers in parallel in order to reduce the serial resistance. The thickness of the top metal forming the secondary coil is 3 µm, which provides comparable serial resistance to the primary coil. As can be seen in Fig. 4.1, the direction of the upper coil turns is reverse to the direction of the lower coil turns. Owing to that, currents generated by an external electromagnetic field are subtracted from each other, thus providing EMI (Electromagnetic Interference) immunity. The transformer dimensions amount to 770 x 650 µm.

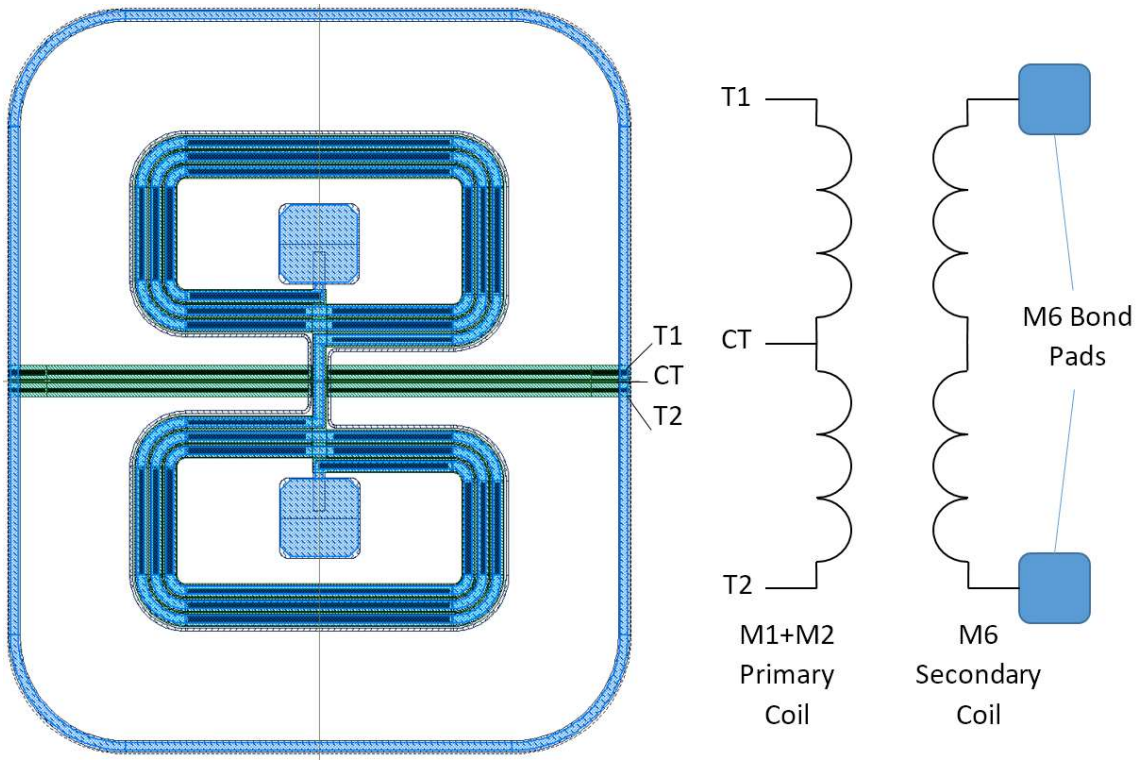

Fig. 4.1. Layout of differential coreless transformer with center-tapped primary coil.

Two different designs utilizing the differential coreless transformer have been prototyped and evaluated in this work:

- Bidirectional digital galvanic isolator, and
- analog galvanic isolator.

4.2 Fabrication Process

The galvanically isolated translator for HV applications utilizes the ONC25BCD technology which is extended by an additional 6th metal layer. The high isolation voltage is increased by the thick oxide formed between the 5th and the 6th metal layers. In order to maximize the isolation barrier, the 3rd and 4th metal layers are not employed in the transformer design. Consequently, the thickness of the isolation barrier is approximately 7.4 µm, which is an adequate value for attaining at least 2.2 kV_{rms} reliable isolation voltage. Two identical transformers connected in series, one on each die, are employed in the design, thereby doubling the isolation voltage to 4.4 kV_{rms}. Nevertheless, the measurement indicates that the achieved isolation voltage amounts almost to a value twice as high - 7.8 kV_{rms} [9].

4.3 Communication through the Isolator

In comparison with the translator discussed in Chapter 2, the transformer-based translator is capable of transmitting a single pulse signal from the primary to the secondary side. Therefore, the ultra-wideband (UWB) pulse polarity modulation (PPM) is utilized in the designs discussed in this chapter, enabling a high data rate, low power consumption and low propagation delay communication through the isolator. The simulation results of the UWB modulation are depicted in Fig. 4.2. The logic high is assigned to the positive pulse and the logic low is assigned to the negative pulse. Fig. 4.2 B) demonstrates that the pulse width reaches approximately 320 ps, thus the transmitted amount of energy is significantly lower when compared to PWM or OOK modulation.

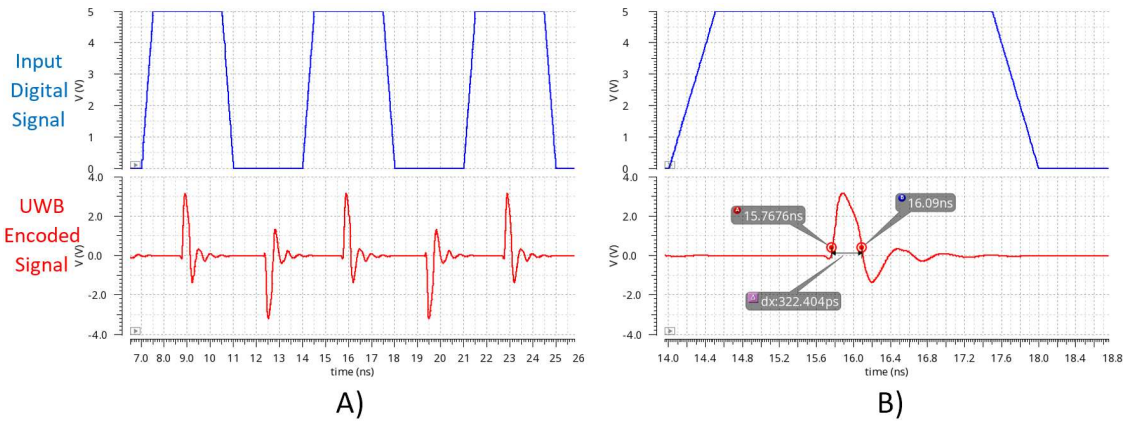

Fig. 4.2. UWB modulation. A) Simulation results. B) Detail of positive pulse representing logic high. Pulse width is approximately 320 ps.

4.4 Bidirectional Digital Galvanic Isolator

The implemented design includes two identical chips interconnected via two bond wires. Each chip consists of a differential coreless transformer with a center-tapped primary coil and a transceiver connected to this primary coil of the transformer. The rising and the falling edge detector is connected to the positive and negative pulse input respectively. Depending on the input, the transmitter encodes the input data rising edge and falling edge to a differentially positive and negative impulse respectively.

The schematic diagram of the transceiver is depicted in Fig. 4.3. The primary winding of the center-tapped transformer introduced in Section 4.1 is connected to the T1 and T2 terminals. The center tap (CT) is grounded. Fig. 4.3 illustrates that the transmitter's output is directly connected to the receiver's input.

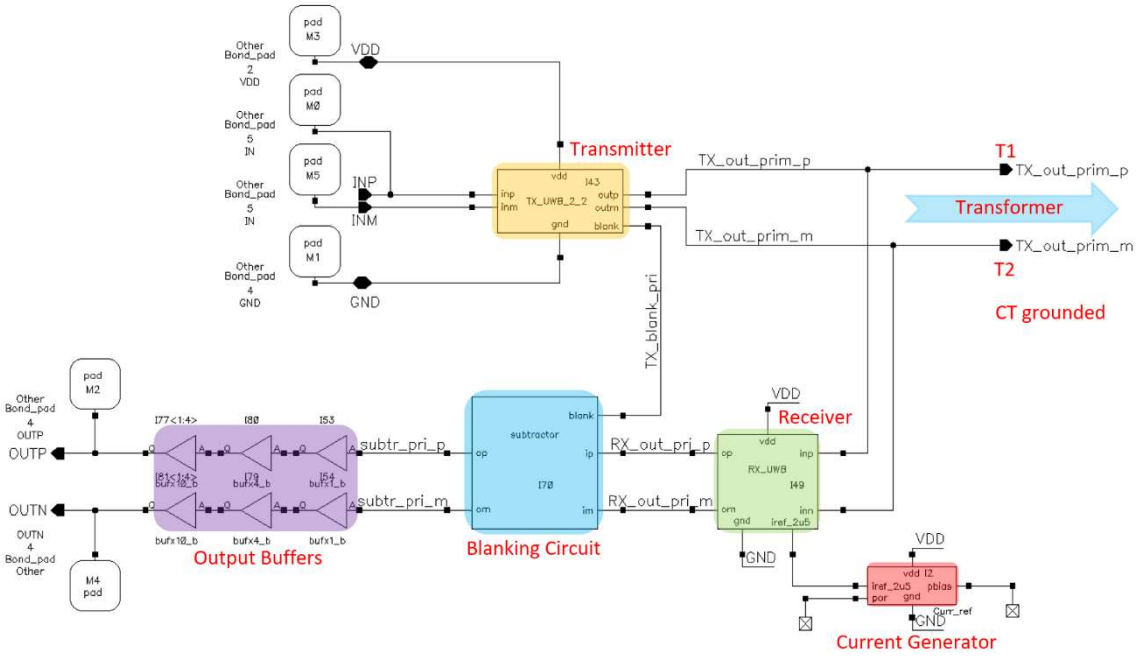

Fig. 4.3. Schematic diagram of the transceiver. Transceiver is connected to center-tapped primary coil by T1 and T2 terminals. Center tap is grounded.

4.4.1 UWB Transmitter

The transmitter generates UWB pulses in response to the input signal. The transmitter consists of two identical transformer drivers (OUTP, OUTM) differing in the edge detectors on their inputs. The upper and lower driver generates the UWB pulse on every rising and falling edge of the input control signal, respectively. Since the T1 and T2 transformer terminals are excited against the GND alternately, only a positive pulse is generated on both OUTP and OUTM outputs.

4.4.2 UWB Receiver

The UWB receiver provides demodulation of the UWB pulses. The T1 and T2 differential inputs are connected to the primary coil of the center-tapped transformer in a fashion similar to the transmitter. The received positive and negative pulse is outputted on the OUTP and OUTM receiver's outputs respectively. The receiver utilizes the identical fundamental concept as the receiver employed in Chapter 2.

4.4.3 Blanking Circuit

The blanking circuit is connected between the negative and positive receiver outputs and the respective chip's outputs to mute the receiver outputs during data transmission and hence to avoid self-interference from the chip's transmitter. The blanking circuit is triggered on the rising edge of the blank input signal generated in the transmitter.

4.4.4 Evaluation of the Bidirectional Digital Galvanic Isolator

The bidirectional digital galvanic isolator has been prototyped and encapsulated in a fashion similar to the galvanically isolated systems discussed in Chapters 2 and 3. The SOIC-16 Dual Flag package has been utilized to assembly low voltage and high voltage dice as a multi-chip module, as illustrated in Fig. 4.4.

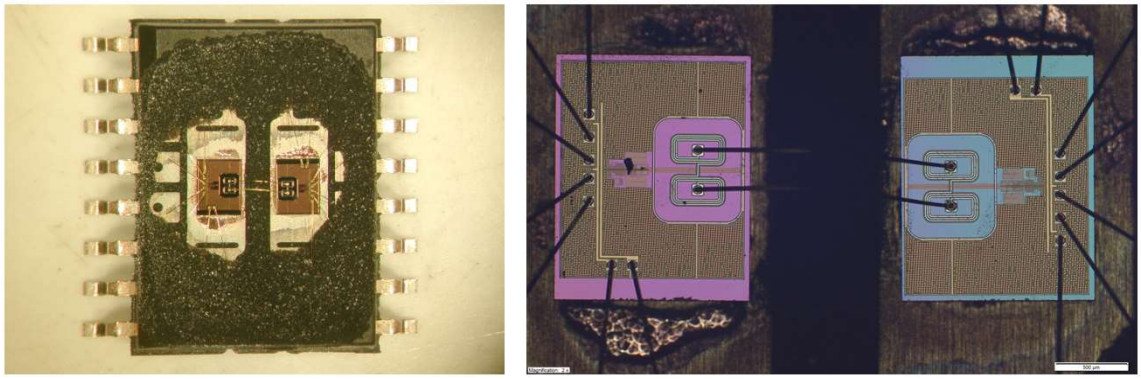

Fig. 4.4. System module assembled in SOIC-16 Wide Body package. A) Locally de-capsulated IC. B) Micrograph with both chips.

The galvanic isolator has been evaluated in the test configuration depicted in Fig. 4.5. The external RS1 and RS2 flip-flops have been inserted to decode the output pulses back to a square wave signal. The high side is also equipped with the V5 voltage regulator in order to provide 5 V floating power supply during CMTI measurements. The low and high side inputs are terminated by 50 ohm resistance to match the characteristic impedance of the transmission line between a pulse generator and the test board. Both the pulse and square wave output signals are accessible on the LS and HS output terminals. The high dV/dt generator for the CMTI measurements is connected to the CMTI terminals.

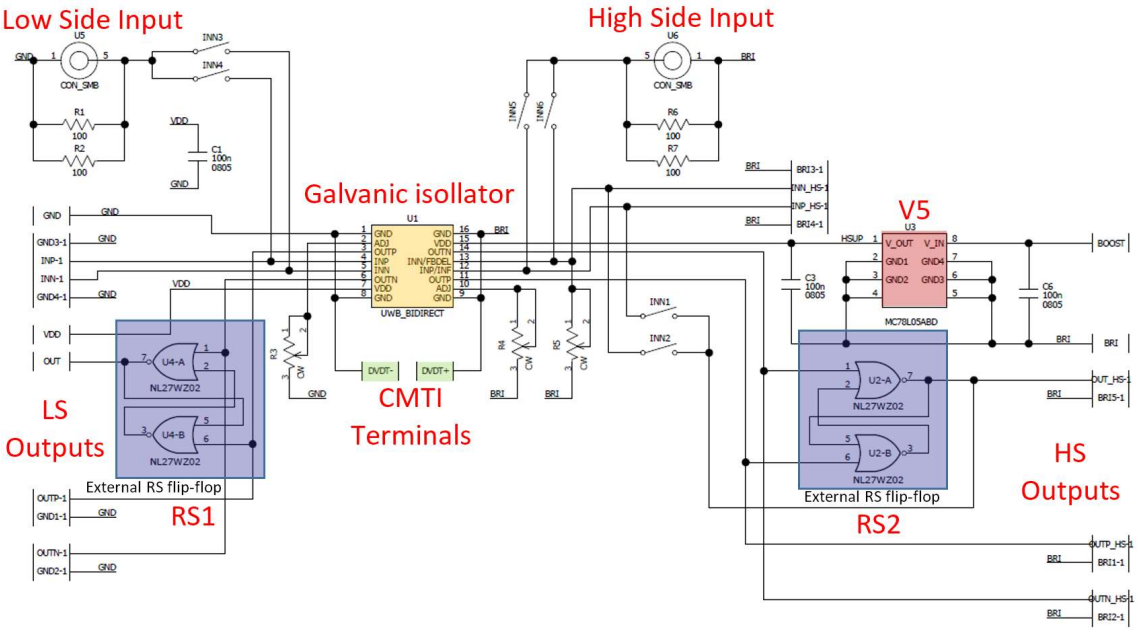

Fig. 4.5. Schematic diagram of the bidirectional digital galvanic isolator test configuration.

The measured waveforms of the unidirectional operation are illustrated in Fig.4.6. The RS flip-flop has not been utilized and both positive and negative inputs have been shorted together in the measurement. The galvanic isolator reaches stable operation for the 150 MHz input control signal frequency that results in 300 Mb/s data rate, since each input pulse generates two output pulses – OUTP and OUTN at the rising and falling edge of the input signal, respectively.

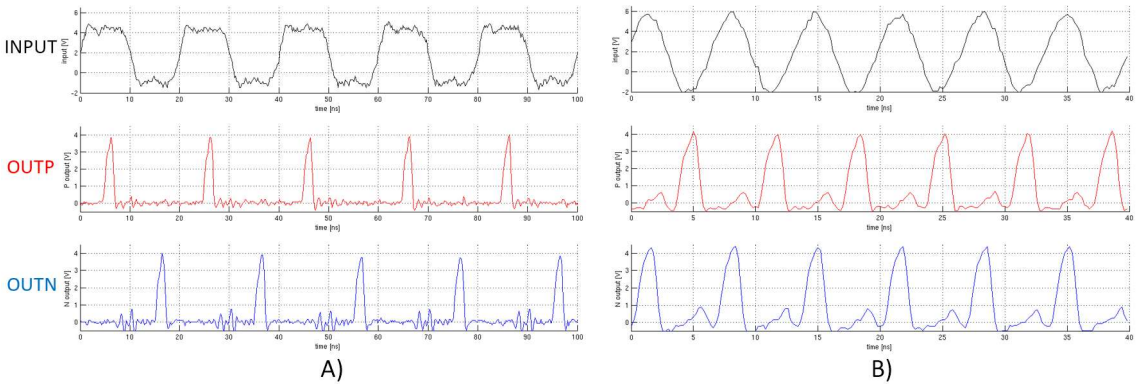

Fig.4.6. Measured waveforms of unidirectional operation of the galvanic isolator without external R-S flip-flop. A) 50 MHz operation. B) 150 MHz operation.

The bidirectional operation is demonstrated in Fig.4.7. The positive and negative control signal inputs are shorted together to provide both positive and negative output pulses in response to a single control signal. The external RS flip-flops generate a significant phase shift as may be seen in Fig.4.7 A). Fig.4.7 B) illustrates that in the bidirectional mode, the galvanic isolator achieves stable operation for the 68 MHz input control signal frequency resulting in 136 Mb/s simultaneous data rate in both directions. Certainly, for the bidirectional operation, precise timing is essential in order to avoid the transmitted and received pulses interfering with each other.

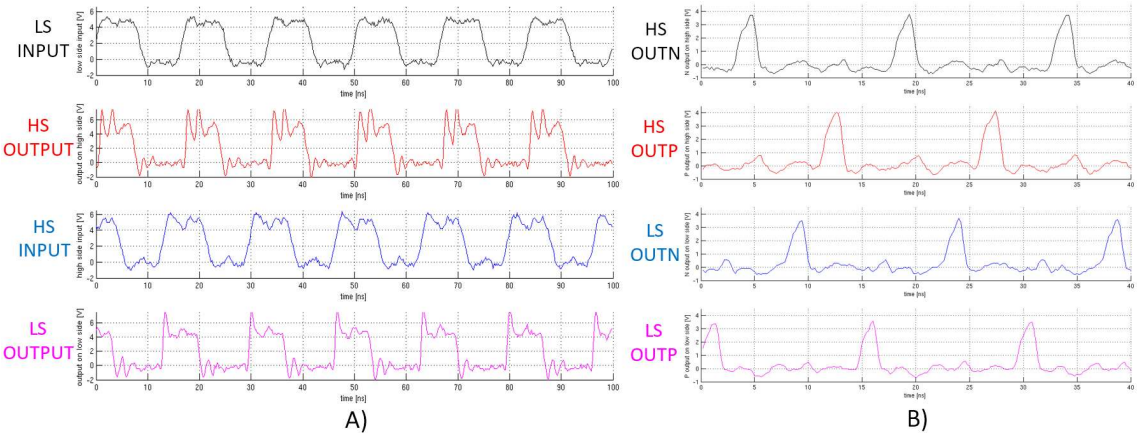

Fig.4.7. Measured waveforms of bidirectional operation of the galvanic isolator. A) 60 MHz operation utilizing external RS flip-flops. B) 68 MHz operation without external RS flip-flops. Only outputs are shown due to limitation of oscilloscope probes number.

The measured propagation delay of the control signal from the input to the output through the galvanic isolation barrier amounts to 4.3 ns.

A closed-loop configuration has been utilized to evaluate the CMTI of the bidirectional galvanic isolator. Both low and high side RS flip-flops has been employed to provide the rectangular output signal. The output of the high side RS flip-flop has been connected to the positive and negative high side inputs, both shorted together, thus the high side output signal is instantly transmitted back to the low side and showing on the low side output. The high dV/dt generator has been connected to the CMTI terminals (Fig. 4.5) to provide the positive and negative slope of the test signal. Examples of the measured waveforms are depicted in Fig. 4.8.

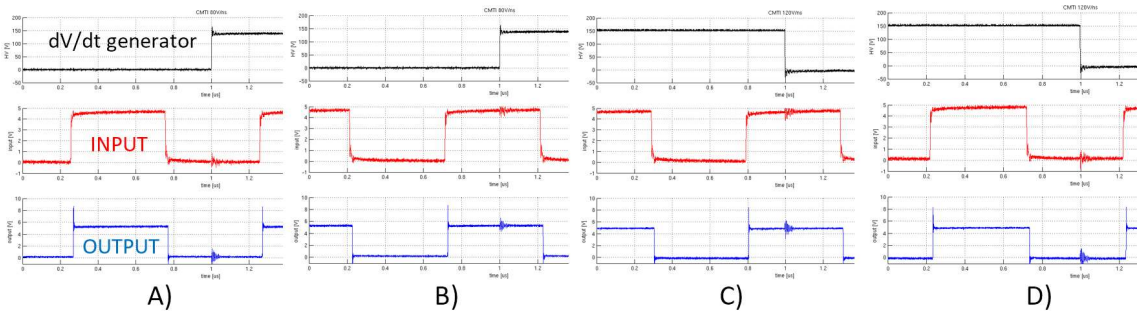

Fig. 4.8. CMTI measurement. A) Positive dV/dt slope at input low. B) Positive dV/dt slope at input high. C) Negative dV/dt slope at input high. D) Negative dV/dt slope at input low.

The galvanic isolator operates stably at 80 and 120 V/ns positive and negative slope, respectively. The current consumption is listed in Table 4.1.

Table 4.1. Bidirectional digital galvanic isolator current consumption.

Data Rate [Mb/s]	20	100	200	300
TX current [mA]	0.74	3.55	7.09	11.1
RX current [mA]	0.47	2.20	4.40	7.40

4.4.5 Results and Discussion

The galvanic isolator reaches stable unidirectional operation for the 150 MHz input control signal frequency that results in a 300 Mb/s data rate. In the bidirectional mode, the galvanic isolator achieves stable operation for the 68 MHz input control signal frequency resulting in a 136 Mb/s simultaneous data rate in both directions. The attained data rate is limited by the internal blanking circuit adapted for the oscilloscope probe measurement, which constrains the pulse widths provided by the outputs of the isolator. A higher frequency operation is expected in full integration designs.

The measured propagation delay does not even reach 5 ns, which represents an excellent value in comparison with contemporary galvanic isolator designs.

The CMTI measurement reveals greater sensitivity to common mode transients. The CMTI to the positive and negative slope amounts to 80 and 120 V/ns, respectively. These values are most likely limited by the external components and connections. Nevertheless, in order to attain greater CMTI values, a more complex coding must be implemented.

The measured current consumption at 100 MHz, representing 200 Mb/s, amounts to 7 mA on the transmitter and 4.4 mA on the receiver when receiving. The receiver in the idle mode consumes less than 100 µA.

4.5 Analog Galvanic Isolator

The aim of this design is to find a replacement of the standard opto-coupler employed in typical isolated flyback applications. Such approach is highly suitable for the full module integration of the primary and secondary side controllers into the one single package.

4.5.1 Low Voltage Die

The schematic diagram of the low voltage die bearing the operational transconductance amplifier, modulator and transmitter is depicted in Fig. 4.9. The transmitter and its connection is identical to the one utilized in the bidirectional isolator in Section 4.4.

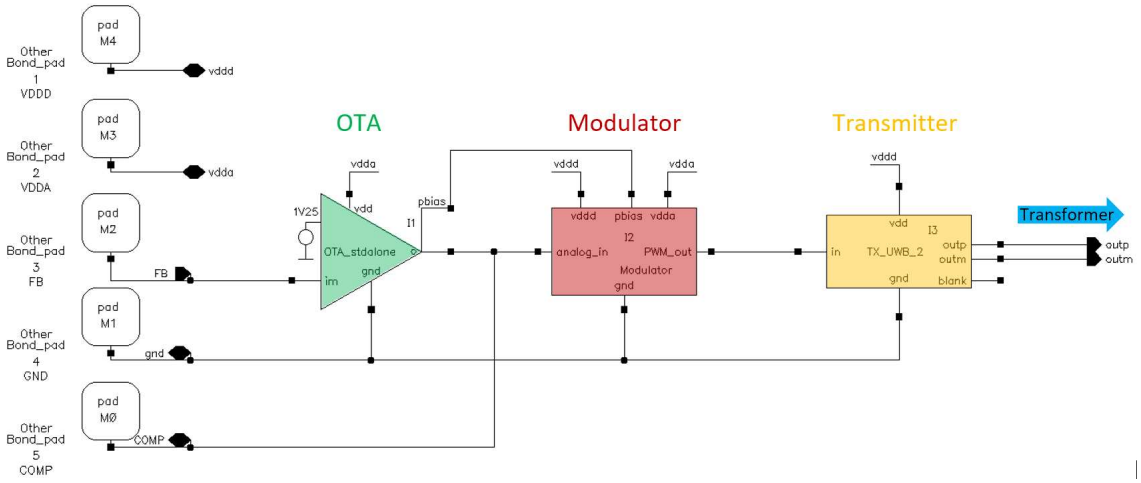

Fig. 4.9. Schematic diagram of low voltage die.

4.5.2 Operational Transconductance Amplifier and Modulator

The 1.25 V reference and the FB feedback voltages are applied to the positive and negative inputs of the OTA, respectively. The input terminal of the modulator senses the COMP voltage and compares its value with the voltage provided by a sawtooth wave generator, thus the modulator encodes the COMP voltage value into the PWM signal, as illustrated in Fig. 4.10. The generated PWM signal is transmitted to the high voltage die in a fashion similar to the bidirectional isolator in Section 4.4.

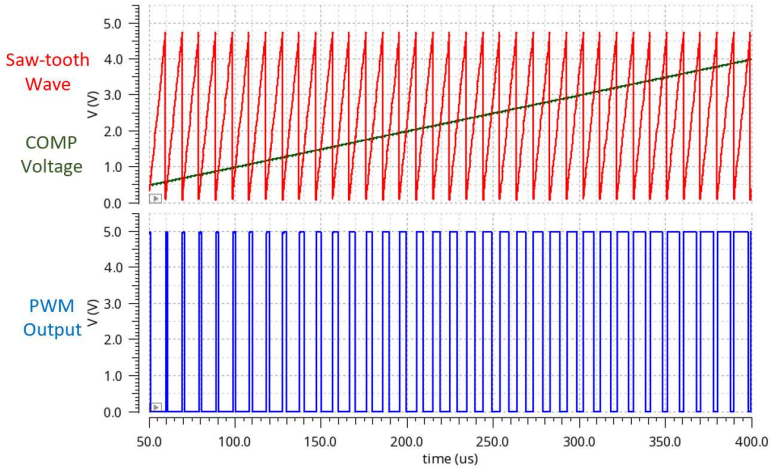

Fig. 4.10. Encoding of COMP voltage value into PWM signal.

4.5.3 High Voltage Die

The schematic diagram of the high voltage die, depicted in Fig. 4.11, utilizes the identical receiver and current reference designs as the bidirectional isolator discussed in Section 4.4. The positive and negative output of the receiver is connected to the set and reset terminal of the RS flip-flop, respectively, thus the PWM signal representing the analog COMP value is obtained on the output of the RS flip-flop.

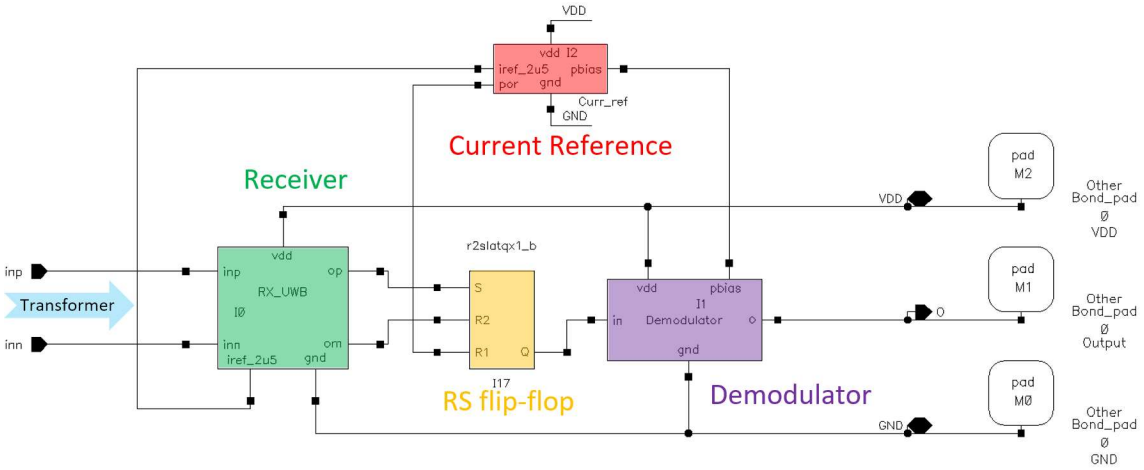

Fig. 4.11. Schematic diagram of high voltage die.

4.5.4 Demodulator

The demodulator decodes the PWM to analog COMP voltage and provides that value to the output of the high voltage die.

4.5.5 Evaluation of the Analog Galvanic Isolator

The analog galvanic isolator has been prototyped and encapsulated in the same manner as the bidirectional digital isolator illustrated in Fig. 4.4. Two sets of tests have been performed to evaluate the modulation, transmission and demodulation of an analog signal:

- Transmission of a sine wave applied on the COMP terminal,
- employment of the design in the real isolated flyback application.

The carrier frequency of the modulator has been set to 100 kHz as a compromise value between the resulting time constant of the isolator system and power consumption. The measured current consumption at 100 kHz amounts to approximately 60 µA on the transmitter side, which represents a significantly lesser value in comparison with the standard opto-coupler designs that require current in the order of mA. The receiver side current consumption amounts to 90 µA, which also does not exceed the current consumption of the designs utilizing the opto-couplers.

Fig. 4.12 illustrates the measured response to sine wave signals applied on the COMP terminal. The aim of this test was to evaluate the phase angle between the input and output sine wave signals. The measured time delay amounts to approximately 17 µs, which corresponds with the 7.4 kHz pole. Such value is sufficiently high not to affect the feedback loop stability of the typical flyback converter.

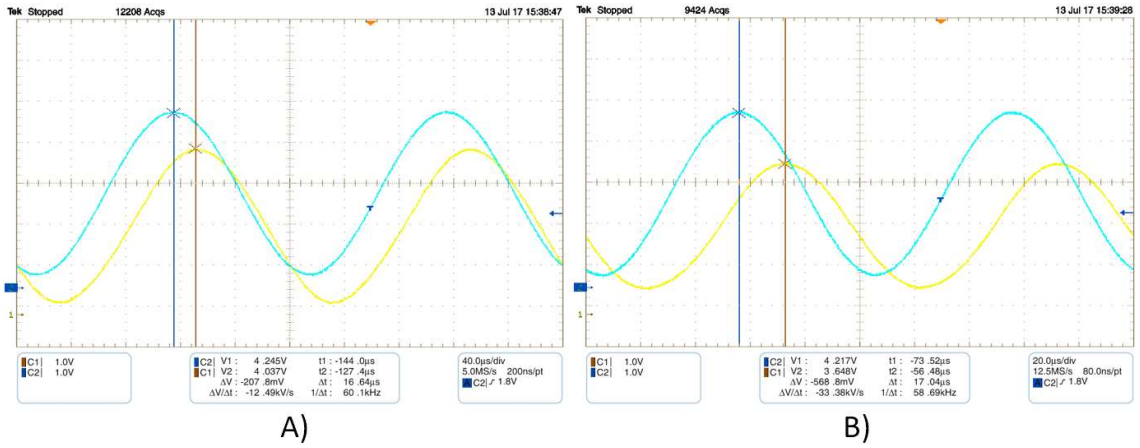

Fig. 4.12. Measured response to sine wave signal applied on the COMP terminal. Blue – COMP input, yellow – demodulator output. Waveforms are averaged. A) 5 kHz. B) 10 kHz. Measured time delay amounts to 17 µs.

In the final test, the analog galvanic isolator was inserted into the typical flyback converter design employing the NCP1234 controller [10], depicted in Fig.4.13.

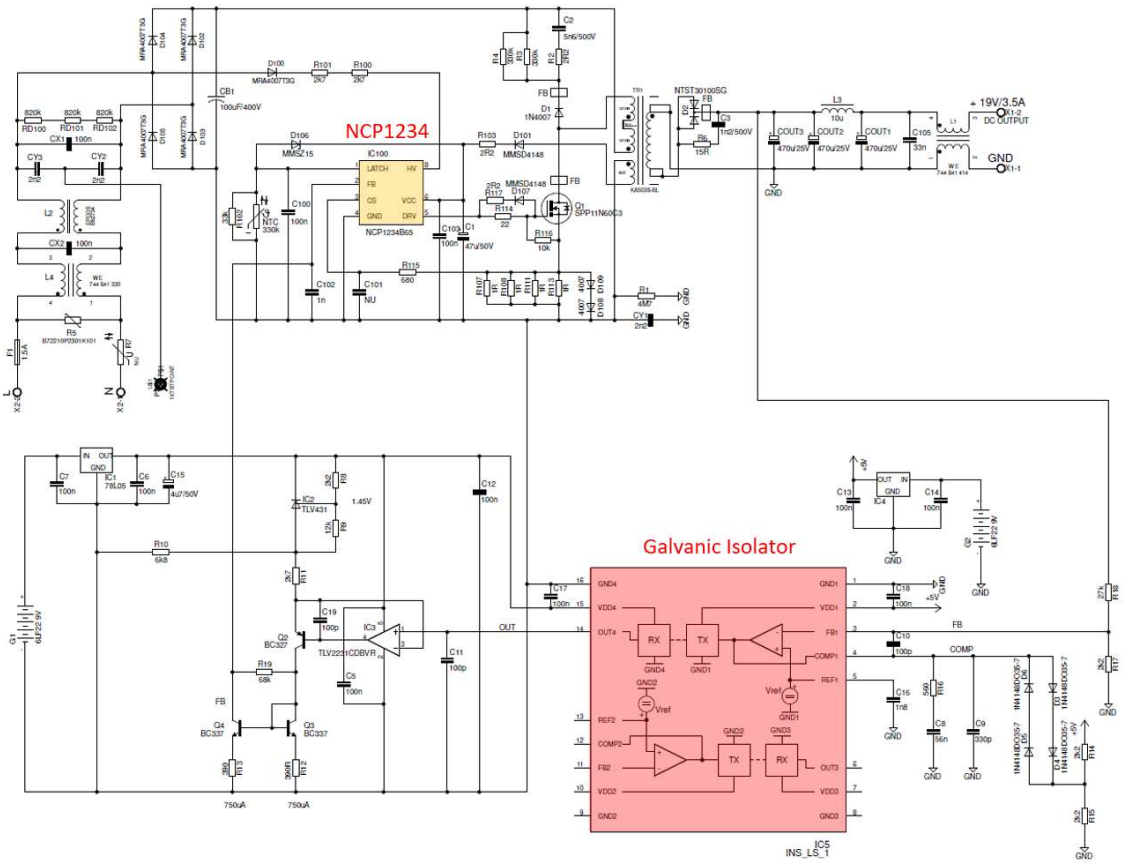

Fig.4.13. AC-DC converter application utilizing analog galvanic isolator.

The load step response from 100 mA to 1.5 A of the AC-DC flyback converter utilizing the analog galvanic isolator is depicted in Fig.4.14. As may be seen from the waveforms, the analog isolator replaces the opto-coupler adequately. The controller provides a stable step response from light to full and full to light load conditions.

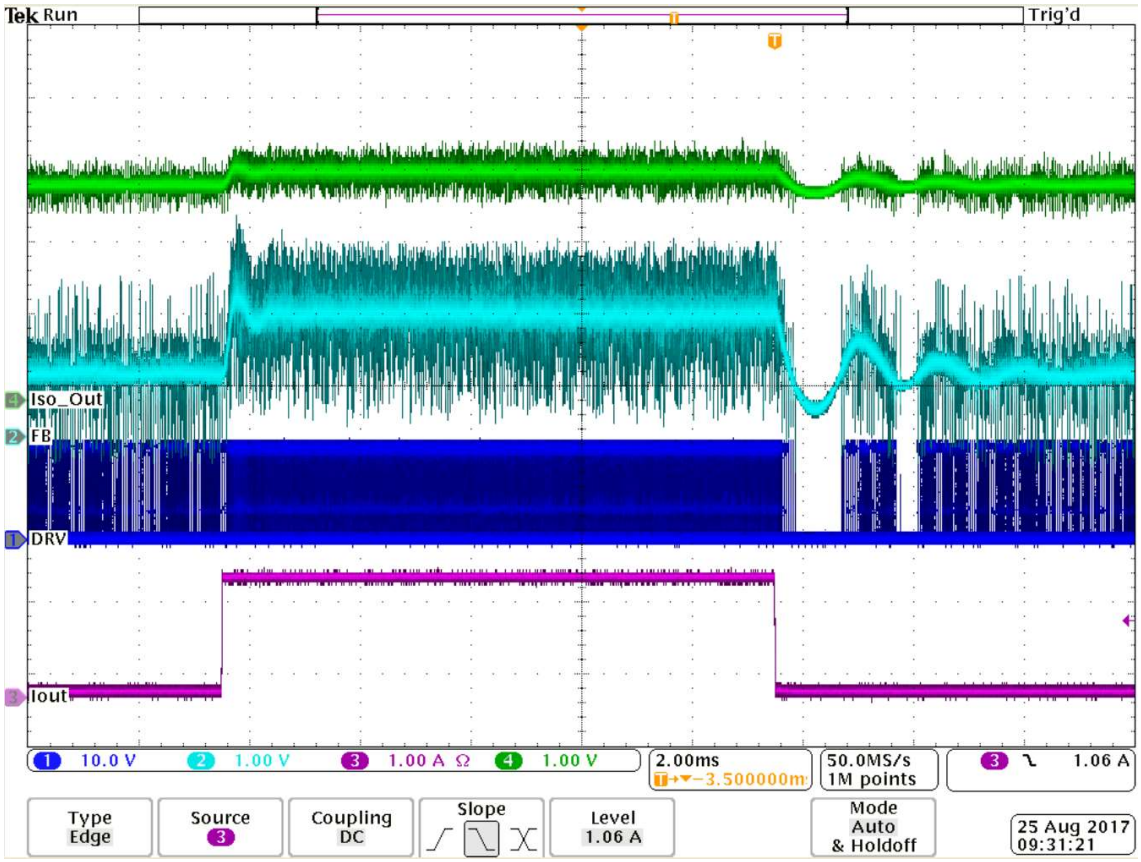

Fig.4.14. Measured waveforms of AC-DC flyback converter application utilizing the opto-coupler replacement – load step response. Green – demodulator output, cyan – FB terminal of NCP1234, blue – DRV terminal of NCP1234, violet – load current.

4.5.6 Results and Discussion

The analog galvanic isolator is a part of the subsequent design stemming from the bidirectional galvanic isolator. The analog isolator has been tested in real AC-DC converter application as a replacement of the standard opto-coupler. A stable step response, from the light (100 mA) to full (1.5 A) and full to light load conditions, has been achieved. The bandwidth of the analog galvanic isolator is reduced by the introduction of an extra pole, whose frequency is directly given by the carrier frequency modulating the analog signal. In the discussed flyback application, the 100 kHz carrier frequency has been utilized, thereby achieving the 7.4 kHz pole. Such value is comparable to the frequency of an extra pole introduced by the standard opto-coupler, thus is adequate for the typical flyback applications. For applications requiring a higher pole frequency, the carrier frequency must be increased. The measured current consumption at 100 kHz amounts to approximately 60 µA on the transmitter side, which represents a significantly lesser value in comparison with the standard opto-coupler designs that require current in the order of mA. The receiver side current consumption amounts to 90 µA, which also does not exceed the current consumption of the designs utilizing the opto-couplers.

5 CONCLUSION

1) Design of 800 V Galvanically Isolated Translator

The first aim of this Thesis was to design a galvanic isolation suitable for HV applications that require either measuring high voltages or communicating between different voltage domains. The development was divided into two consecutive steps:

- Design of the galvanically isolated translator.
- Design of the galvanically isolated HB driver for industrial applications.

The design of the galvanically isolated translator was divided into three basic blocks:

- Transmission line,
- transmitter,
- receiver.

Transmission Line
Instead of the typical vertical transformer or a high voltage capacitor, the proposed method utilizes lateral on-chip spacing between resonant structures to provide galvanic isolation. In order to achieve low signal attenuation, all transmission line components, such as the adjacently coupled resonators, have been tuned precisely to the same resonant frequency using extra test structures:

- Capacitor value skews of the coupled resonators.
- Reduced transmission line with one coupled resonator removed.
- Transmitter generating pulse bursts.
- Transmitter generating continuous signal.
- Receiver outputting digital signal.
- Receiver outputting analog signal corresponding to received signal strength.

To the best of the author's knowledge, this case of CMOS lateral resonant coupling being utilized and investigated in chip-to-chip communication is yet unprecedented. This technique has been proved as a viable way to increase the maximum achievable isolation rating in fully-integrated CMOS galvanic isolation designs.

Transmitter
In order to avoid the need of using extra on-chip inductors, the transmitter oscillator was connected directly to the first coupled resonator of the transmission line. The oscillator frequency was tuned to the resonant frequency of the adjacently coupled resonators.

Receiver
A completely novel design of an RF detector featuring very low stand-by current consumption and high sensitivity has been introduced by the author of this Thesis.

Communication through the Galvanically Isolated Translator
The galvanically isolated domains communicate with each other via the means of digital signals. For that purpose, two AC carrier techniques relying on modulation and demodulation have been utilized:

- OOK, and
- PWM.

The OOK digital modulation seemed a sensible candidate for high-bitrate applications. For low power applications, the PWM communication has been selected.

Design of Galvanically Isolated Half Bridge Driver for Industrial Applications
The galvanically isolated half bridge driver for industrial applications has proved itself a viable target application for the galvanically isolated translator utilizing lateral resonant coupling. Two parts of the half bridge driver have been designed:

- Low voltage die employing the transmitter,
- high voltage die employing the receiver.

The presented design of the half bridge driver amply satisfies the industrial application requirements such as high negative transient immunity and high CMTI.

2) Design of GI Translator for HV Applications Complying with the Safety Standards

In order to achieve as high galvanic isolation level as possible, the second goal set by this Thesis was the design of a galvanically isolated translator utilizing two vertical transformers connected in series. Although a communication scheme similar to the one utilized for lateral coupling may be employed, the UWB pulse polarity modulation has been utilized instead, enabling a high data rate, low power and low propagation delay communication through the isolator. The core of the receiver design, developed for the lateral coupling in the first phase of this work, has also been employed in the UWB receiver. In order to evaluate this concept, two structures have been designed:

- Bidirectional digital galvanic isolator, and
- analog galvanic isolator.

The design of the bidirectional digital isolator reliably allows using only a single galvanic isolator for communication in both, low-to-high and high-to-low, directions. This approach greatly reduces the area consumed by the isolator.

The analog galvanic isolator was introduced as a part of the subsequent design stemming from the bidirectional galvanic isolator. The analog isolator has been tested in a real AC-DC converter application as a replacement of the standard opto-coupler. This design enables full integration of primary and secondary side controllers in a single package, thereby reducing the complexity and cost of the AC-DC converters.

Future Work

The current consumption of the transmitter in the galvanically isolated translator must be optimized in the future design. The 2.8 GHz oscillator frequency seems to be a boundary value for the 5 V MOSFET transistors available in the ONC25BCD process, resulting in high current requirements of the oscillator. Another fabrication process providing transistors featuring higher transit frequency must be selected.

The GI translator for HV applications must be proven in target applications. Sensible candidates are:

- The half bridge driver, and
- AC-DC primary side controller integrated with the secondary side controller in a single package.

6 BIBLIOGRAPHY

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1993 – 1999	Gymnasium Rožnov pod Radhoštěm

PUBLICATIONS

PANKO, V., BANAS, S., PTACEK, K., BURTON, R., DOBES J., "An Accurate DC and RF Modeling of Nonlinear Spiral Polysilicon Voltage Divider in High Voltage MOSFET Transistor," in *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Xi'an 2012, 2012.

M. JAVID, R. BURTON, K. PTACEK and J. KITCHEN, "CMOS integrated galvanically isolated RF chip-to-chip communication utilizing lateral resonant coupling," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, 2017.

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US PATENTS

10,432,098	Switching device control with second assertion of drive signal during conduction phase
10,411,086	High voltage capacitor and method
10,270,440	Output driver having pull-down capability
10,097,097	Method and apparatus for self-synchronization of a synchronous rectifier
10,063,154	Current sense detection for synchronous rectification
10,050,541	Synchronous rectifier control with second assertion of drive signal during conduction phase
10,008,457	Resonance-coupled signaling between IC modules
9,973,091	Precise and dynamic control of synchronous rectification switch voltage in a switched mode power supply
9,954,523	Receiver for resonance-coupled signaling
9,837,916	Method and apparatus for synchronous rectifier
9,594,099	Method of and circuit for brown-out detection
9,013,898	Synchronous rectifier controller, power converter using same, and method therefor
8,786,297	Method of and circuit for brown-out detection
8,711,582	Parasitic element compensation circuit and method for compensating for the parasitic element
8,710,804	Discharge circuit and method
7,956,651	Method for detecting a current and compensating for an offset voltage and circuit
7,800,456	Method of forming an oscillator circuit and structure therefor
7,688,052	Charge pump circuit and method therefor
7,564,704	Method of forming a power supply controller and structure therefor

SELECTED IC PRODUCTS

NCP5181, NCP5104, NCP5106, NCP5109, NCP5111, NCP5304	High Voltage High and Low Side Driver
NCP51820	High Speed Half-Bridge Driver for GaN Power Switches
NCP4303, NCP4304, NCP4305, NCP4306	Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies
NCP107x and NCP106x family	High-Voltage Switcher for Low Power Offline SMPS
NCP1392, NCP1396, NCP1398	High-Voltage Half-Bridge Driver with Inbuilt Oscillator
NCP1631	Interleaved, 2-Phase Power Factor Controller
NCP1937	Combination Power Factor Correction and Quasi-Resonant Flyback Controllers for Adapters

RESEARCH ACTIVITY

Design of monolithic high voltage devices

Design of high voltage ESD protections

Communication between galvanically isolated high voltage and low voltage parts of an integrated circuit

ABSTRACT

This Thesis introduces a novel lateral resonant coupling technique and discusses the design of an 800 V galvanically isolated translator which is subsequently utilized in the 800 V half bridge driver for industrial applications. The fabrication cost of this design is lesser in comparison with the currently widespread galvanically isolated translators. For applications that require a higher level of galvanic isolation, a follow-up development of the galvanically isolated translator is presented. This design utilizes a single galvanic isolator for communication in both, low-to-high and high-to-low, directions, which greatly reduces the area consumed by the isolator. As a part of the subsequent design, a galvanic isolator transmitting an analog value is introduced. The analog isolator has been tested in a real AC-DC converter application as a replacement of the standard opto-coupler. This design enables full integration of primary and secondary side controllers in a single package, thereby reducing the complexity and cost of the AC-DC converters.

ABSTRAKT

Tato dizertační práce představuje novou techniku laterární rezonanční vazby, která je využita v návrhu galvanicky izolovaného posouvače úrovně, který je následně implementován v 800 V půlmůstkovém kontroléru pro průmyslové aplikace. Ve srovnání s tradičními galvanickými izolátory jsou výrobní náklady tohoto řešení nižší. Pro aplikace vyžadující vyšší úroveň galvanické izolace je popsán následný vývoj galvanicky izolovaného posouvače úrovně, který využívá pouze jeden galvanicky oddělený posouvač úrovní pro komunikaci v obou směrech, což výrazně snižuje plochu struktury izolátoru. Jako součást následného návrhu je představen galvanický izolátor který je schopen přenášet analogovou hodnotu napětí. Analogový izolátor byl testován v reálné aplikaci síťového spínaného zdroje jako náhrada standardního optočlenu. Tato konstrukce umožňuje integraci primárních a sekundárních obvodů v jednom pouzdře, což umožní snížit složitost a cenu spínaného zdroje.