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DEVELOPMENT OF ACTIVE DEVICES AND DESIGN OF UNCONVENTIONAL CIRCUITS FOR APPLICATIONS IN SIGNAL GENERATION, PROCESSING, SENSING AND MEASUREMENT

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
DEPARTMENT OF RADIO ELECTRONICS

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VÝVOJ AKTIVNÍCH PRVKŮ A NÁVRH NEKONVENČNÍCH OBVODŮ A APLIKACÍ PRO GENEROVÁNÍ A ZPRACOVÁNÍ SIGNÁLŮ ZE SENZORŮ A MĚŘENÍ

A THESIS OF A TALK FOR THE PROFESSORIAL APPOINTIVE PROCEDURE
IN THE STUDY FIELD OF ELECTRONICS AND COMMUNICATIONS

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KLÍČOVÁ SLOVA

Aktivní prvky, analogové obvody, CMOS, elektronické ladění, filtry, fraktální obvody, oscilátory, rozsah přeladění, sensory.

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CONTENT

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The author graduated from the three-year Bachelor programme and the two-year Master's programme (with honours) both at the Faculty of Electrical Engineering and Communication (FEEC), Brno University of Technology (BUT) in the field of Electronics and Communication. He obtained a rector's award for results in study and representation of university (EEICT conference and competition) in 2008. He finished his Ph.D. study in 2012 in the same field. He also attended additional pedagogical courses (accredited) at Lifelong Learning Institute of BUT Brno (Institut celoživotního vzdělávání) from 2011 to 2012. He served at the dept. of Radio Electronics as a research worker (junior and senior scientist at the SIX center) from 2012 to 2020. Between 2016 and 2020, he has also been involved in several research projects at the dept. of Telecommunications. He serves as associate professor (from 2017) and received an academic position in 2021 at the dept. of Radio Electronics. His scientific and pedagogical activities are focused on analog and mixed-signal electronic circuits and analog signal processing.

Research and development activities of the author concentrate on basic research areas (projects of the Czech Scientific Foundation) as well as projects of applied research (within the framework of the FP-7 project or COST projects) of the European Union solved at his workplace). He works in areas of advanced active elements with multi-parameter control and their applications (generators of signals, filters, complex analog and mixed systems, etc.) intensively. He pursues modeling and development of active devices in CMOS technologies available at the workplace. His team has developed 5 integrated circuits in 0.7, 0.35 μm and 0.18 μm technologies allowing modular assembling of different advanced active elements of multi-terminal arrangement. These results were obtained within the framework of the Czech Scientific Foundation and Czech Ministry of Education projects. He is author and co-author of 12 functional prototypes. The author publishes his research results in renowned international scientific journals in the field of electronics and communication and at international conferences (publication activities in accordance to Web of Science: 103 papers in journals with impact factor/ 59 as first author; 106 papers in proceedings of international conferences/ 50 as first author; 924 citations without autocitations; h-index: 22). He also serves as reviewer for many journals and conferences (also as conference programme committee member) and as member of editorial boards of several scientific journals (Radioengineering, IEEE Transactions on Instrumentation and Measurement, MDPI Sensors). He received rector's awards for 10th and 3rd place in the university competition Top 10 Excellence VUT in 2012 and 2013 respectively (evaluated for 2011 and 2012 in the category "Ph.D. publications").

Pedagogical activities of the author are focused on practical education (computer and laboratory exercises in the courses Electronic Circuit Theory, Analog Electronics, Design of Analog Filters, and High-frequency Circuits). He serves as lecturer of selected topics in the courses Electronic Circuit Theory, Design of Analog Filters and High-frequency Circuits. He has been guarantor of Electronic Practice and Analog Electronics courses. He is a member of the advisory board of the doctoral (Ph.D.) study programme Electronics and Communication and the master (M.Sc.) study programme Telecommunications. He supervised 47 successfully defended final master's and bachelor's theses, one Ph.D. thesis, and 8 contributions of students at the EEICT conference and competition.

1 INTRODUCTION

Modern communication systems always require strong and reliable analog subparts because full digital processing in whole blocks of a communication chain is not possible in many cases (too high frequencies, unsubstantially high power consumption and robustness of digital parts, economic reasons, etc.). The analog signal processing parts belong to a fundamental principle of current as well as future electronic systems. A complete digital solution of the system is suitable only for specific cases or even impossible. We have to also consider drawbacks of digital parts (certain processing delay and inability to react to changes in the system immediately) when a complex system is designed. The digital solution cannot be always totally appropriate and optimal if a simpler, cheaper and sufficient analog way exists. Sustaining research interests of many workers and scientists all over the world in various topics of analog signal processing illustrates the high importance of this field in practice. These activities are spread into various areas (classic circuit theory and synthesis, fractional-order circuits and systems, development of active devices, application in communication, sensing, measurement methodology, and many others). Analog processing incudes amplification, filtering, generating, mixing, shaping, etc. of signals in almost all electronic devices. Many unsolved questions are open for further research as well as being very important to introduce newly obtained results to students because these approaches should be disseminated among the modern technical society of young workers, designers and experts in the field.

The current development of active elements as fundamental parts of communication and signal processing systems has strong motivation due to drawbacks of standard devices (operational amplifier for example) for advanced performances allowing simple electronic adjustment (control) of application and simplified design of unconventional topologies [1], [2], [3]. Some discussion about the organization and basic principles of electronic adjustment has been given for example in [4]. This work covers examples of solutions performing externally driven (adjusted) parameter(s) of an active device serving for tunability and adjustability purposes of designed blocks and parts of complex systems.

This thesis focuses on several topics solved in the last 5 years. These fields of analog signal processing target methodologies for tunability and the adjustability range of the parameters extension, design of fractional-order circuits and elements, and methods for processing and distribution of sensed information from closed environments (for example agricultural cultivation reservoirs, hydroponics, etc.). The following sections introduce several selected typical examples of developed solutions. The following section briefly introduces the proposed and designed active elements (cells) fabricated in several CMOS processes of integrated circuits (ICs). These application specified integrated circuits (ASICs) are key parts of many presented solutions in this work. The first topic deals with examples of circuits profiting from extended tunability range in the field of filters, oscillators and active capacitance multipliers. The second topic discusses interesting fractional-order circuits and systems employing benefits of non-integer approaches for the design of variable-order two port (integrator/differentiator), special phase shifter and adjustable immittance generation. The third topic covers applications of the developed integrated devices for sensing and distribution (transmission) purposes and measuring systems operating at the boundaries of two environments.

2 DEVELOPMENT OF ACTIVE DEVICES

Our research team developed several ASICs including special active elements for efficient implementation in various conventional and unconventional analog applications from elementary circuit synthesis and development of new solutions of active filters, oscillators, nonharmonic generators, signal shapers, detectors, etc. up to complex systems where these active elements serve in several functional blocks (parts of the processing chain). The following text discusses the most useful fabricated devices used for the majority of published results in recent years. Design and fabrication of chips received founding from the Czech Scientific Foundation. The presented examples are selected because further application-focused sections show employment of these or very similar devices directly in discussed systems.

Five different active cells, available in a single DIL28 package, were designed for the modular approach [5] of advanced active elements within the framework of the Czech Scientific Foundation project "Research for electronically adjustable advanced active elements for circuit synthesis" in 2016. This IC has been fabricated in 0.35 μm I3T25 3.3 V ON Semiconductor (formerly AMIS) process. On-chip available devices are still useful for further research activities and experimental verifications in many recently published works and present activities. Figure 2.1 shows content of the IC by symbolical representation of available active elements (each active element = single cell of IC). These symbols also explain the fundamental principle of each element. The fabricated device includes two voltage multipliers (multiplication of two differential voltages) with a current output terminal (abbreviated as MLT). To the best of the author's knowledge, a similar device is not commercially available yet. Two multipliers were intended due to different behavior of a fully CMOS based solution in comparison with bipolar transistors Gilbert's core based solution [6], [7]. Implementation of the selected input pair of voltages as driving (DC) creates a linearly adjustable Operational Transconductance Amplifier (OTA) [1]. The IC package also includes a Voltage Differential Difference Buffer (VDDB) for a simple solution of the mathematical operation of summation and subtraction (with unity gain). The necessity of many current output terminals for synthesis of current-mode circuits [8] led into the design of Current Controlled Current Conveyor of second generation (CCCII) [1]. Inter-terminal relations are also indicated in Fig. 2.1. The adjustable resistance of current input terminal X represents a very useful feature for adjustable circuits and applications. The prototype of an electronically adjustable Current Amplifier (CA) was designed for very good linearity of the DC transfer response. Further details, topological internal schemes and performances of fabricated cells are available in [9]. In total, four from all five cells have a single adjustable parameter (single degree of freedom). Two degrees of freedom are available when two of these devices are connected together based on the modular approach [5] that creates very interesting advanced active devices for further applications. The modular approach suggests to interconnect simple active devices (performing adjustable feature) into complex units allowing multi-parameter controllability/adjustability and multi-terminal transfer relations [5]. The example of modular approach-based generation of an active device was also introduced in [9] where interconnection of three of these cells (two MLTs and CCCII) is shown together with a very interesting application in an electronically (voltage) tunable quadrature oscillator. The device is called a Current Controlled Voltage Differencing Current Conveyor Transconductance Amplifier (CC-VDCCTA) and its principle with final application is shown in Fig. 2.2. Figure 2.3 illustrates the top-layout design of the final product.

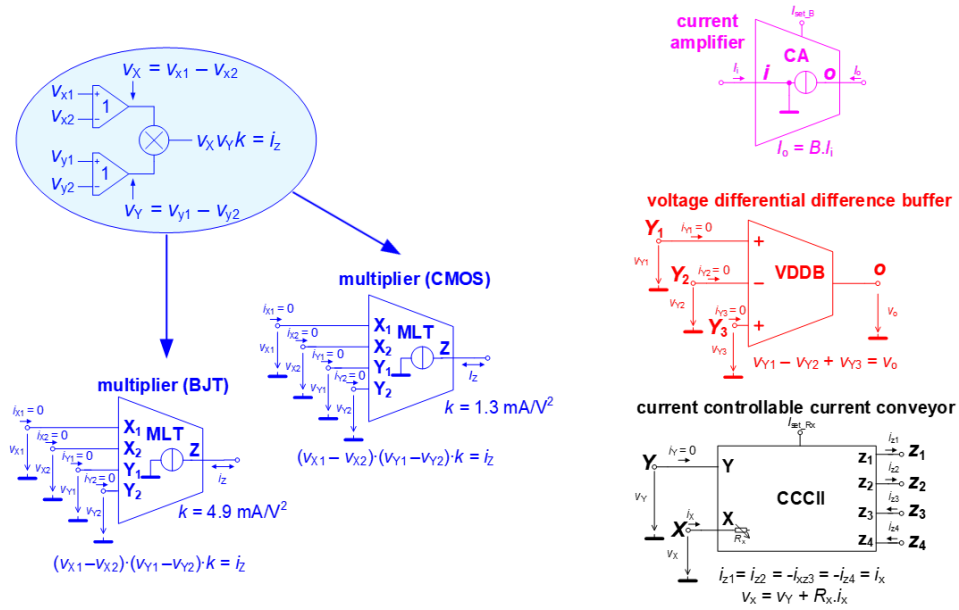


Fig. 2.1 Symbols of active elements/cells in fabricated IC (0.35 μm I3T ON Semiconductor process) and their fundamental principle expressed by inter-terminal relations

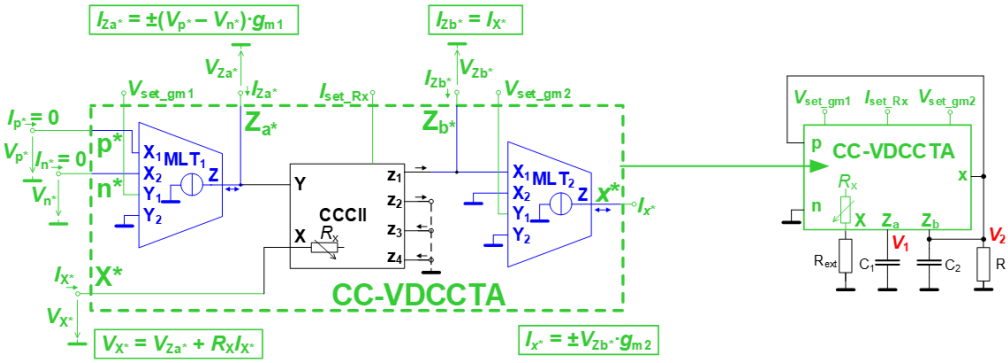


Fig. 2.2 Example of interconnection of partial elements (modular approach) for a complex active device and application in an electronically tunable oscillator.

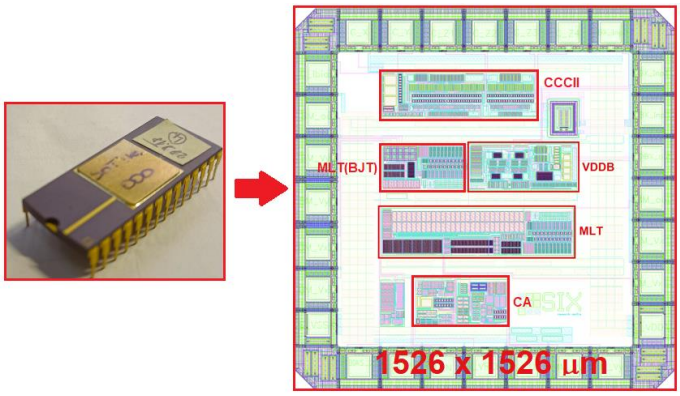


Fig. 2.3 Package and top-layout of fabricated IC including five different active elements/cells (0.35 µm I3T ON Semiconductor process)

The requirement for different applications and further (speed/bandwidth especially) performances were reasons for designing cells using modern 0.18 µm Taiwan Semiconductor Manufacturing Company (TSMC) 1.8 V process within the framework of the Czech Scientific Foundation project "Active elements with differential ports for design of original non-differential and pseudo-differential functional blocks" in 2017/18. There are also MLTs and conveyors available but different (smaller in transistors size as well as level of supply voltage compared to the I3T process) technology required to complete the redesign of these blocks in different topologies and aspect ratios of transistors. The multiplier was created completely using CMOS solution and a second (inverted) current output terminal added. The dynamics and linearity of fabricated cells decreased (about ±200 mV of input level) but speed and bandwidth increased (more than 80 MHz). Cells using the I3T process [9] have bandwidth up to 40-50 MHz and input dynamics at least ±500 mV. The internal topologies of important active elements integrated on the IC (TSMC process) were presented partially in [10]. The project "Deterministic, chaotic and stochastic phenomena in the sub-micron integrated structures" supported fabrication of improved MLTs for modeling and experiments with chaotic systems. Packages (DIL40) including five MLTs were delivered from a producer (TSMC and IMEC Belgium) in 2021. The internal topology of the novel and redesigned MLT together with symbol and basic ideal principle is given in Fig. 2.4. Figure 2.5 shows the top-layout of the fabricated IC and detail of the single MLT cell. All further details can be found in [11] and [12].

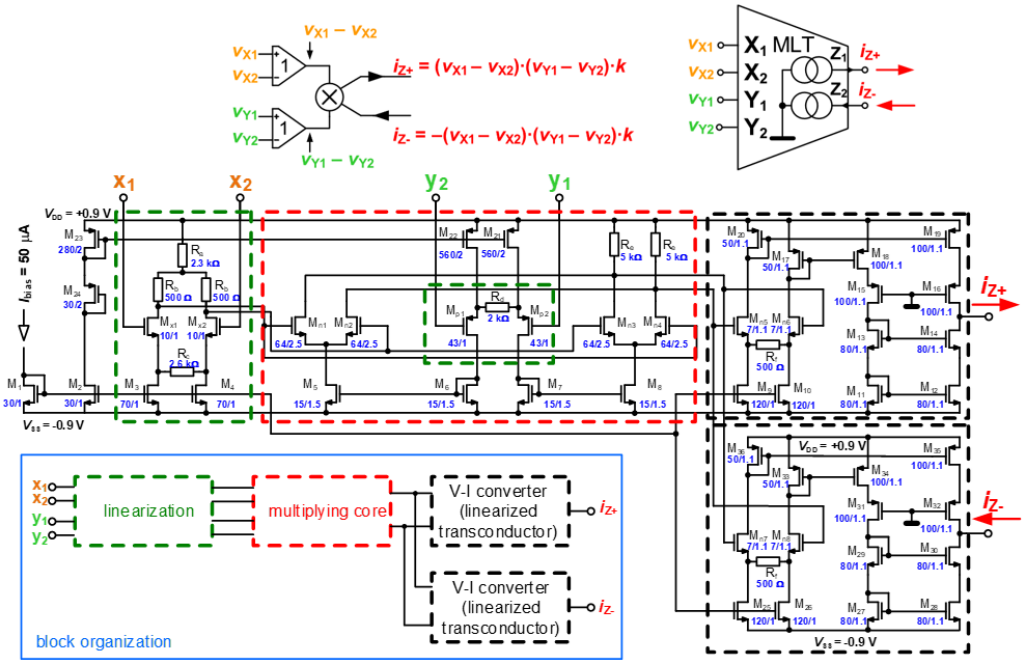


Fig. 2.4 Operational principle, symbol and internal topology of double output CMOS MLT designed and fabricated using 0.18 μm TSMC process

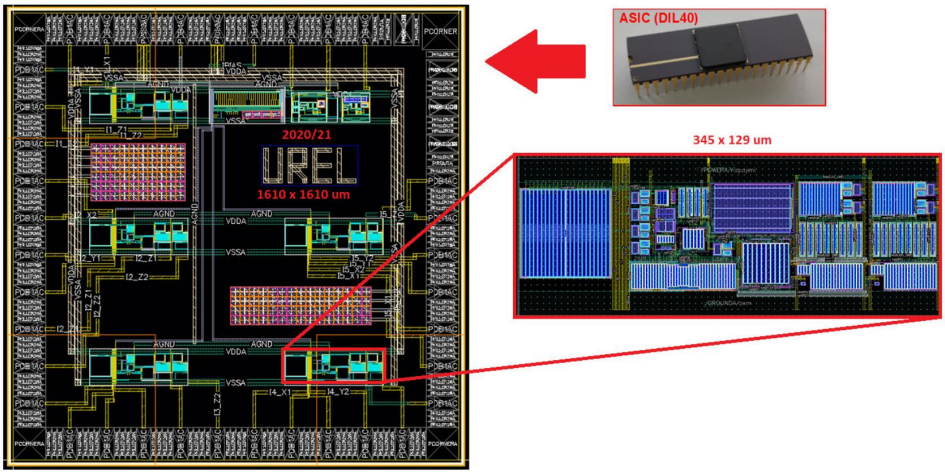


Fig. 2.5 Package, top-layout and cell layout of MLT (0.18 μm TSMC process)

3 TUNABILITY AND ADJUSTABILITY RANGE EXTENSION

Decreasing supply voltage means certain limitation for tunability and adjustability ranges of the designed circuits and systems. Therefore, efforts of researchers concentrate on searching for ways how to enhance the range of key parameters (features such as center frequency of filter, oscillation frequency, etc.) while the driving force range (DC voltage or current for adjusting parameters) remains still constant or decreasing range of driving force ensures unchanged range of tunability.

There are various methods (dependence of parameters on driving voltage, structural/topological modifications of circuit, etc.) how to reach the intended goal. The following text shows several developed examples.

3.1 ACTIVE FILTER

The simple single-purpose band-pass filter (BP) [13] in Fig. 3.1 has been designed and selected as a perfect example of application where tunability extension has clear reasons. This filter employs a differential voltage (unity gain) buffer (DVB) settable by the VDDB device discussed in Section 2, OTA and three passive elements. The center frequency of this filter can be tuned more than expected for standard cases. These adjustability extension features can be implemented also in multifunctional filters when similar approaches are used.

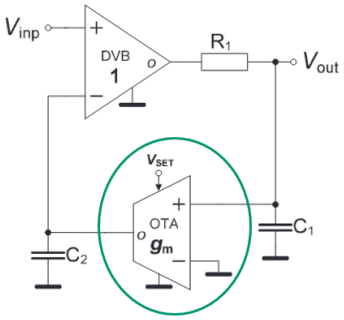


Fig. 3.1 Circuit topology of band-pass filter designed for experiments with center frequency tunability range

The tunability of the center frequency concentrates on a single parameter (transconductance g_m) of the transfer function:

$$K_{BP}(s) = \frac{V_{out}}{V_{inp}} = \frac{\frac{1}{R_1 C_1} s}{s^2 + \frac{1}{R_1 C_1} s + \frac{g_m}{R_1 C_1 C_2}}, \tag{3.1}$$

where center frequency ($\omega_C = 2\pi f_C$):

$$\omega_C = \sqrt{\frac{g_m}{R_1 C_1 C_2}}, \tag{3.2}$$

is adjusted without affecting the bandwidth of BP (quality factor is proportionally influenced by g_m) [13]. The lossless integrator formed by OTA and C_2 is tested with several cases of OTA solutions where these solutions have different dependences of g_m on the driving voltage V_{SET}. The first dependence utilizes linearly adjustable $g_m \sim V_{SET}$, then $f_C \sim \sqrt{(V_{SET})}$. It means square root adjustment of f_C. The second case implements g_m proportional to the square of V_{SET} ($g_m \sim V_{SET}^2$). It results in linear adjustment of f_C ($f_C \sim V_{SET}$). It is clear that increased power n of V_{SET} (V_{SET}^n) has an impact on dependence in accordance to $f_C \sim (V_{SET})^{n-1}$. However, it means increased complexity (number of active elements in cascade) that may encounter issues with limitation of dynamics vs gain and stability when the number of active elements is too high (high gain in the path). The last solution changes the type of dependence to exponential form by selection of a different type of amplifier in the OTA block. Transconductance now has the definition $g_m = 10^{2(VSET-1)}$ and furthermore, the center frequency shows exponential dependence on V_{SET}:

$$\omega_C = \frac{10^{(V_{SET\_A}-1)}}{\sqrt{R_1 R_2 C_1 C_2}}. \tag{3.3}$$

The following results compare the discussed dependences of center frequency on voltage V_{SET}. All design specifications, details and parameters are given in [13]. The magnitude responses are shown in Fig. 3.2 for all three cases in order to see differences in tunability range. Figure 3.3 compares all dependence of center frequencies on the identical range of V_{SET}. This voltage variation has not attained one decade (typical for low-voltage design) but the exponential dependence of f_C on V_{SET} allows almost one decade adjustment of f_C.

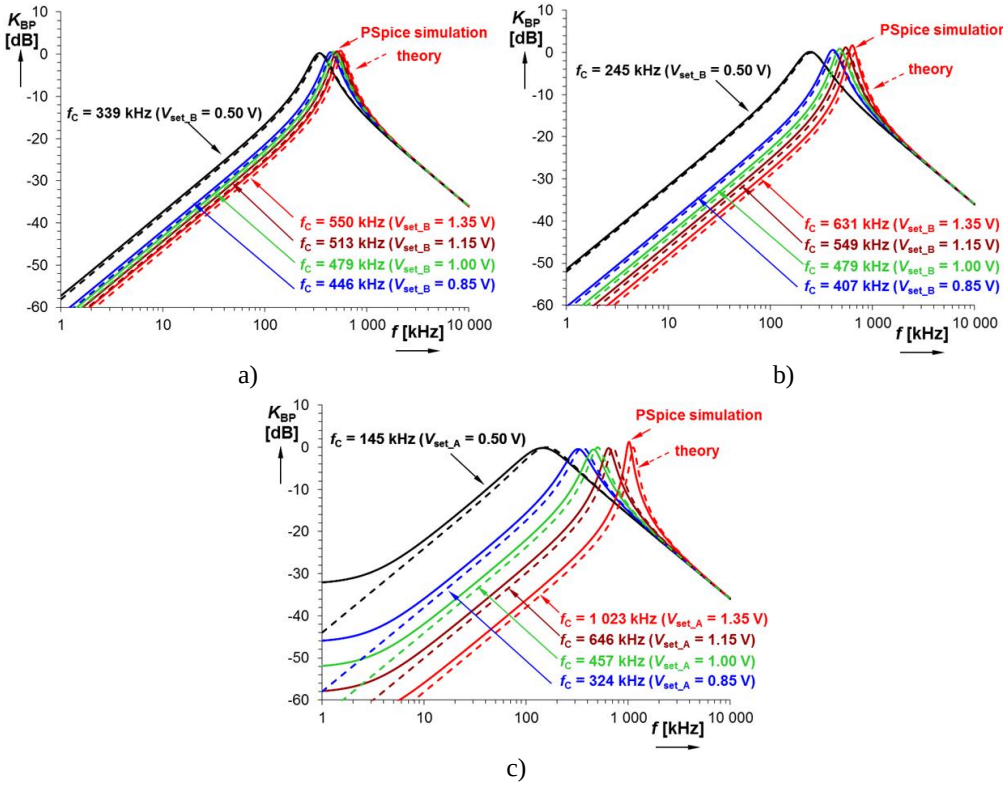


Fig. 3.2 Magnitude frequency responses of the BP filter for: a) square-root tuning, b) linear tuning, c) exponential tuning

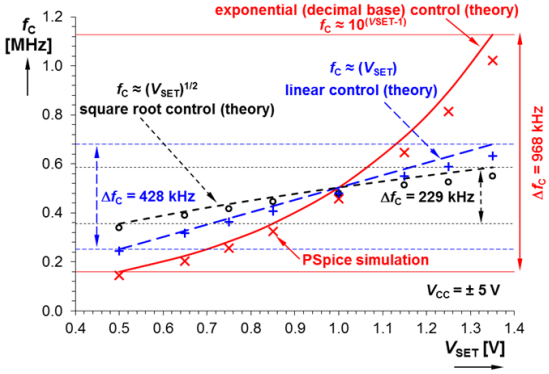


Fig. 3.3 Comparison of dependences of center frequency on V_{SET} for all three cases

3.2 OSCILLATOR

The extension of tunability range is useful also in the design of signal generators. Widely tunable harmonic oscillators have beneficial application in fields of communication and signal processing systems. The methodology used for extending tunable properties must be used properly and carefully because it is not so simple as in active filters. Inappropriate modification of loop gains in unsuitable circuit topologies causes principal variability of output level(s), i.e. voltage(s) in circuit nodes and then also increase of total harmonic distortion (THD) as well as issues with amplitude stability when frequency of oscillation (FO) is tuned. A solution presented in [14] shows this feature in a two-loop (of lossy and lossless integrator) based oscillator. The tunability of frequency targets to both loops consisting electronically adjustable time constants. These time constants are suitable for controllability enhancement by cascading electronically controllable negative current conveyors of second generation (ECCII-) [1], [2], [3] having adjustable current gain (B) between the X and Z terminal. The condition of oscillation (CO) adjustment (for automatic amplitude stabilization) is solved by a variable gain voltage amplifier (VA). The principle is depicted in Fig. 3.4. The specific circuit solution in Fig. 3.5 shows implementation of this principle (see organization of blocks indicated as $a_1 \ldots a_n$ and $b_1 \ldots b_n$). Based on the analysis in [14], the oscillation frequency can be expressed as:

$$\omega_0 = \frac{B^n}{\sqrt{R_1 R_2 C_1 C_2}} \,. \tag{3.4}$$

Note that this form of oscillation frequency requires simultaneous adjustment of n current gains B ($B_{a1} \cdot B_{a2} \ldots \cdot B_{an} = B_a^n$; $B_{b1} \cdot B_{b2} \ldots \cdot B_{bn} = B_b^n$; $B_a^n = B_b^n$). The relation between $B_{a/bi}$ and $V_{SETBa/bi}$ has a proportional character. These gains have quite low settable values (typically from tenths to low units) in presented ECCIIs. Then, limited dynamical ranges and nonlinear limitations of transfers in loops presents not such a significant issue when not so high n is selected. This circuit topology also generates constant amplitude levels in nodes 1 and 2 that are not influenced by the tuning procedure [14]. The example of dependences of oscillation frequency on driving voltage is shown in Fig. 3.6. The number n is the parameter of each trace. All information required for a further detailed study and design specifications are given in [14].

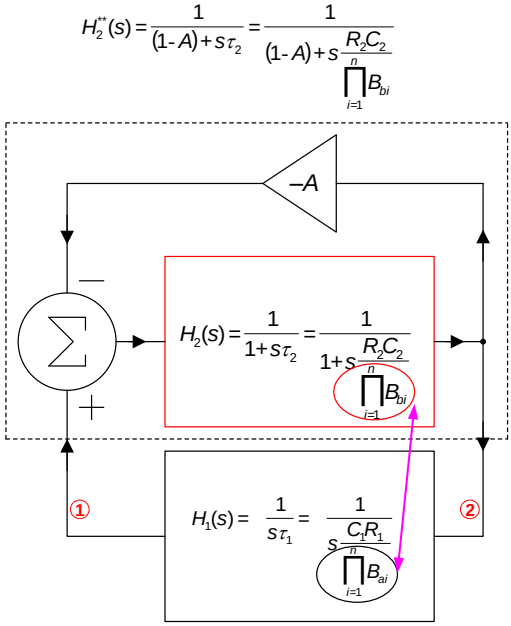


Fig. 3.4 Principle of time constant enhancement in a two loop-based autonomous system of an oscillator.

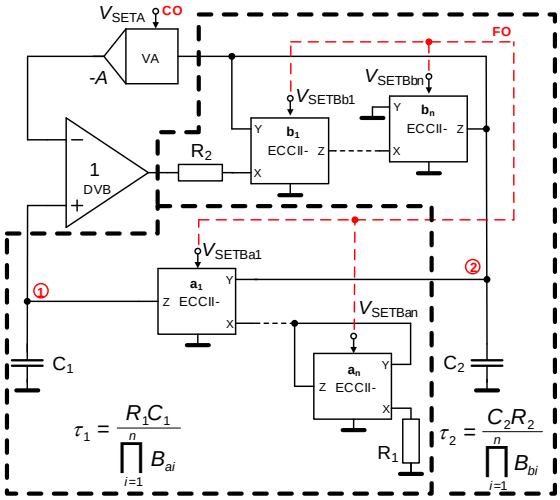


Fig. 3.5 The specific circuit solution corresponding to the principle in Fig. 3.4

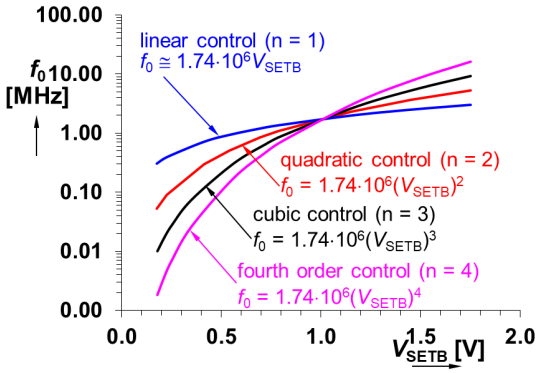


Fig. 3.6 Comparison of ideal dependences of FO of the oscillator on V_{SETB} for n = 1, 2, 3 and 4

3.3 CAPACITANCE MULTIPLIER

Electronically adjustable replacements of passive elements (that have no electronic adjustability) have an important role in the design of adjustable functional blocks as shown above. Moreover, some extreme values of capacitance and inductance are not available (or have large, bulky and heavy physical construction) without synthetic implementation [2]. The extension of a tunable range of a capacitance value was selected as a typical example where the discussed methodology can be beneficially used. Figure 3.7 shows the example of a capacitance multiplier using the above discussed elements (ECCII-) and DVB in the loop and a variable gain amplifier (with gain A) that serves for cancelling real losses caused by small-signal parasitic elements presented in the circuit topology [15]. The ideal input impedance of this circuit has form:

$$Z_{in}(s) = \frac{1}{sC_1 \prod_{i=1}^{n} B_i} \cdot \tag{3.5}$$

The real form respecting the most influencing parasitic elements (hatched resistors in Fig. 3.7) can be expressed as [15]:

$$Z_{in}{}'(s) = \frac{1 + sC_1 \left(R_o + R_{X1} - A \cdot R_{X1} \right)}{sC_1 \prod_{i=1}^{n} B_i}, \tag{3.6}$$

where a proper value of A allows to cancel the impact of parasitic resistances R_o and R_{X1} in nodes of the connected capacitor C_1. The purpose of n members of gains B is similar as in the previous case. Then the multiplication factor of capacity has a value determined by B^n (value of B adjusted simultaneously for all active elements). The generated total capacity (C_m) has a value adjustable in accordance with relation $C_m = C_1 \cdot B^n$. Construction details and setting of experiments are discussed in detail in [15]. The example of dependence of C_m on V_{SETB} for n = 1, 2, and 3 is presented in Fig. 3.8.

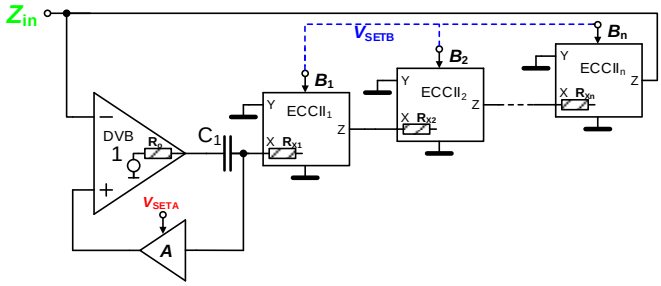


Fig. 3.7 Proposed capacitance multiplier with a large total capacity range

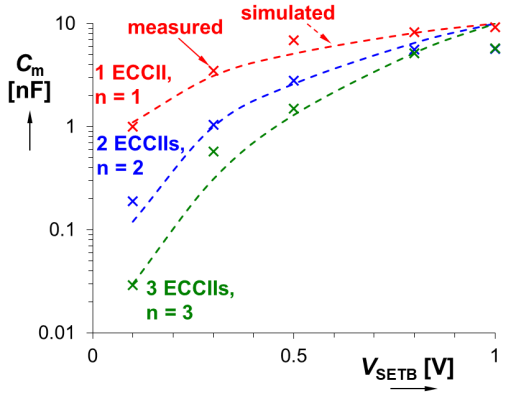


Fig. 3.8 Dependence of C_m on current gain B (V_{SETB}) for a variation of the number of ECCIIs in the structure (n = 1, 2 and 3)

4 FRACTIONAL-ORDER CIRCUITS AND APPLICATIONS

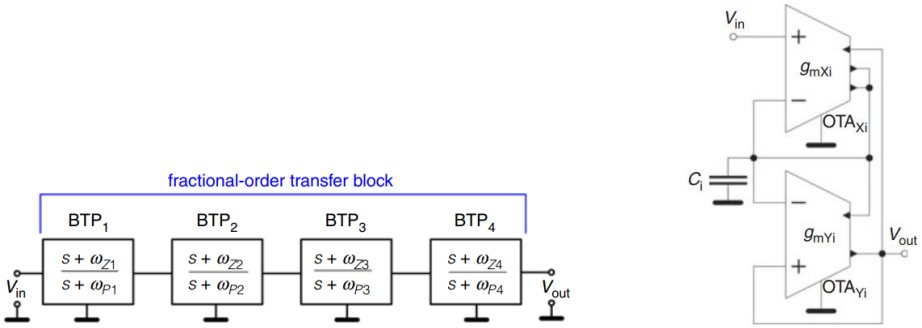
Non-integer (fractional) systems and behavior of the real world [16] brought many unanswered questions in recent years also to analog electronics and especially circuits synthesis, modeling and design. There are unconventional building blocks operating with fractional-order character required in the theory of control (see [10], [17], [18] and references cited therein), forming special impedances [19], [20], transfer blocks of special (non-standard) transfer responses (two-ports and multi-ports including integrators, differentiators and filters) [21], [22] and oscillators of specified phase shift (see [23] and references cited therein). Many of these circuits and structures are used for modeling real-world systems (matters, materials, tissues) [24]. Our team also contributed to this topic within the project "Synthesis of reliable electrical phantoms describing fractional impedance behavior of real-world systems (2019 – 2021)". The fractional-order immittances and transfer blocks can be created by two ways. The fractional-order behavior can be approximated by active circuits or by implementation of fractional-order passive elements (or their approximants) instead of integer-order elements in standard circuits.

4.1 FRACTIONAL-ORDER TRANSFER BLOCK

The example of a very universal transfer block was presented in [25]. The independent electronic adjustment of zero and pole of each so-called bilinear two port (BTP) allows specific forming of frequency response approximating fractional-order behavior. The operational

bandwidth and phase ripple of this two-port depends on the number of sections especially. The frequency locations of zeros and poles are given by specific design requirements and algorithms proposed for example in [19], [20] and many similar works. It creates an intended frequency response (valid for immittances and two-ports as well, i.e. impedance/admittance and transfer magnitude and phase frequency responses). Figure 4.1 shows four BTPs in cascade and a circuit solution of a single BTP employing two OTAs. The transfer function of four blocks in cascade is expressed as (negative order α supposed):

$$K_{\text{int}}(s) = \frac{\prod_{i=1}^{4}\left(1 + s\frac{C_i}{g_{mYi}}\right)}{\prod_{i=1}^{4}\left(1 + s\frac{C_i}{g_{mXi}}\right)} \cong const. \cdot s^{\alpha} \cdot \tag{4.1}$$



a) b)

Fig. 4.1 The synthesis of a fractional-order reconfigurable transfer block: a) chain using BTPs, b) single BTP based on OTAs

Tab. 1 Parameters of BTPs for experimental tests of integrator behavior

i	C_i, nF	g_{mYi}, mS	g_{mXi}, mS
$\alpha = -0.11$ ($\varphi = -10°$)			
1	2200	2.20	1.72
2	1000	8.33	6.58
3	100	6.94	5.48
4	10	5.89	4.54
$\alpha = -0.33$ ($\varphi = -30°$)			
1	2200	2.20	0.80
2	1000	17.00	6.52
3	100	28.00	11.00
4	10	46.00	19.00

The transfer block in Fig. 4.1 allows simple electronic reconfiguration of the order α (positive-differentiator or negative-integrator). Then the slope of the magnitude is defined as $\pm\alpha \cdot 20$ dB/dec and phase reaches $\pm\alpha \cdot \pi/2$ ($\pm\alpha \cdot 90°$) where α represents the non-integer order achieving values between $0 < |\alpha| < 1$. The experiment shows two different α values for behavior of a fractional-order integrator. Specific setting of parameters can be used for generating fractional-order

differentiator behavior as well. Table 1 includes a list of parameters valid for each section obtained by approaches available in [20], [21]. The results of the experiment are shown in Fig. 4.2. All details and specifications of the design are explained in [25]. The phase ripple (error) ±1° and ±3° has been intentionally determined.

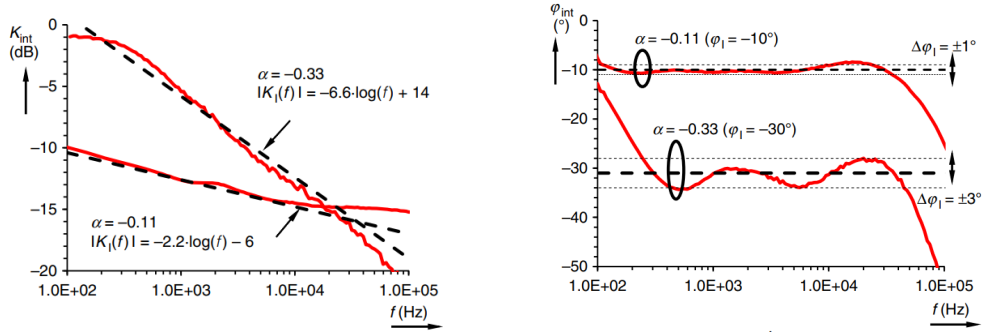


Fig. 4.2 Frequency response of a reconfigurable fractional-order integrator using four BTPs: a) magnitude responses, b) phase responses

4.2 CONSTANT PHASE BLOCK

A fractional-order phase shifter does not have a flat magnitude response typical for an integer-order all-pas filter (alternative name for phase shifter) [26]. Improvements in magnitude were obtained when a reciprocal response to passive fractional-order RC low-pass or high-pass filter determines gain (dependent on frequency) of an active part [27]. However, two ports allowing flat magnitude and phase response (arbitrarily settable value of constant phase shift through a specified band) has not been introduced. It means a constant phase shift for several frequencies. This phase shift is determined by the value of the passive fractional-order element (also called constant phase element - CPE) approximated by RC ladder topology [19], [20]. Figure 4.3 shows an example of RC ladder topology of CPE (fractional-order capacitor in this case) applied in the circuit of a special phase shifter – a constant phase block (CPB). Values of elements are obtained by algorithms presented in [19], [20] and presented in [28]. The circuit uses an operational amplifier (OA) and an automatic amplitude gain control circuit (AGC) presented in [28] with all details. Results of the analysis for two different orders $\alpha_1 = -0.25$ and $\alpha_2 = -0.50$ are shown in Fig. 4.4. The presented behavior of this transfer function is not available using standard linear circuit theory (Hilbert transform). However, it may be useful for synthesis of special subparts of systems as in nonlinear and chaos theory as well as for modeling of various special functions of natural matter.

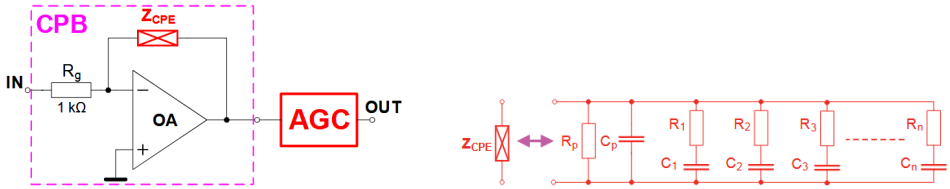
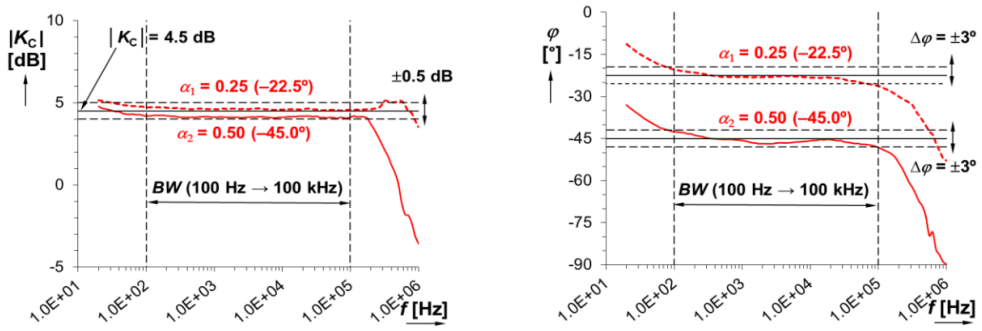


Fig. 4.3 Special phase shifter (constant phase block) performing flat magnitude and phase response: a) circuit implementation, b) typical solution of constant phase element (fractional-order passive element)



a) b)

Fig. 4.4 The frequency response of CPB: a) magnitude, b) phase responses

4.3 ADJUSTABLE FRACTIONAL-ORDER IMMITTANCES

Synthesis of fractional-order immittances is important for practice especially when the value and order α of the impedance can be reconfigured. Active solutions have this ability as presented in [29]. However, also passive CPEs with determined and nonadjustable order can be beneficially extended to electronically adjustable immittances (in value of equivalent capacity or inductance) when used in appropriate circuit topology [30]. The discussed (Section 2) active elements (MLT and DVB/VDDB) fabricated using I3T25 ON Semiconductor process have been selected for this design. Figure 4.5 shows solutions forming active immittance of fractional-order capacitance and inductance character. The electronic adjustment of transconductance g_m offers variability of multiplication factor. The interchange of immittance (CPE) position in topology causes impedance inversion (i.e. the circuits behave as a capacitance multiplier and impedance inverter creating inductance with an adjustable transformation constant). A typical example of operation is documented in Fig. 4.6 on a capacitance multiplier operating with passive CPE having values $C_\alpha = 56\ \mu F/sec^{0.5}$ and $\alpha = 0.5$. The driving voltage V_{SET_gm} between 0.05 and 0.5 V adjusts the value of equivalent capacity between 2 and 19.6 $\mu F/sec^{0.5}$, see all details in [30].

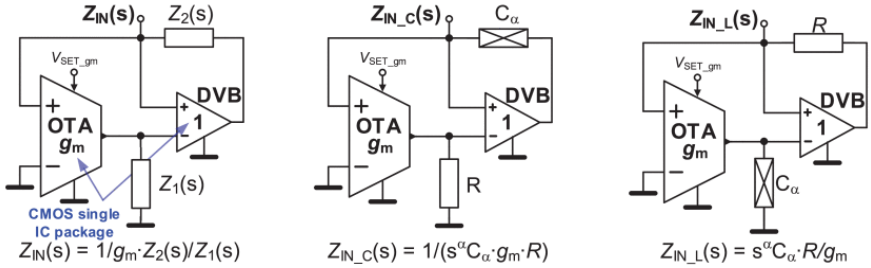
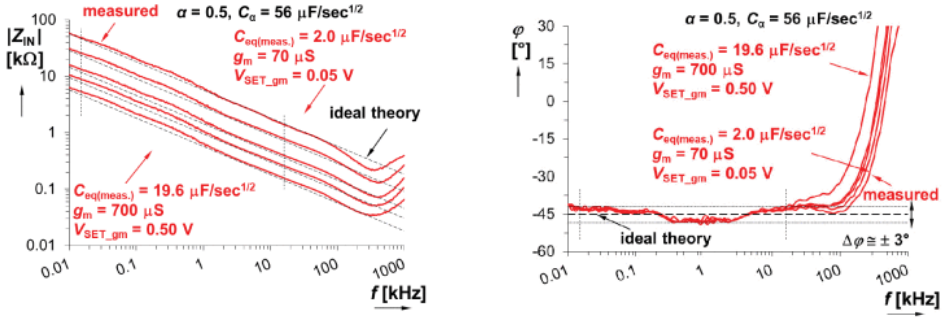


Fig. 4.5 General topology (left) for a fractional-order capacitance multiplier (middle) and impedance inverter generating synthetic inductance (right).



a) b)

Fig. 4.6 Example of operation and electronic adjustability of equivalent capacity of a capacitance multiplier: a) magnitude responses, b) phase responses.

5 READOUTS FOR SENSOR SIGNAL PROCESSING

Integrated circuit design brings significant advantages to sensing various electrical and non-electrical quantities. Our team implemented the fabricated ICs (Section 2) also for purposes of construction of complex systems together with specific commercially available sensors of various quantities (temperature, height of plants, illuminance, etc.). In most cases, processing systems have served for distribution of sensed quantity from isolated and closed environments (agricultural cultivation reservoirs for example) by infra-red (IR) or electromagnetic wireless communication for short distances (several cm). Three examples (illuminance, distance and temperature measurement) are presented further in the text.

5.1 ILLUMINANCE MEASUREMENT

The block scheme of the proposed and designed system for illuminance measurement and processing of the sensed signal is shown in Fig. 5.1. This system uses a standard photoresistor. The principle of operation is quite simple. The actual DC voltage from the voltage divider (including photoresistor) defines the duty cycle of the modulation square wave that is multiplied with the carrier wave at 32.765 kHz (operational band of many commercially available IR receivers). This multiplication generates bursts of variable lengths that are transmitted by an IR diode. Except for the power stage (discrete bipolar transistor), the complete transmitting part, including the pulse width modulation (PWM) generator (ramp generator and single threshold comparator), is created by fabricating analog cells (I3T25 CMOS process). The complete circuit topology includes almost all types of active elements (MLTs, CCCIIs, VDDBs) discussed in Section 2 and Fig. 2.1. The full circuitry is quite extensive and can be found in [31] including all design details and all results of corresponding analyses. The purpose and application of this system is shown in Fig. 5.2. The comparison of transmitted and received (demodulated) quantity (covered in duty cycle variation) results in the typical example of dependence of a duty cycle on illuminance (measured by reference luxmeter) is shown in Fig. 5.3. The error of this measurement is below 10% and acceptable for intended purposes (standard growing process does not require highly accurate information for illuminance regulation, etc.).

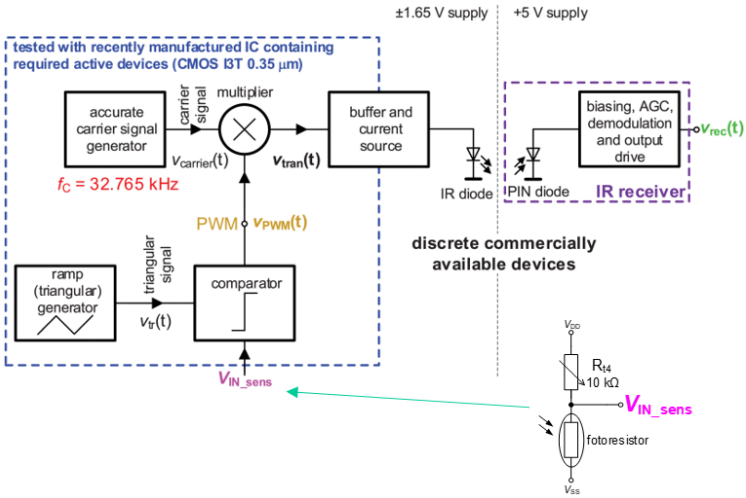


Fig. 5.1 Block scheme of designed sensing system for illuminance measurement and signal distribution

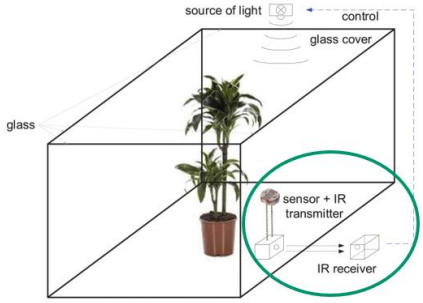


Fig. 5.2 Example of application in transmission of measured illuminance from a closed agricultural reservoir for cultivation of plants

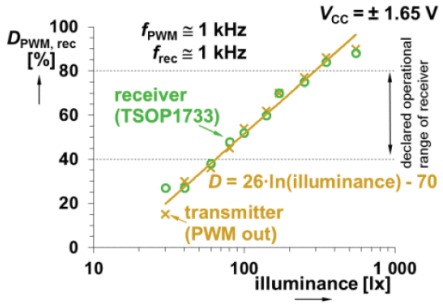


Fig. 5.3 Example of transmitted and received duty cycle in dependence on illuminance

5.2 DISTANCE MEASUREMENT

The height or distance measurement is very important in the cultivation procedure of plants when the growing process requires monitoring in various stages (Fig. 5.4). Of course, the same system as in the previous section can be used but the main intention of the design is to focus on

simplifying the transmitting as well as receiving part (replacement of expensive commercially available IR receivers) [32], see Fig. 5.5. The simplification consists in the direct duty cycle processing without the necessity of second modulation (multiplication by carrier wave 32 kHz), i.e. the PWM signal is directly transmitted by an IR diode without the necessity of generating variable length bursts required for the TSOP family of IR receivers. Then the transmitting part uses less blocks as well as the simple phototransistor suffices at the receiving site. The wireless transmission distance reaches similar values as in the previous case (cm). However, the PWM frequency must be lower (units of kHz) than in the previous case due to reaction times and delays (influencing edges of the square wave) of the phototransistor. The low-cost reflective sensor (Fig. 5.6) with sufficient accuracy (this is the main source of inaccuracies) has been used. The measurement error caused by this sensor reaches several mm (acceptable for the intended application). The system itself generates errors below 3%. Typical results comparing the transmitted and received duty cycle in dependence on measured distance are given in Fig. 5.7. It is necessary to see [32] for all important details and parameters.

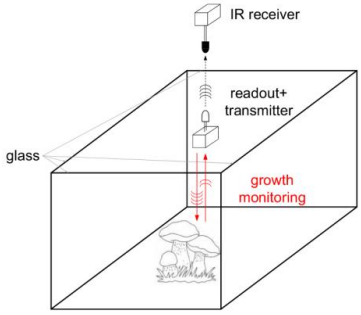


Fig. 5.4 Illustration of measurement of height of plants and distribution of signal from a closed agricultural reservoir for cultivation

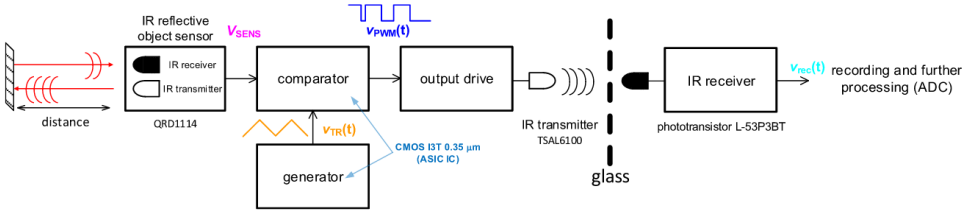


Fig. 5.5 Block concept of system proposed for measuring distance and signal distribution

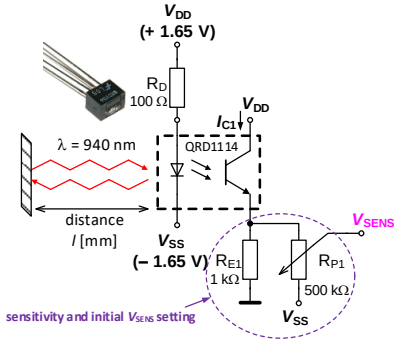


Fig. 5.6 Principle of the IR reflective sensor

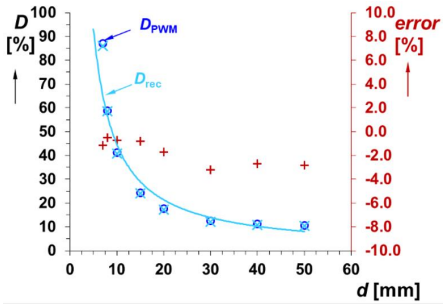


Fig. 5.7 Comparison of transmitted and received duty cycle of square waves in dependence on measured distance

5.3 TEMPERATURE MEASUREMENT

The last example shows the method of measurement when a different wireless transmission (radiofrequency) has been used because IR communication is not possible in all situations (vapor on glass or inside of closed area, etc.). Figure 5.8 introduces a concept [33] using electromagnetic coupling (two ferrite antennas tuned to resonances operating in bands of several hundreds of kHz as shown in the blocks scheme in Fig. 5.9) and amplitude modulation sufficient for short distances (as in previous cases) without significant disadvantages. This type of modulation is sufficient because very slow DC signals are processed on very short distances. Transmitting and receiving parts are constructed from available analog cells (0.35 μm I3T25 CMOS process). The measurement error was tested and evaluated up to several units of °C. Typical results in Fig. 5.10 compare theoretical dependence (empirical equation in [32]) of detected/received voltage on temperature with the experiment. Again, all details for interested readers are available in [33].

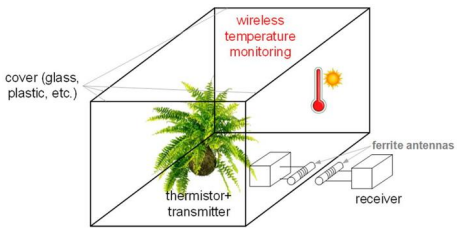
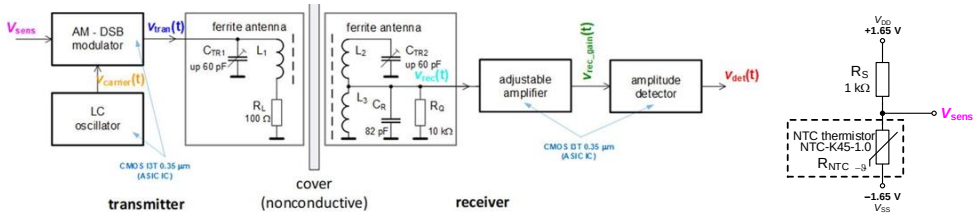


Fig. 5.8 The idea of a system using low-cost analog wireless (electromagnetic) monitoring of temperature in specific environments



a) b)

Fig. 5.9 Transmitting and receiving parts of a system for temperature measurement using short range wireless (radiofrequency/electromagnetic) coupling

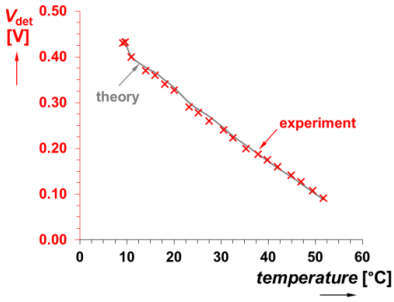


Fig. 5.10 Dependence of detected/received voltage on temperature

6 CONCLUSION

The presented results cover recent activities of the author in three main areas (adjustability extension in circuits, fractional order circuits, and analog systems for sensor applications). These areas have been solved at our departments and by our research team in the past 5-6 years. Several research projects supported these activities. Extended tunability of circuits was solved in projects "Interdisciplinary research of wireless technologies (2015 – 2019)" and "Active elements with differential ports for design of original non-differential and pseudo-differential functional blocks (2016 – 2018)". The fractional-order circuits were the topic of projects "Analogue fractional systems, their synthesis and analysis (2018 – 2020)" and "Synthesis of reliable electrical phantoms describing fractional impedance behavior of real-world systems (2019 – 2021)". The systems for processing signals from sensors represent quite a new topic (last 2 years) for our research group. Practical utilization of principles and features of developed active elements on chips seems to be very useful and beneficial in these applications. Several further projects (also in the field of analog circuits) were solved with participation of the author. Fields of nonlinear systems and experimentation with chaos in projects "Chaotic tangles in subsystems of radiofrequency channel (2015 – 2017)" and "Deterministic, chaotic and stochastic phenomena in the sub-micron integrated structures (2019 – 2021)" have employed ICs (TSMC process) for modeling complex nonlinear structures. These recent works and projects significantly contributed to my knowledge in these fields and provided good background for further study and continuing development in the discussed areas.

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ABSTRACT

This thesis describes research activities in the field of analog signal processing regarding topics of adjustability and tunability (extension of ranges of adjustability) of filtering circuits and oscillators as well as immittances (synthetic elements), fractional-order circuits and readouts for analog systems for measurement of nonelectrical quantities in sensing applications. The examples presented in the first part of work explain importance of the tunability extension on active filter, oscillator and capacitance multiplier performance. The second part targeting on fractional-order circuits discusses example of two-port (integrator) synthesis using electronically adjustable bilinear transfer sections, special fractional-order phase shifter (constant phase block) allowing flat magnitude and phase response, and generalized structure for synthesis of fractional-order adjustable immittances (capacitance, inductance). The last part shows three types of analog systems for measurement, processing and distribution of information about illuminance, distance and temperature from isolated agricultural cultivation reservoirs. These results are supported by experiments employing our own developed and fabricated active elements and chips in various low-voltage CMOS technologies.

ABSTRAKT

Tato práce popisuje příklady výzkumných aktivit v oblasti analogového zpracování signálů v tématech rozšiřování ladících rozsahů filtračních obvodů a oscilátorů stejně jako elektronicky nastavitelných imitancí (syntetických prvků), obvodů neceločíselného řádu a analogových systémů pro zpracování signálů ze senzorů neelektrických veličin. Příklady prezentované v první části práce vysvětlují důležitost rozšiřování ladících rozsahů na aktivním filtru, oscilátoru a speciálním kapacitním násobiči. Druhá část práce cílí na příklady fraktálních (neceločíselných) obvodů v oblasti syntézy přenosových funkcí (integrátor) na bázi tzv. elektronicky nastavitelných bilineárních sekcí, návrhu speciálního fraktálního dvojbranu s konstantní modulovou a fázovou přenosovou charakteristikou a obecnou strukturu pro syntézu fraktálních elektronicky laditelných imitancí (kapacitního nebo induktivního charakteru). Poslední část ukazuje tři vybrané typy analogových systémů pro měření, zpracování a distribuci signálů nesoucích informaci o osvětlení, vzdálenosti, a teplotě z izolovaných prostředí (např. laboratorních reservoárů pro pěstění rostlin). Výsledky byly podpořeny experimenty využívající naše vlastní vyvinuté a vyrobené aktivní prvky a čipy v různých nízkonapěťových CMOS technologiích.