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Novel Active Function Blocks and Their Applications in Frequency Filters and Quadrature Oscillators

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
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NOVEL ACTIVE FUNCTION BLOCKS AND THEIR APPLICATIONS IN FREQUENCY FILTERS AND QUADRATURE OSCILLATORS

NOVÉ AKTIVNÍ FUNKČNÍ BLOKY A JEJICH APLIKACE V KMITOČTOVÝCH FILTRECH A KVADRATURNÍCH OSCILÁTORECH

ZKRÁCENÁ VERZE PH.D. THESIS

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KLÍČOVÁ SLOVA

Analogové zpracování signálu, proudový mód, napěťový mód, smíšený mód, kmitočtový filtr, fázovací článek prvního řádu, univerzální filtr, KHN-ekvivalent, inverzní filtr, aktivní uzemněný induktor simulátor, kvadraturní oscilátor, UCC, UVC, DBTA, PCA, CFTA, ZC-CFTA, CCCFTA, ZC-CCCITA, GCFDITA, CBTA, MCFOA, VGC-MCFOA, CC-VCIII-.

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CONTENTS

INTRODUCTION

Frequency filters and sinusoidal oscillators are linear electric circuits [63] that are used in wide area of electronics and also are the basic building blocks in analogue signal processing. The analogue frequency filters are the most often used as anti-aliasing video filters in the analogue sections of high-speed data communication systems defined by ITU BT 601 standard [65] or for signal processing in wireless LANs described by IEEE 802.11 standard [41], in IF (Intermediate Frequency) receiver stages of the GSM cellular telephones [23], in receiver baseband blocks of modern radio systems [51], in hard-drive communication interfaces [38], measurement systems [67], automotive industry [26], or in piezoresistive pressure sensors [53]. Oscillators also represent an important unit in many telecommunication, instrumentation and control systems [1], [3], [18], [30].

In the last decade, for analogue signal processing huge number of active building blocks were introduced. However, there is still the need to develop new active elements that offer new and better advantages. This thesis is, therefore, focused on definition of other novel ABBs and, furthermore, novel filter and oscillator structure designs.

In the present days a number of trends can be noticed in the area of analogue filter and oscillator design, namely reducing the supply voltage of integrated circuits and transition to the current-mode [63]. On the other hand, voltage- and mixed-mode circuit design still receive considerable attention of many researchers. Therefore, the proposed circuits in this work are working in current-, voltage-, or mixed-mode.

1 STATE OF ART

Nowadays, the presented structures of active frequency filters and oscillators are often employing current conveyors (CCs), where the second-generation current conveyor (CCII) [55] is the most popular. The CCII is the basic block of many other active elements. Here, the current-feedback operational amplifier (CFOA) [22], [60] that is a combination of the CCII and voltage follower (VF) [54] or the composite current conveyor (CCC) [58] that is the interconnection of the plus-type and minus-type CCIIs can be mentioned. Recently, based on the CCC the modified CFOA (MCFOA) [69] was reported. Later, the inverting second-generation current conveyor (ICCII) as a missing building block in analogue signal processing techniques has been introduced [4]. By the combination of CCII and ICCII the dual-X second-generation current conveyor (DXCCII) [71] for the tunable continuous-time filter design has been built. Recently, further research has focused on CCs with variable current and/or voltage gains such as electronically tunable second-generation current conveyor (ECCII) [45], variable gain current conveyor (VGCCII) [70], or voltage and current gain second-generation current conveyor (VCG-CCII) [20].

Using the duality principle, the voltage conveyor (VC) has been presented in 1981 [27]. As in the theory of CCs, also here the first- and second-generation VCs (VCI, VCII, IVCI, and IVCII) were described [27], [21], [46]. The best known VC is the plus-type differential current voltage conveyor (DCVC+) [52] that is more often labelled as the current differencing buffered amplifier (CDBA) [2]. Recently, the current-controlled CDBA (C-CDBA), the current-controlled inverting CDBA (C-ICDBA), and the z copy-controlled gain-CDBA (ZC-CG-CDBA) [8] have also been introduced [43]. By the modification of the CDBA or replacement of the VF by the operational transconductance amplifier (OTA) [29] the differential-input current feedback amplifier (DCFA) [72], and current differencing transconductance amplifier (CDTA) [7] have been presented.

Based on the idea of the "universal" active element [17] the universal current conveyor (UCC) [5], [14], [84] was designed and developed as a sample series containing 50 pieces, using the CMOS 0.35 μm technology, under the designation UCC-N1B 0520 at our workplace, and produced in cooperation with AMI Semiconductor Czech, Ltd., (now ON Semiconductor

Czech Republic, Ltd.). On the basis of the UCC, the universal voltage conveyor (UVC) was designed [15], [46], [74], [87]–[90], and produced under the designation UVC-N1C 0520. The realizable generations and types of VCs using the UVC were shown by Minarcik and Vrba in [46].

2 THESIS OBJECTIVES

In the last decade, for analogue signal processing huge number of active building blocks (ABBs) were introduced, however, there is still a need to develop new active elements that offer new and better advantages. Therefore, the main aim of this thesis is to define various types of novel active building blocks. The first intention is to define such novel more-terminal ABB with low-impedance current/high-impedance voltage inputs and high-impedance current/low-impedance voltage outputs, which will belong to the group of "universal" active elements, e.g. UCC and UVC. Special attention will be paid on active element with only current inputs and outputs. From the cascadability point of view, ABBs with low-input and high-output impedance terminals are the most interesting. The proposed active element will be further studied and, if possible, modified according to special needs.

In the present days a number of trends can be noticed in the area of active function block design. The attention is also focused on ABBs with tunability property. Here the current or voltage gain tuning can be mentioned. Hence, part of this work is focused on such novel ABB design that voltage gain can be controlled by means of external current.

Voltage conveyors are also important and useful elements in analogue signal processing, however, their potentials are still not enough studied. Therefore, special attention will be also paid on novel VC design with tunability feature.

The main part of the thesis will concentrate on application possibilities of the defined functional blocks. First-order all-pass filters are widely used in analogue signal processing. Several current-mode (CM), voltage-mode (VM), or mixed-mode first-order AP filter realizations using different active building blocks have been reported in the literature. These topologies realize either inverting or non-inverting type of filters. For realizing the complementary type, they need to change the circuit topology. Furthermore, most of the reported realizations do not include electronical tunability property. Hence, the intention is to propose such AP filters that enable both the inverting and the non-inverting type AP filter responses simultaneously and easy tunability of the natural frequency.

Part of this work focuses on such second-order filter structures that can provide all standard filter responses without changing the circuit topology. Special attention is paid to Kerwin–Huelsman–Newcomb structure that enables mutually independent control of the quality factor Q and characteristic frequency ω_0.

Due to disadvantages of conventional inductors, active element-based inductor design is very desirable to designers today. During the last few decades, various grounded inductors have been created using different high-performance active building blocks. However, they employ excessive number of active and passive components. Thus, the aim is to create single grounded capacitor-based positive grounded inductor simulator in compact form.

Quadrature oscillators also represent an important unit in many communication, control systems, instrumentation and measurement systems. Therefore, part of this work attempts this issue.

In the first step the theoretical analyses are done using SNAP software [37]. To verify the behavior of the proposed circuits, defined active elements are implemented using bipolar or CMOS internal structures. The feasibility of selected circuits are also confirmed by experimental measurements.

3 NOVEL ACTIVE BUILDING BLOCKS AND THEIR PROPERTIES

This Chapter presents different novel active elements, where all of them have been introduced and developed within this work at the Department of Telecommunications, Brno University of Technology. These active building blocks (ABBs) are further used in this work for various filter and oscillator designs.

3.1 Differential-input buffered and transconductance amplifier (DBTA)

The differential-input buffered and transconductance amplifier (DBTA) [75], [76], [78], [79], [86], was introduced at our Department in 2009 and it belongs to the group of "universal" active elements presented above. It is a six-port active element, which schematic symbol is shown in Fig. 3.1. It has low-impedance current inputs p, n and high-impedance voltage input y. The difference of the i_p and i_n currents flows into auxiliary terminal z. The voltage v_z on this terminal is transferred into output terminal w using the VF [54] and also transformed into current using the transconductance g_m, which flows into output terminal x.

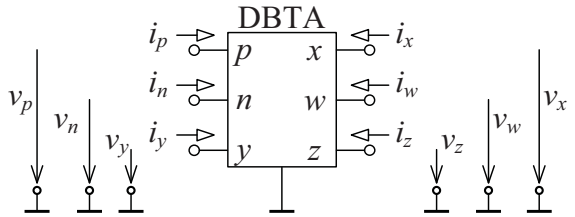


Fig. 3.1: Schematic symbol of DBTA

Relations between the individual terminals of the non-ideal DBTA can be described by following hybrid matrix:

$$\begin{bmatrix} v_p \\ v_n \\ i_y \\ i_z \\ v_w \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_p & 0 & 0 & 0 \\ 0 & 0 & \beta_n & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \gamma & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ v_y \\ v_z \\ i_w \\ v_x \end{bmatrix}, \tag{3.1}$$

where $\alpha_p = 1 - \varepsilon_i$, $\alpha_n = 1 - \varepsilon_i$ and ε_i ($|\varepsilon_i| \ll 1$) are the current tracking errors from p and n terminals to z terminal, $\beta_p = 1 - \varepsilon_v$, $\beta_n = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) are the voltage tracking errors from p and n terminals to z terminal and $\gamma = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) is the voltage tracking error from z terminal to w terminal of DBTA, respectively.

3.2 Current follower transconductance amplifier (CFTA)

When the CDTA has been introduced in 2003 [7], it has been considered to be a versatile active building block for current-mode signal processing circuits. Analogous to the CDBA [2], the input circuitry of the CDTA is also formed by the CDU, which is followed by the OTA [29]. In the point of view of the low power dissipation and manufacturing cost, it is important to keep the internal structure transistor count and the count of ABBs at minimum. The earlier reported circuits in [6], [7], [61], [66], do not fully use the potential of the CDTAs, since one of

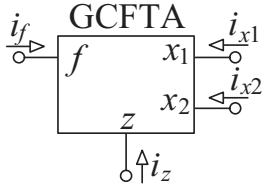


Fig. 3.2: Schematic symbol of GCFTA

the input terminals p or n is not used. This may cause some noise injection into the monolithic circuit [35]. Thus, to avoid this problem, the CDTA has been simplified by replacing the CDU by a simple current follower (CF) or inverter (CI). The appropriate novel ABBs are called current follower transconductance amplifier (CFTA) [12], [73], [80], [82], and inverted current follower transconductance amplifier (ICFTA) [81], which was in [12] also introduced as current inverter transconductance amplifier (CITA).

The generalized CFTA (GCFTA) element consists of an input CF (positive or negative) that transfers the input current to the z terminal and a dual-output OTA stage, which is used to convert the voltage at the z terminal to dual-output currents [85]. The transconductance parameter g_m corresponds for the positive output and $-g_m$ for the negative output. In general, the equations describing an ideal GCFTA (Fig. 3.2) are:

$$\begin{bmatrix} v_f \\ i_z \\ i_{x1} \\ i_{x2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ a & 0 & 0 & 0 \\ 0 & b_1 g_m & 0 & 0 \\ 0 & b_2 g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{x1} \\ v_{x2} \end{bmatrix}, \tag{3.2}$$

where $a,\ b_1,\ b_2 \in \{1, -1\}$.

3.3 Z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA)

The ZC-CCCITA (z-copy current-controlled current inverting transconductance amplifier) is recently presented ABB at our Department [83], which is a derivative of the conventional ZC-CITA [9]. It essentially consists of an input negative current-controlled current follower (i.e. current-controlled current inverter) stage that transfers the input current to the z and zc terminals and a transconductance amplifier stage, which converts the voltage at the z terminal to output current at the x terminal. The circuit symbol of ZC-CCCITA is shown in Fig. 3.3 and the hybrid matrix is as follows:

$$\begin{bmatrix} v_f \\ i_z \\ i_{zc} \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} R_f & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & g_m & 0 & 0 & 0 \\ 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{zc} \\ v_{x+} \\ v_{x-} \end{bmatrix}. \tag{3.3}$$

In (3.3), the intrinsic resistance R_f and the transconductance g_m can be defined as:

$$R_f = \frac{V_\mathrm{T}}{2I_\mathrm{O}} \quad \text{and} \quad g_m = \frac{I_\mathrm{B}}{2V_\mathrm{T}}, \tag{3.4}$$

respectively. Here the V_T is the thermal voltage (approximately 26 mV at 27°C), the I_O is the bias current to control the intrinsic resistance of the input terminal f, and the I_B is the control current adjusting the transconductance g_m of the ZC-CCCITA.

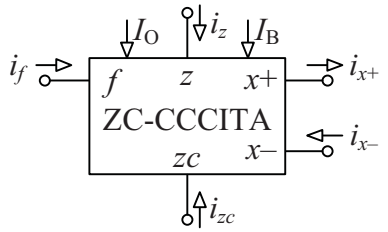


Fig. 3.3: Schematic symbol of ZC-CCCITA

3.4 Generalized current follower differential input transconductance amplifier (GCFDITA)

In one of more recent publication [11], authors introduced a modified version of the GCFTA [81] with buffered voltage outputs wherein the transconductance of conventional GCFTA is changed to differential input transconductance amplifier. Here presented new ABB is called generalized current follower differential input transconductance amplifier (GCFDITA), which is a derivative of the circuit presented in [11]. Compared to [11], the new ABB does not have a buffered voltage output terminal.

The generalized current follower differential input transconductance amplifier (GCFDITA) consists of an input positive or negative current follower that transfers the input current at terminal f to the z terminal and a balanced-output differential input transconductance amplifier (BO-DITA) stage, which is used to convert the difference voltage between the z and v terminals to balanced output currents. The transconductance parameter g_m corresponds for the positive output and $-g_m$ for the negative output. The schematic symbol of GCFDITA is shown in Fig. 3.4. In general, the hybrid matrix characterizing an ideal GCFDITA is:

$$\begin{bmatrix} v_f \\ i_z \\ i_v \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ a & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & g_m & -g_m & 0 & 0 \\ 0 & -g_m & g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_v \\ v_{x+} \\ v_{x-} \end{bmatrix}, \tag{3.5}$$

where $a \in \{1, -1\}$ and $g_m = \frac{I_B}{2V_T}$. Here the V_T is the thermal voltage (approximately 26 mV at 27°C) and the I_B and is control current adjusting the transconductance g_m. Depending on the values of a, two variants of GCFDITA are possible, namely current follower differential input transconductance amplifier (CFDITA) for $a = 1$ and current inverter differential input transconductance amplifier (CIDITA) for $a = -1$.

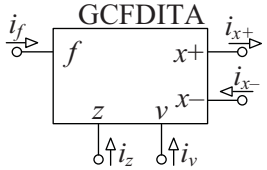


Fig. 3.4: Schematic symbol of GCFDITA

3.5 Voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA)

The voltage gain-controlled MCFOA (VGC-MCFOA) (Fig. 3.5) is recently presented ABB at our Department, which is a derivative of the MCFOA presented in [68]. Relations between the individual terminals of the VGC-MCFOA can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{Y}} \\ i_{\mathrm{Z1}} \\ i_{\mathrm{Z2}} \\ i_{\mathrm{Z3}} \\ v_{\mathrm{X}} \\ v_{\mathrm{W}} \end{bmatrix} = \begin{bmatrix} -\alpha_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_2 & 0 & 0 & 0 & 0 \\ 0 & -\alpha_3 & 0 & 0 & 0 & 0 \\ \alpha_4 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & h\beta_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{W}} \\ i_{\mathrm{X}} \\ v_{\mathrm{Y}} \\ v_{\mathrm{Z1}} \\ v_{\mathrm{Z2}} \\ v_{\mathrm{Z3}} \end{bmatrix}, \tag{3.6}$$

where $\alpha_j = 1 - \varepsilon_{ij}$ and $\beta_k = 1 - \varepsilon_{vk}$ ($j = 1, 2, 3$ and $k = 1, 2$) are the non-ideal current and voltage gains, respectively, and ε_{ij} ($|\varepsilon_{ij}| \ll 1$) and ε_{vk} ($|\varepsilon_{vk}| \ll 1$) denote current and voltage tracking errors of the VGC-MCFOA, respectively. The presented novel ABB can be easily electronically tuned by means of the voltage gain h.

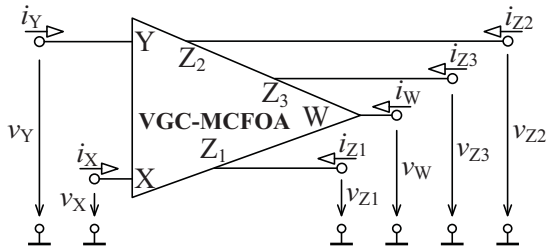
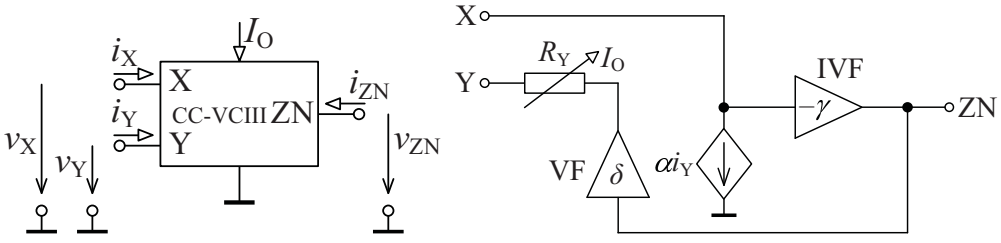


Fig. 3.5: Schematic symbol of VGC-MCFOA

3.6 Minus-type current-controlled third-generation voltage conveyor (CC-VCIII–)

The minus-type current-controlled third-generation voltage conveyor (CC-VCIII–) is a novel three-port building block with electronic tuning, which schematic symbol and behavioral model are shown in Fig. 3.6 [77]. The current through the X terminal follows the current of the Y terminal. The voltage of the Y terminal follows the voltage of the X terminal. Finally, the voltage of the ZN terminal follows the inverted voltage of the X terminal. The intrinsic resistance of Y terminal can be easily controlled by means of external control current I_{O}, which makes the introduced ABB attractive for resistorless and electronically controllable



(a) (b)

Fig. 3.6: (a) Schematic symbol and (b) behavioral model of CC-VCIII–

linear circuit applications. Relations between the individual terminals of the non-ideal CC-VCIII– can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{X}} \\ v_{\mathrm{Y}} \\ v_{\mathrm{ZN}} \end{bmatrix} = \begin{bmatrix} 0 & \alpha & 0 \\ \delta & R_{\mathrm{Y}} & 0 \\ -\gamma & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{X}} \\ i_{\mathrm{Y}} \\ i_{\mathrm{ZN}} \end{bmatrix}, \tag{3.7}$$

where $\alpha = 1 - \varepsilon_i$, $\delta = 1 - \varepsilon_{v1}$, and $\gamma = 1 - \varepsilon_{v2}$. Here, the R_{Y} is the intrinsic resistance of the y terminal, ε_i ($|\varepsilon_i| \ll 1$) and ε_{v1}, ε_{v2} ($|\varepsilon_{v1}|$,$|\varepsilon_{v2}| \ll 1$) denote current and voltage tracking errors of CC-VCIII–, respectively.

4 FIRST-ORDER ALL-PASS FILTER DESIGN

First-order all-pass (AP) filters are widely used in analogue signal processing in order to shift the phase of an electrical signal while keeping its amplitude constant. First proposed AP filters employing op-amps suffer from the well-known limitations of opamp-based circuits such as frequency limitations, the use of a large number of passive elements and lack of electronic tuning [49]. Therefore, to eliminate these disadvantages, other types of active elements have started to be used for AP filter design. They also play a great role in the design of other types of active circuits such as quadrature or multiphase oscillators and high-Q band-pass filters [16], [25], [62].

4.1 Electronically tunable resistorless all-pass filter using novel voltage conveyor

Nowadays, as already mentioned, the electronically tunable resistorless VM all-pass filters receive considerable attention. In current technical literature huge number of such filters are presented, where the tunability feature of circuits used are solved in different ways. For example, in recently presented voltage differencing-differential input buffered amplifier (VD-DIBA)-based VM all-pass filter [10] the tunability property of the OTA is used to shift the phase response of the circuit. Another technique is given in [42], where the appropriate resistor is replaced via MOSFET-based VCR. After the CCCII [24] was introduced, a new period has been opened with respect to electronical tunability in the analog filter design. Here the intrinsic X-input resistance of the CCCII is controlled via an external current, as shown in [44]. The same technique is adapted to the novel type of voltage conveyor, namely CC-VCIII– [77], where analogously the input circuitry is formed by the CCCII.

The novel VM all-pass filter using canonic number of passive and active elements (i.e. single capacitor, and single CC-VCIII–) is shown in Fig. 4.1 [77]. Considering the ideal CC-VCIII–

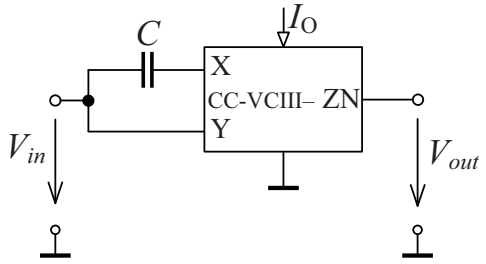


Fig. 4.1: Proposed electronically tunable resistorless first-order all-pass filter

(i.e. α, δ, and γ are unity), routine analysis yields voltage transfer function in following form:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{sCR_{\rm Y} - 1}{sCR_{\rm Y} + 1}. \tag{4.1}$$

From (4.1), the phase of the filter is found as:

$$\varphi(\omega) = -2\text{arctg}(\omega CR_{\rm Y}), \tag{4.2}$$

and the natural frequency ω_0 can be express as:

$$\omega_0 = \frac{1}{CR_{\rm Y}}. \tag{4.3}$$

Taking into account the non-idealities of the CC-VCIII–, the TF in (4.1) converts to:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{\gamma(sCR_{\rm Y} - \alpha)}{sCR_{\rm Y} + \alpha\delta\gamma}, \tag{4.4}$$

Assuming that all of the nonideal gains are constant in our frequency range of interest, the phase response of the filter is given as:

$$\varphi(\omega) = -\text{arctg}\left(\frac{\omega CR_{\rm Y}}{\alpha}\right) - \text{arctg}\left(\frac{\omega CR_{\rm Y}}{\alpha\delta\gamma}\right). \tag{4.5}$$

From (4.4) and (4.5) it can be seen that the non-idealities of the CC-VCIII– slightly affect the magnitude and phase responses of the filter. Consequently, the pole frequency of the presented filter is found as:

$$\omega_0 = \frac{\alpha\delta\gamma}{CR_{\rm Y}}, \tag{4.6}$$

and the active and passive sensitivities of ω_0 are given as:

$$S_{\alpha}^{\omega_0} = S_{\delta}^{\omega_0} = S_{\gamma}^{\omega_0} = 1, \quad S_{C}^{\omega_0} = S_{R_{\rm Y}}^{\omega_0} = -1. \tag{4.7}$$

From Eq. (4.7) it is evident that all sensitivities of active parameters and passive components for ω_0 are unity in relative amplitude. Hence, the proposed filter shows low sensitive performance.

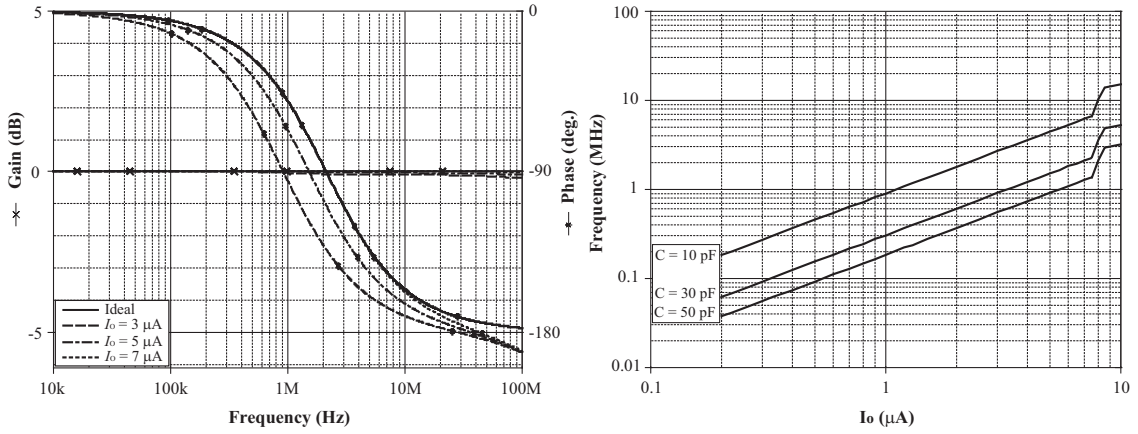
For a complete analysis of the circuit, it is also important to take into account parasitic impedances of the CC-VCIII–. Therefore, the matrix relationship of (3.7) changes as follows:

$$\begin{bmatrix} i_{\rm X} \\ v_{\rm Y} \\ v_{\rm ZN} \end{bmatrix} = \begin{bmatrix} sC_{\rm X} + \frac{1}{R_{\rm X}} & \alpha & 0 \\ \delta & R_{\rm Y} & 0 \\ -\gamma & 0 & sC_{\rm ZN} + \frac{1}{R_{\rm ZN}} \end{bmatrix} \begin{bmatrix} v_{\rm X} \\ i_{\rm Y} \\ i_{\rm ZN} \end{bmatrix}. \tag{4.8}$$

Here $R_{\rm X}$, $R_{\rm ZN}$, $C_{\rm X}$, and $C_{\rm ZN}$ are the parasitic resistances and capacitances at their relevant terminals. Considering these parasitics of the all-pass filter in Fig. 4.1, the ideal TF of (4.1) turns to be:

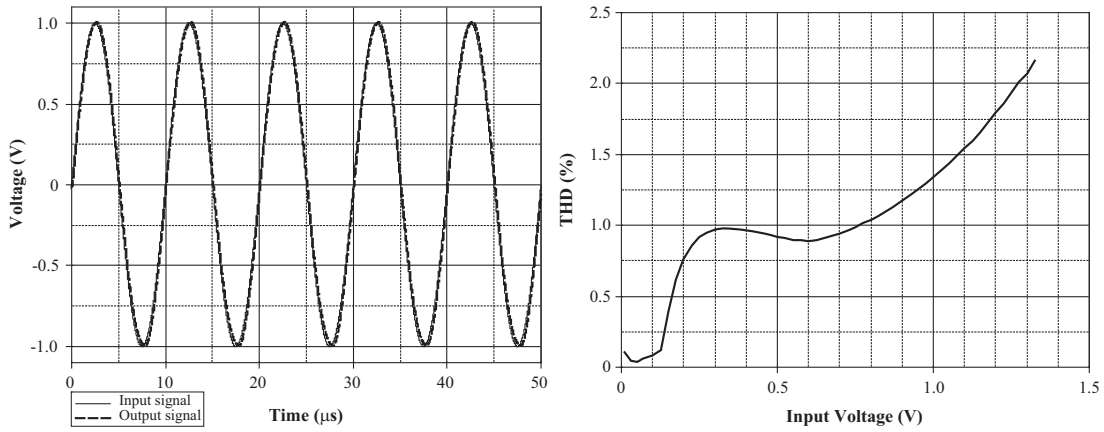
$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{\gamma R_{\rm X}(sCR_{\rm Y} - \alpha)}{R_{\rm Y}R_{\rm X}s(C + C_x) + R_{\rm Y} + \alpha\delta\gamma R_{\rm X}}, \tag{4.9}$$

where $R_{\rm X}$ and $C_{\rm X}$ denote parasitic resistance and capacitance at X terminal of CC-VCIII–. Note that the parasitic capacitance $C_{\rm X}$ can be absorbed into the external capacitor as it appears in parallel with it. If $R_{\rm Y}$ is sufficiently higher than $R_{\rm X}$ and $C \gg C_{\rm X}$, the TF in (4.9) become to form presented in (4.4).



(a) (b)

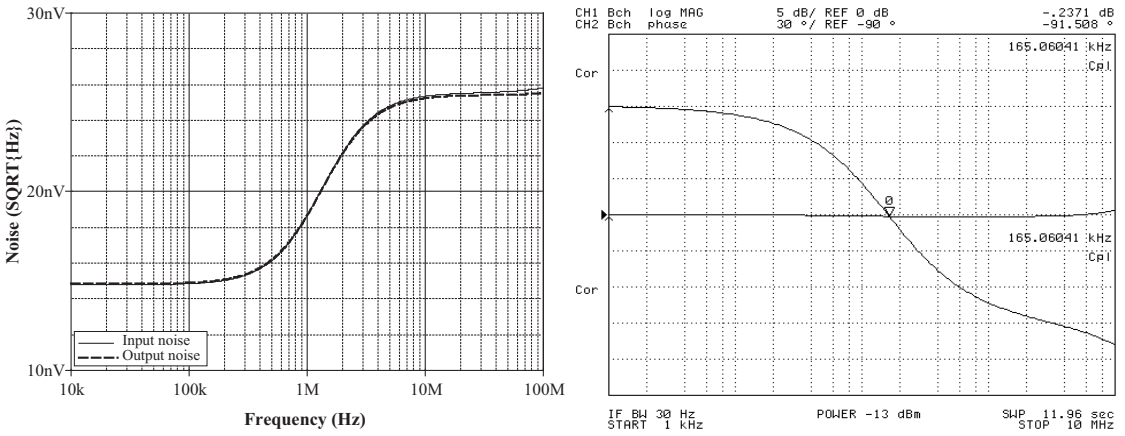
Fig. 4.2: a) Electronical tunability of gain and phase responses by the bias current I_{O}, (b) possibility of tuning the pole frequency by the bias current I_{O} at different values of C



(a) (b)

Fig. 4.3: (a) Time-domain responses of the proposed all-pass filter at 100 kHz, (b) THD of the all-pass filter at 100 kHz

Using the CMOS implementation of the CC-VCIII–, the proposed circuit in Fig. 4.1 has been simulated in SPICE software. The transistors are modeled by the TSMC 0.35 μm CMOS process parameters. The DC power supply voltages are equal to ± 2.5 V and $V_{\mathrm{B}} = -1.7$ V. Fig. 4.2(a) shows the ideal and simulated phase and gain responses illustrating the electronic tunability for $C = 30$ pF. The pole frequency of the proposed filter is varied for $f_0 \approx = \{0.908; 1.52; 2.12\}$ MHz using the bias current $I_{\mathrm{O}} = \{3; 5; 7\}$ μA, respectively. Similarly, possibility of tuning the pole frequency by the bias current I_{O} at three different values of C is shown in Fig. 4.2(b). To illustrate the time-domain performance, transient analysis is performed to evaluate the voltage swing capability and phase errors of the filter as shown in Fig. 4.3(a). A sine-wave input of 1 V amplitude and frequency of 100 kHz was applied to the filter while keeping the bias current $I_{\mathrm{O}} = 5$ μA and $C = 30$ pF. Note that the output waveform is very close to the input one. The THD variation with respect to amplitude of the applied sinusoidal input voltage at 100 kHz (filter parameter: $I_{\mathrm{O}} = 5$ μA and $C = 30$ pF) is shown in Fig. 4.3(b). The THD rapidly increases when the input signal is increased beyond 0.7 V amplitude. An input with the amplitude of 1 V yields THD value of 1.34%. Using the INOISE and ONOISE statements, the input and output noise behavior with respect to frequency has also been simulated, as it is shown in Fig. 4.4(a). The equivalent input and output noises at pole frequency ($f_0 \cong 1.52$ MHz) are found as 20.83 and 20.82 nV/$\sqrt{\mathrm{Hz}}$, respectively. The total power dissipation of the proposed all-pass filter at $f_0 \approx 1.52$ MHz is found to be 15.6 mW.



(a) (b)

Fig. 4.4: (a) Input and output noise variations versus frequency, (b) measured gain and phase characteristics of the proposed VM first-order all-pass filter

In order to confirm the simulation results, the behavior of the proposed all-pass filter has also been verified by experimental measurements. In the measurements the UVC-N1C 0520 [59], [87] integrated circuit has been used. The capacitor value has been chosen as 1 nF and the intrinsic resistance value of the Y terminal has been selected as 1 kΩ. In this case a 90° phase shift is at $f_0 \cong 159.15$ kHz. In the measurements the network analyzer Agilent 4395A has been used and the results are shown in Fig. 4.4(b). The real behavior of the filter corresponds to theory well.

5 SECOND-ORDER MULTIFUNCTION AND UNIVERSAL FILTERS

In the present days the highest attention is paid on such second-order filter structures that can provide at least the basic three standard filter functions, i.e. low-, band-, high-pass or all standard (also band-stop and all-pass) filter responses without changing the circuit topology. Such circuit topologies are called multifunction or universal filters, respectively. Probable the best known multifunction filtering structure is the KHN (Kerwin–Huelsman–Newcomb) that, furthermore, enables mutually independent control of the quality factor Q and characteristic frequency ω_0 [34]. This Chapter is focused on this issue.

5.1 Universal VM filter employing single DBTA

This Section presents the application possibilities of the recently defined DBTA in VM universal filter. The proposed VM second-order filtering structure employing single DBTA and four passive components is shown in Fig. 5.1 [79]. Note that even if all passive elements are shown as floating, which might be not attractive for integration [13], it should be mentioned that unused voltage inputs are always grounded, as described below.

The output voltages V_{o1} and V_{o2} of this circuit are given by the relations:

$$V_{o1} = \frac{G_1 g_m V_{i1} + sC_2 G_2 V_{i2} + s^2 C_1 C_2 V_{i3} - sC_2 g_m V_{i4}}{D}, \tag{5.1}$$

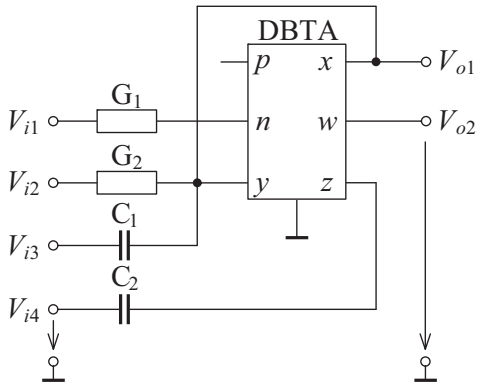


Fig. 5.1: Proposed voltage-mode universal filter using single DBTA

$$V_{o1} = \frac{\left[\begin{array}{l} -\left(sC_1G_1 + G_1G_2\right)V_{i1} + G_1G_2V_{i2} + \\ +sC_1G_1V_{i3} + \left(s^2C_1C_2 + sC_2G_2\right)V_{i4} \end{array}\right]}{D}, \tag{5.2}$$

where

$$D = s^2C_1C_2 + sC_2G_2 + G_1g_m. \tag{5.3}$$

For the proposed filter depending on the status of circuit input four voltages V_{i1}, V_{i2}, V_{i3} and V_{i4} numerous filter functions are obtained. Based on the output selected there are two cases shown as presented below:

Case I. If the $V_o = V_{o1}$ is used as output, then from (5.1) the realizable transfer functions in voltage mode are:

(i) If $V_{i2} = V_{i3} = V_{i4} = 0$ (grounded), a low-pass filter (LP1) can be obtained with V_o/V_{i1};
(ii) If $V_{i1} = V_{i3} = V_{i4} = 0$ (grounded), a band-pass filter (BP1) can be obtained with V_o/V_{i2};
(iii) If $V_{i1} = V_{i2} = V_{i4} = 0$ (grounded), a high-pass filter (HP1) can be obtained with V_o/V_{i3};
(iv) If $V_{i1} = V_{i2} = V_{i3} = 0$ (grounded), a band-pass filter (BP2) can be obtained with V_o/V_{i4};
(v) If $V_{i2} = V_{i4} = 0$ (grounded) and $V_{i1} = V_{i3} = V_{in}$, a band-stop filter (BS) can be obtained with V_o/V_{in};
(vi) If $V_{i1} = 0$ (grounded) and $V_{i2} = V_{i3} = V_{i4} = V_{in}$, an all-pass (AP) can be obtained with V_o/V_{in}.

In this case the proposed circuit is universal and can provide all standard types of filter functions, i.e. low-, band-, high-pass, band-stop, and an all-pass response without changing the circuit topology.

Case II. If the $V_o = V_{o2}$ is used as output, then from (5.2) the realizable transfer functions in voltage mode are:

(vii) If $V_{i1} = V_{i3} = V_{i4} = 0$ (grounded), a low-pass filter (LP2) can be obtained with V_o/V_{i2};
(viii) If $V_{i1} = V_{i2} = V_{i4} = 0$ (grounded), a band-pass filter (BP3) can be obtained with V_o/V_{i3};
(ix) If $V_{i3} = 0$ (grounded) and $V_{i1} = V_{i2} = V_{i4} = V_{in}$, a high-pass filter (HP2) can be obtained with V_o/V_{in}.

Thus, the circuit is multifunction and it is capable of realizing low-, band- and high-pass response without changing the circuit topology. In case of HP2 response the proposed circuit requires component matching conditions $C_1 = C_2$ and $G_1 = G_2$.

For all filters the natural frequency ω_0, quality factor Q and bandwidth BW derived from (5.3) are:

$$\omega_0 = \sqrt{\frac{G_1g_m}{C_1C_2}},\ Q = \frac{1}{G_2}\sqrt{\frac{C_1G_1g_m}{C_2}},\ \mathrm{BW} = \frac{\omega_0}{Q} = \frac{G_2}{C_1}. \tag{5.4}$$

Note that the quality factor Q can be controlled independently of natural frequency ω_0 by G_2. By replacing appropriate conductor by FET-based VCR [31], [57], the quality factor Q can be controlled electronically, which is particular advantage of the proposed circuit. The

natural frequency ω_0 can be independently adjusted from the bandwidth, by varying C_2, G_1 or g_m of the proposed frequency filter. Here, the appropriate capacitor can be replaced by a voltage-controlled capacitor (VCC) [40], [47], or by digitally-controlled varactor (DCV) [19] for electronical control of the natural frequency ω_0 independently from the bandwidth.

The relative sensitivities of the ω_0, Q and BW parameters of the designed circuit derived from (5.4) are:

$$\begin{aligned} S^{\omega_0}_{G_1,g_m} &= -S^{\omega_0}_{C_1,C_2} = \frac{1}{2}, \quad S^{\omega_0}_{G_2} = 0, \\ S^{Q}_{C_1,G_1,g_m} &= -S^{Q}_{C_2} = \frac{1}{2}, \quad S^{Q}_{G_2} = -1, \\ S^{\mathrm{BW}}_{G_2} &= -S^{\mathrm{BW}}_{C_1} = 1, \quad S^{\mathrm{BW}}_{C_2,G_1,g_m} = 0. \end{aligned} \tag{5.5}$$

From the results it is evident that the sensitivities are low and not larger than unity of absolute value.

Taking into account the non-idealities of DBTA and assuming the transconductance g_m of its OTA as follows [64]:

$$g_m = \frac{g_m \omega_g}{s + \omega_g} \cong g_m(1 - \mu s), \tag{5.6}$$

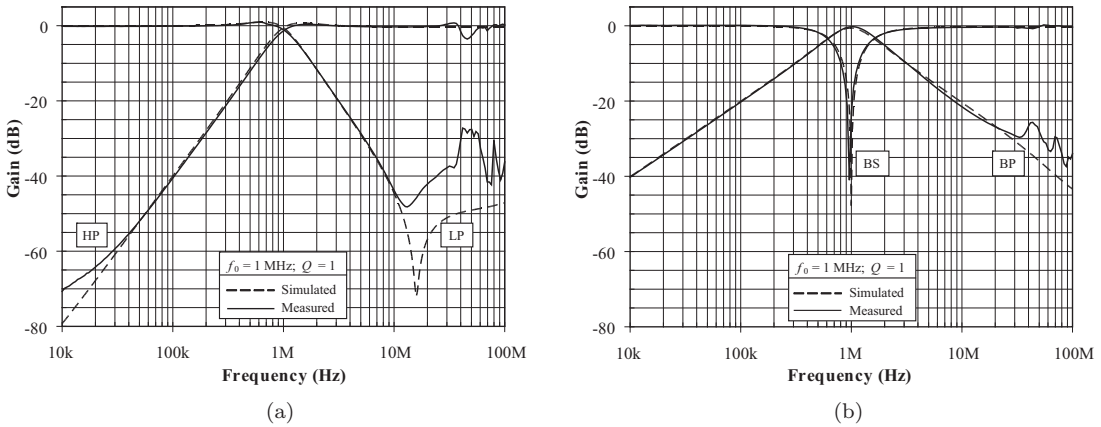
where ω_g is the first-pole of the OTA and $\mu = 1/\omega_g$, the denominator of (5.1), (5.2) becomes:

$$D = s^2 C_1 C_2 + s C_2 G_2 \left(1 - \frac{\alpha_{\mathrm{n}} \beta_{\mathrm{n}} G_1 g_m \mu}{C_2 G_2}\right) + \alpha_{\mathrm{n}} \beta_{\mathrm{n}} G_1 g_m. \tag{5.7}$$

Due to the parasitic effect, the characteristic departs from the ideal responses. But, the parasitic effect can be made negligible satisfying the following condition:

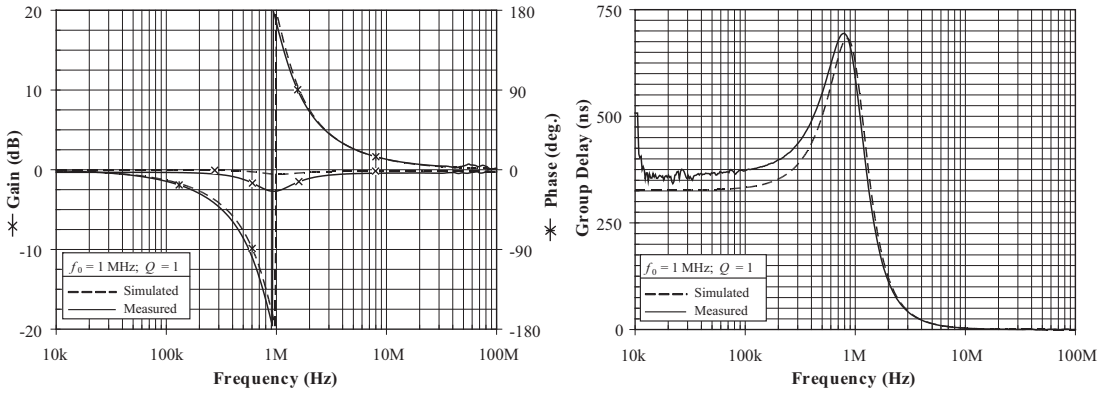
$$\frac{\alpha_{\mathrm{n}} \beta_{\mathrm{n}} G_1 g_m \mu}{C_2 G_2} \ll 1. \tag{5.8}$$

Using the bipolar implementation of the DBTA, the proposed universal filter structure (*Case I*) has been designed for characteristic frequency $f_0 \approx 1$ MHz and the quality factor of filters $Q = 1$, and simulated in SPICE software. The following values have been chosen: $C_1 = C_2 = 150$ pF, $G_1 = G_2 = 1$ mA/V ($R_1 = R_2 = 1$ kΩ) and $g_m = 1$ mA/V ($I_{\mathrm{B}} = 50$ μA). For the practical measurements the DBTA has been implemented by using commercially available amplifiers. The simulation and measurement results of the low- (LP1), band- (BP2), high-pass



(a) (b)

Fig. 5.2: Simulated and measured frequency characteristics for: (a) LP1 and HP1, (b) BP2 and BS responses of the proposed circuit of Fig. 5.1



(a) (b)

Fig. 5.3: Simulated and measured frequency responses of the all-pass (AP) filter: (a) gain and phase responses, (b) group delay response

(HP1), band-stop (BS), and all-pass (AP) frequency filter working in voltage mode are shown in Fig. 5.2 and Fig. 5.3. From the results it is evident that the results of the measurements are in agreement with the simulations. In the higher-frequency region the real properties of the amplifiers and parasitic capacities or inductances of the constructed prototypes begin to be more significant.

6 APPLICATIONS ON GROUNDED INDUCTANCE SIMULATORS

Conventional spiral inductors are too big, too heavy, too costly, and they require tuning. Due to these disadvantages, active element-based inductor design is very desirable to designers today. The positive inductance simulators (PIS) can be used in many applications such as active filter design, oscillator design, analog phase shifters and cancellation of parasitic element [32]. Not only the PIS, but also a negative inductance simulator (NIS) plays an importance role in cancellation/compensation of parasitic inductances. Actively simulated NISs also find in several applications such as in microwave circuits for impedance matching, in chaotic oscillations, in antenna to minimize reflection at the input so that it provides a better radiation pattern, to compensate bond wire inductance which is an increasing problem in high-speed/low-power integrated circuits because of reduced noise margin and cancellation of undesired inductance. It is well known that, unlike capacitance, the magnitude of the negative inductance increases with frequency in the same way as for positive inductances. However, a negative inductance provides a negative 90° phase like a capacitor [36].

6.1 Active-C grounded positive and negative inductor simulators in compact form

The proposed PIS and NIS in this Section (Fig. 6.1) use canonic number of passive and active elements (i.e. single grounded capacitor, single ZC-CCCITA). Using (3.3) and doing routine circuit analysis yields the following input impedances for both the circuits:

$$Z_{in_1} = -Z_{in_2} = sL_{eq} = \frac{sCR_f}{g_m} = \frac{sCV_{\mathrm{T}}^2}{I_{\mathrm{O}}I_{\mathrm{B}}}. \tag{6.1}$$

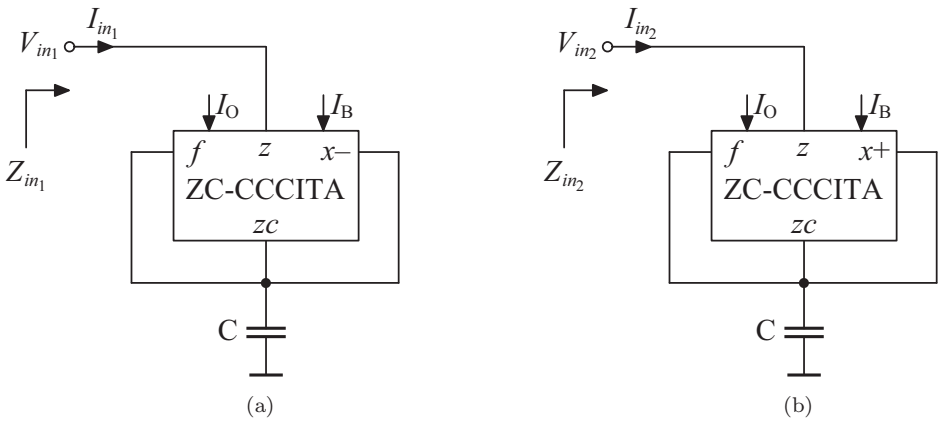


Fig. 6.1: Proposed grounded (a) positive and (b) negative inductance simulators

From (6.1) it is obvious that circuits in Fig. 6.1 represent lossless positive and negative inductor simulators, respectively. In both circuits it can be also clearly seen that the inductance value L_{eq} can be adjusted electronically by either I_{O} and/or I_{B} currents.

Here, the non-ideal analysis will only focus on the grounded PIS circuit (i.e. Fig. 6.1(a)). It is sufficient since in case of the NIS it involves only sign change. Hence, taking into account the non-idealities of the ZC-CCCITA, except for the parasitics R_z and C_z, the input impedance of the circuit from Fig. 6.1(a) is given as:

$$Z'_{in_1} = R_{lossy} + sL_{eq} =$$

$$= \frac{1-\beta_2}{\beta_1 g_m} + \frac{R_f}{\beta_1 g_m (R_{zc}||R_x)} + \frac{s(C+C_{zc}+C_x)R_f}{\beta_1 g_m} =$$

$$= \frac{2V_{\mathrm{T}}(1-\beta_2)}{I_{\mathrm{B}}\beta_1} + \frac{V_{\mathrm{T}}^2}{I_{\mathrm{O}}I_{\mathrm{B}}\beta_1(R_{zc}||R_x)} + \frac{V_{\mathrm{T}}^2 s(C+C_{zc}+C_x)}{I_{\mathrm{O}}I_{\mathrm{B}}\beta_1}. \tag{6.2}$$

This equation clearly indicates that there is a lossy term (resistance) in the simulated impedance and thus the quality factor of the inductor is not infinite. To increase the quality factor of the simulated inductor, the lossy term needs to be minimized and this can be achieved by:

(i) making the β_2 very close to unity (by using high-output resistance current mirrors) and,
(ii) choosing $R_f \ll R_{zc}||R_x$.

Assuming now the lossy term being minimized, the input impedance Z'_{in_1} approximates to the inductance of value $L_{eq} = \frac{(C+C_{zc}+C_x)R_f}{\beta_1 g_m}$. In practice, the external capacitor is chosen such that $C \gg C_{zc} + C_x$.

Till now, we have neglected the effects of parasitics R_z and C_z. Taking into account them we get the input admittance as:

$$Y_{in_1} = \frac{1}{R_z} + sC_z + \frac{1}{sL_{eq}}. \tag{6.3}$$

Assuming the operating frequency $\omega_0 \ll min\left(\frac{R_z}{L_{eq}}, \sqrt{\frac{1}{C_z L_{eq}}}\right)$, the upper frequency potential of the circuit is limited, but the effects of the parasitics on the simulated inductance can be reduced.

Ass application, the passive RLC band-pass filter (BPF) is shown in Fig. 6.2(a) [50] and the appropriate active circuit using the proposed grounded PIS is shown in Fig. 6.2(b). Routine

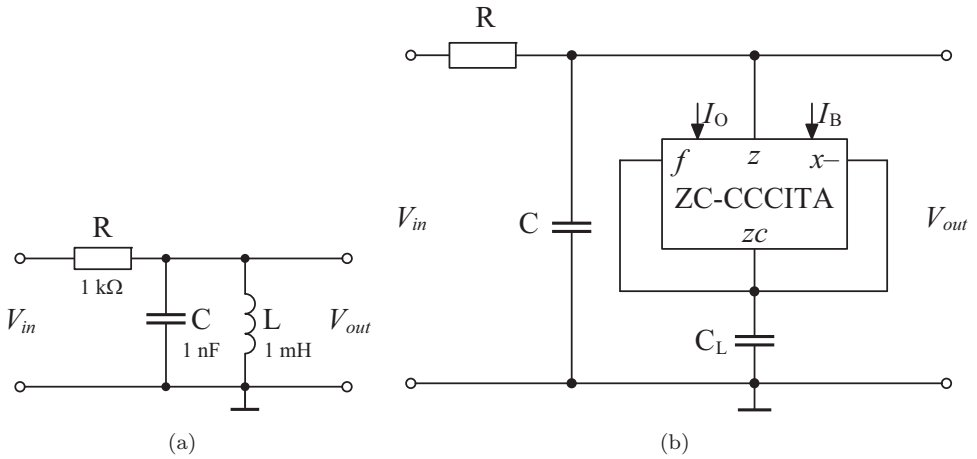


Fig. 6.2: (a) Second-order band-pass prototype and (b) its transformed equivalent circuit diagram

circuit analysis yields the following voltage transfer function of the BPF:

$$K_{\mathrm{BPF}}(s) = \frac{V_{out}}{V_{in}} = \frac{s\frac{1}{CR}}{s^2 + s\frac{1}{CR} + \frac{1}{CL}} = \frac{s\frac{1}{CR}}{s^2 + s\frac{1}{CR} + \frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_LV_{\mathrm{T}}^2}}. \tag{6.4}$$

The denominator of circuits in Fig. 6.2 is identically same, therefore, the natural angular frequency ω_0, the quality factor Q, and the bandwidth BW (ω_0/Q) can be found as:

$$\omega_0 = \frac{1}{V_{\mathrm{T}}}\sqrt{\frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_L}}, \quad Q = \frac{R}{V_{\mathrm{T}}}\sqrt{\frac{I_{\mathrm{O}}I_{\mathrm{B}}C}{C_L}}, \quad BW = \frac{1}{CR}. \tag{6.5}$$

The active and passive sensitivities of the filter parameters are following:

$$S^{\omega_0}_{I_{\mathrm{O}},I_{\mathrm{B}}} = -S^{\omega_0}_{C,C_L} = \frac{1}{2},\ S^{\omega_0}_{V_{\mathrm{T}}} = -1,\ S^{\omega_0}_{R} = 0, \tag{6.6}$$

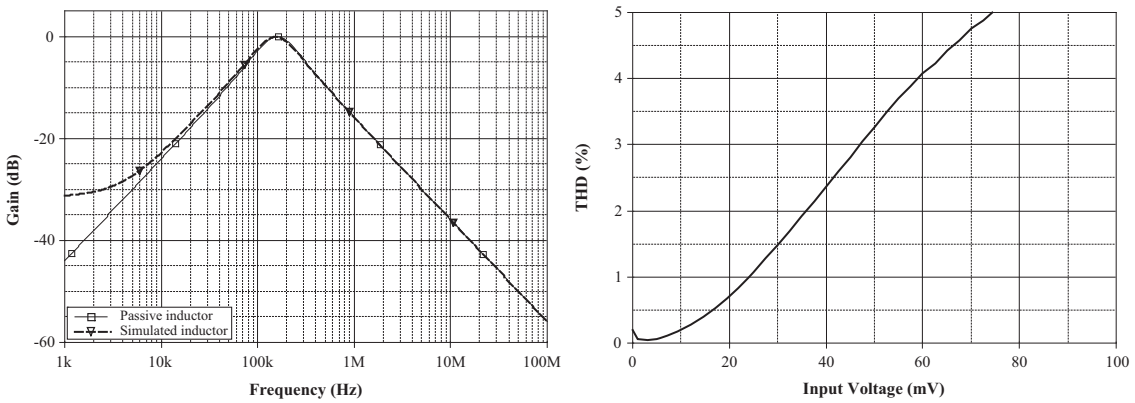
$$S^{Q}_{I_{\mathrm{O}},I_{\mathrm{B}},C} = -S^{Q}_{C_L} = \frac{1}{2},\ S^{Q}_{R} = -S^{Q}_{V_{\mathrm{T}}} = 1, \tag{6.7}$$

$$S^{BW}_{C,R} = -1,\ S^{BW}_{I_{\mathrm{O}},I_{\mathrm{B}},V_{\mathrm{T}},C_L} = 0, \tag{6.8}$$

that are all not more than unity in magnitude.

Using the proposed bipolar implementation of the ZC-CCCITA, the proposed grounded PIS in Fig. 6.1(a) and the second-order voltage-mode band-pass filter from Fig. 6.2(b) has been simulated for the characteristic frequency $f_0 = \omega_0/2\pi \cong 159.15$ kHz and the quality factor $Q = 1$. The passive component values are shown in Fig. 6.2(a). The bipolar implementation of the ZC-CCCITA has been used and in the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [28]. The inductor simulator is realized with the following active parameters and passive element values: $g_m = 1$ mA/V ($I_{\mathrm{B}} = 52$ μA), $R_f = 1$ kΩ ($I_{\mathrm{O}} = 13$ μA), and $C_L = 1$ nF to obtain the required $L = 1$ mH. Ideal and simulated gain responses of the second-order VM BPF are shown in Fig. 6.3(a). In order to investigate distortion of the proposed BPF, the THD at 159.15 kHz has been simulated and the results are shown in Fig. 6.3(b).

The SPICE simulations confirm the feasibility of the proposed PIS and results are in good agreement with theory.



(a) (b)

Fig. 6.3: (a) Ideal and simulated gain responses of the second-order VM BPF, (b) THD of the proposed second-order BPF at 159.15 kHz

7 QUADRATURE SINUSOIDAL OSCILLATORS

The quadrature oscillator (QO) is a circuit that provides two sinusoids with 90° phase difference. Such circuit is frequently used in various applications, i.e. in telecommunications for quadrature mixers and single-sideband generators, for measurement purposes in vector generators or selective voltmeters. Therefore, quadrature oscillators represent an important unit in many communication, control systems, signal processing, instrumentation and measurement systems [30], [56].

7.1 VM SRCO design using generalized CFTA and UGVF

The generalized configuration realizing VM SRCOs using GCFTA and UGVF is shown in Fig. 7.1. Using (3.2) and doing routine circuit analysis, the CE for the circuit topology can be found as:

$$\text{CE:} \quad s^2 C_1 C_2 R_1 R_2 + s C_2 R_2 (1 - a b_1 g_m R_1) - a b_2 g_m R_1 = 0. \tag{7.1}$$

For the above equation to represent a valid CE for an oscillator, the following conditions should be simultaneously satisfied:

$$a b_1 = 1, \quad a b_2 = -1. \tag{7.2}$$

Only two structures confirm these, as described in Tab. 7.1.

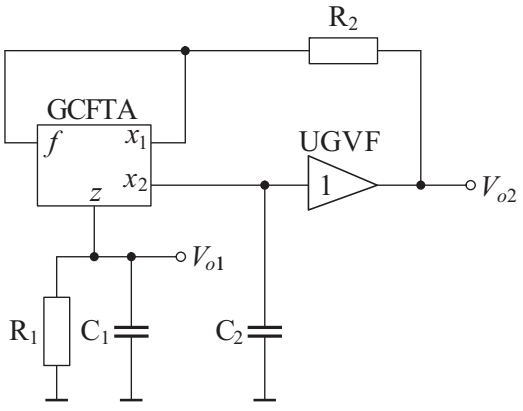


Fig. 7.1: The proposed generalized single-resistance-controlled quadrature oscillator using GCFTA and UGVF

Tab. 7.1: Coefficients of GCFTA

variant	a	b_1	b_2
A	1	1	–1
B	–1	–1	1

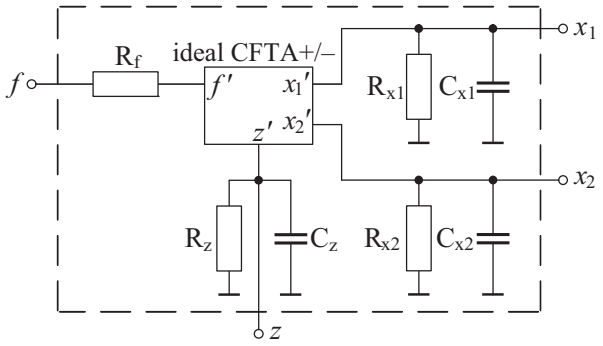


Fig. 7.2: Model of the CFTA+/– including parasitic elements

From (7.1) and (7.2), it is clear that for both the structures A and B, the CO, i.e. the term with s has to be 0 (zero), is:

$$\text{CO:} \quad g_m R_1 \geq 1, \tag{7.3}$$

and the FO is:

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{C_1 C_2 R_2}}. \tag{7.4}$$

It should be pointed out that although (7.3) defines the strict CO, however in practise $g_m R_1$ is made slightly more than unity for the start-up of oscillations. It is evident from (7.3) and (7.4) that the CO can be controlled independently of FO by changing R_1 and the FO can be controlled by means of resistor R_2. Therefore, the circuit truly describes a SRCO. The two quadrature voltage outputs of the general circuit topology as depicted in Fig. 7.1, are related as:

$$V_{o1} = jb_2 k V_{o2}, \quad \text{where} \quad k = \frac{\omega_0 C_2}{g_m}. \tag{7.5}$$

Clearly, for $k = 1$ the two quadrature voltages have equal amplitude.

For a complete analysis, it is important to take into account the non-idealities of the GCFTA. Here, we provide the non-ideal analysis for variant A (i.e. the one using CFTA+/–). The model of the CFTA+/– including parasitic elements is shown in Fig. 7.2. The non-ideal analysis for variant B can be carried on similar lines.

- The non-zero parasitic input resistance at the terminal f is represented by R_f.
- $I_z = \alpha I_f$, where α represents the parasitic current gain, whose ideal value is unity. Similarly, the voltage transfer gain γ for the unity-gain voltage follower (buffer) differs slightly from its ideal value of unity because of the voltage tracking error.
- The parasitic resistance R_z and parasitic capacitance C_z appears between the high-impedance z terminal and ground. The stray/ parasitic capacitance C_z is absorbed into the external capacitance C_1 as it appears in parallel with it. Also, since the value of R_z is in the order of MΩ, hence for an external resistor of value $R_1 \ll R_z$ connected at this terminal, $R_z||R_1 \approx R_1$. Thus, the non-ideal effects of parasitic impedance at terminal z are reduced, if not completely eliminated.
- The parasitic resistance R_{x_2} and parasitic capacitance C_{x_2} appears between the high-impedance x_2 terminal and ground. The parasitic capacitance can be absorbed in the external capacitance C_2, but the presence of parasitic resistance at terminal x_2 would

change the type of the impedance, which should be of a purely capacitive character. A possible solution is to make the operating frequency $\omega_o > \frac{1}{R_{x_2} C_2}$.

- The parasitic resistance R_{x_1} and parasitic capacitance C_{x_1} appears between the high-impedance x_1 terminal and ground. To alleviate the effects of parasitic impedance at terminal x_1, the CFTA should be designed to have a very low input parasitic resistance at terminal f. Ideally, the value of input parasitic resistance at terminal f is zero and terminal f is virtually grounded. Thus, the parasitic impedance at terminal x_1 is connected between a virtual ground and a true ground.

Considering the first non-ideality and the parasitic capacitances at terminal z and x_2, the CO and FO of the proposed SRCO in Fig. 7.1 get modified and are given as:

$$\text{CO:} \quad \alpha g_m R_1 \geq 1, \tag{7.6}$$

and

$$\text{FO:} \quad f_0 = \frac{1}{2\pi} \sqrt{\frac{\alpha\gamma g_m}{(C_1 + C_z)(C_2 + C_{x_2}) R_2}}. \tag{7.7}$$

The sensitivity study indicates that:

$$|S^{f_0}_{\alpha,\gamma,g_m,R_2}| = \frac{1}{2}, \tag{7.8}$$

$$S^{f_0}_{C_1} = -\frac{C_1}{2(C_1 + C_z)}, \tag{7.9}$$

$$S^{f_0}_{C_z} = -\frac{C_z}{2(C_1 + C_z)}, \tag{7.10}$$

$$S^{f_0}_{C_2} = -\frac{C_2}{2(C_2 + C_{x_2})}, \tag{7.11}$$

$$S^{f_0}_{C_{x_2}} = -\frac{C_{x_1}}{2(C_2 + C_{x_2})}. \tag{7.12}$$

It is evident from (7.8)–(7.12) that the magnitude values of all f_0 sensitivities are less than unity and hence the proposed SRCO exhibits an attractive sensitivity performance. Also, both the CO and the FO in (7.6) and (7.7) are subject to process and temperature variations, to the presence of g_m term in the expressions. Similar tuning laws are also present in [39] and [33]. This should not be seen as a drawback for the FO, since the designer can control it using R_2. For the CO, a common practice is to make $R_1 > \frac{1}{g_m}$, so that even for any changes in the right-hand side value (g_m) the inequality is satisfied and there is an appropriate start-up of the oscillations. For more accurate tuning, the external resistors could be replaced by non-linearity canceled MOSFETs (working in triode region) [57]. This shall provide electronic tuning properties via gate voltages to both the CO and FO and a voltage-controlled oscillator (VCO) is created.

In order to confirm the above given theoretical analysis, the proposed CFTA-based SRCO (variant A) has been simulated with SPICE simulation program. The bipolar implementation of the CFTA+/– and the bipolar implementation of the UGVF, presented in [48] as output stage of CFOA, has been used with the DC supply voltages of $+V_{CC} = -V_{EE} = 2$ V. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [28]. The maximum value of terminal voltage of the UGVF without producing significant distortion is in the full scale of the supply voltage (in this case ±2 V). The DC voltage gain of the UGVF $\gamma \cong 0.9992$ with bandwidth $f_\gamma \cong 3.971$ GHz.

The proposed circuit was designed using the following component values: $C_1 = C_2 = 10$ nF, $R_2 = 1$ kΩ, and $g_m = 1$ mS ($I_B = 52$ μA). The value of R_1 is kept slightly more than 1 kΩ

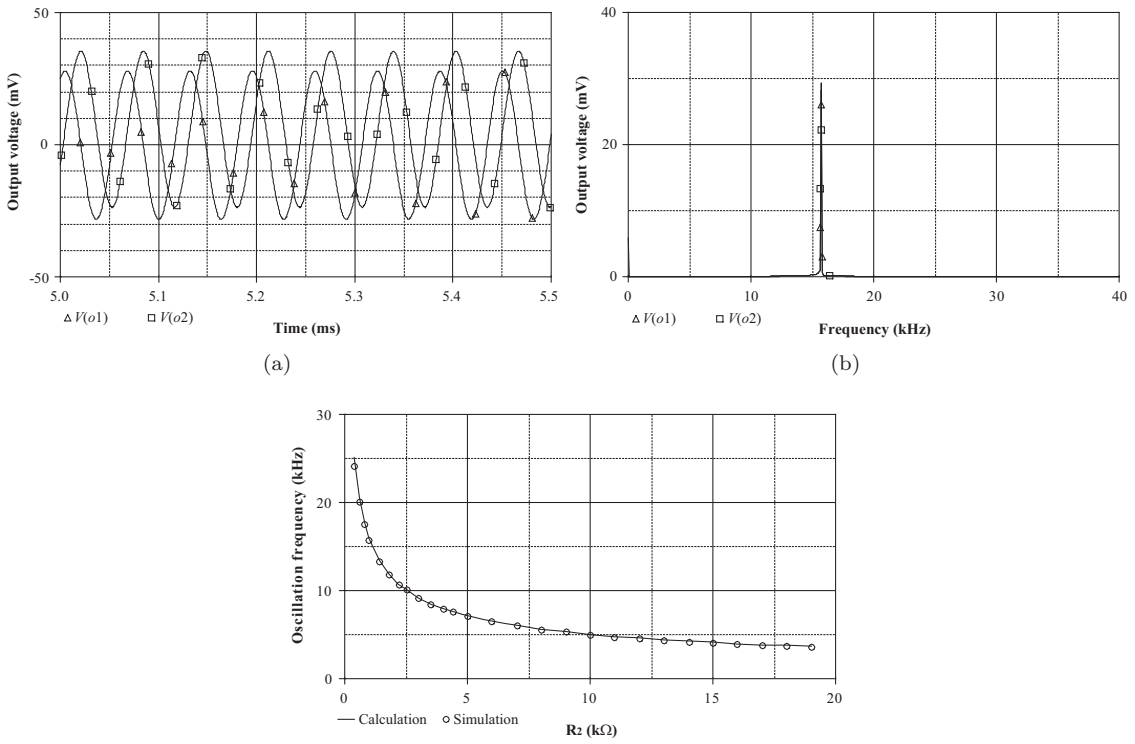


Fig. 7.3: (a) Quadrature voltage outputs V_{o1} and V_{o2} during steady stage, (b) simulated frequency spectrums of outputs V_{o1} and V_{o2}, (c) variation of oscillation frequency with R_2

to start the oscillations. The simulated output waveforms for V_{o1} and V_{o2} at steady stage are shown in Fig. 7.3(a). It is evident from Fig. 7.3(a) that the proposed circuit provides nearly equal sinusoidal waves and which is in accordance with (7.4). The offset (about 12 mV) of the V_{o2} is caused by the simple structure of the UGVF used [48] that does not enable suppress this parameter. Fig. 7.3(b) shows the frequency spectrum of the output waveforms and the value of THD at both the outputs are 1.67%. The variation of FO with resistor R_2 without affecting the CO is shown in Fig. 7.3(c) and it is seen that the simulated values exhibit a close correspondence with the theoretical predictions.

8 CONCLUSION

In the last decade, for analogue signal processing huge number of active building blocks were introduced, however, there is still the need to develop new active elements that offer new and better advantages. Therefore, the main contribution of this thesis was the definition of such novel ABBs, and their application possibilities.

Chapter 3 presents various active elements and introduces novel ones, such as the differential-input buffered and transconductance amplifier (DBTA), the current follower transconductance amplifier (CFTA), the z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA), the generalized current follower differential input transconductance amplifier (GCFDITA), the voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA), and the minus-type current-controlled third-generation voltage conveyor (CC-VCIII–).

Using the proposed ABBs, in Chapter 4, novel structures of first-order all-pass filters are proposed. Chapter 5 presents novel structures of second-order universal filters, KHN-equivalent circuits, and inverse filters. Active grounded inductor simulators are discussed in Chapter 6, and in the Chapter 7 various quadrature sinusoidal oscillators are proposed. The

proposed circuit work in the current-, voltage-, or mixed-mode and their comparison can be found in Appendix B.

To verify the behavior of the proposed circuits, all defined active elements are implemented using either bipolar or CMOS internal structure. The feasibility of selected circuits is also confirmed by experimental measurements.

Here, it is worth mention that part of this work has already been published in journals with impact factor (10 papers in the following journals: International Journal of Electronics, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, IEICE Electronics Express, and AEU - International Journal of Electronics and Communications) and presented at international conferences (17 papers): PWC'07 (12th IFIP International Conference on Personal Wireless Communications, Prague, Czech Republic), TELFOR'08 (16th Telecommunications Forum, Belgrade, Serbia), ICONS'08 (Third International Conference on Systems, Cancun, Mexico), APPEL'08, APPEL'09, and APPEL'10 (Applied Electronics, Pilsen, Czech Republic), NCSP'09 (RISP International Workshop on Nonlinear Circuits and Signal Processing, Honolulu, Hawaii, USA), ELECO'09 (6th International Conference on Electrical and Electronics Engineering, Bursa, Turkey), TSP'08 (International Conference on Telecommunications and Signal Processing, Paradfurdo, Hungary), TSP'09 (32th International Conference on Telecommunications and Signal Processing, Dunakiliti, Hungary), TSP'10 (33th International Conference on Telecommunications and Signal Processing, Baden near Vienna, Austria), and CSS'10 (4th International Conference on Circuits, Systems and Signals, Corfu Island, Greece).

Moreover, here it should be also noticed that my works have received 12 citations from international researchers (for more details, please refer my CV).

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- *FRVS 1648/2008/G1*: Support of experimental works in Bachelor Theses. Holder: Mr. Herencsár
- *FRVS 2057/2008/F1a*: Support of experimental works in Diploma Theses on study programme Telecommunications and Information Technologies. Holder: Assoc. Prof. J. Misurec

Project supported by the European Union
- *OP VK CZ.1.07/1.3.10/02.0018*: Complex educational programme in the field of ICT for the employees of South-Moravian schools. Holder: Assoc. Prof. K. Molnar

Project supported by the Brno University of Technology
- *FEKT-S-10-16*: Research of communication systems and networks. Holder: Prof. K. Vrba

Memberships in Professional Societies and Committees

Since 2007 :

Student Member of the Institute of Electrical and Electronic Engineers (IEEE)
Member of the International Association of Engineers (IAENG)

Since 2008 :

Organizing Committee Member of the International Conference on Telecommunications and Signal Processing (TSP)

Since 2009 :

Member of the Association of Computer, Electronics and Electrical Engineers (ACEEE)
Member of the International Association of Computer Science and Information Technology (IACSIT)

Since 2010 :

Editorial Board Member of the International Journal of Computer and Electrical Engineering (IJCEE)
PC Chair Member of the International Conference on Computer and Automation Engineering (ICCAE)

Since 2011 :

PC Chair Member of the International Conference on Network and Computational Intelligence (ICNCI)

Invited Reviewer

Invited reviewer for the following scientific Journals and Conferences:

- IEEE Transactions on Instrumentation & Measurement
- International Journal of Electronics
- IET Circuits, Devices & Systems
- Circuits, Systems & Signal Processing
- International Journal of Computer and Electrical Engineering
- Elektrorevue - Internet Journal
- International Conference on Advances in Computing, Control, and Telecommunication Technologies (ACT 2009)
- International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2009)
- 32nd International Conference on Telecommunications and Signal Processing (TSP 2009)
- 4th WSEAS International Conference on Circuits, Systems, Signal and Telecommunications (CISST 2010)
- 12th WSEAS International Conference on Networking, Vlsi and Signal Processing (ICNVS 2010)
- 33rd International Conference on Telecommunications and Signal Processing (TSP 2010)

Results in Total

Citations: 12
Paper Reviews: 32
h-index according to Web of Science: 3
Publications: 60

- *Number of accepted or published papers in a journal with Impact Factor:* **11**
- *Number of accepted or presented papers at international conferences:* **31**
- *Other journal publications:* **18**

Award/Nomination: 2

- The paper entitled "Multifunction RF Filters Using OTA", presented at the *12th IFIP International Conference on Personal Wireless Communications - PWC'07*, Prague, Czech Republic, received Best Paper Awards.
- The paper entitled "Generalized design method for voltage-controlled current-mode multifunction filters", presented at the *16th Telecommunications Forum - TELFOR'08*, Belgrade, Serbia, was nominated for "Blazo Mircevski" Award granted for the best paper of a young TELFOR author (http://2008.telfor.rs/nagrade/).

Last update: August 4, 2010

ABSTRACT

Frequency filters and sinusoidal oscillators are linear electric circuits that are used in wide area of electronics and also are the basic building blocks in analogue signal processing. In the last decade, huge number of active building blocks (ABBs) were presented for this purpose. In 2000 and 2006, the universal current conveyor (UCC) and the universal voltage conveyor (UVC), respectively, were designed at the Department of Telecommunication, BUT, Brno, and produced in cooperation with AMI Semiconductor Czech, Ltd. There is still the need to develop new active elements that offer new advantages. The main contribution of this thesis is, therefore, the definition of other novel ABBs such as the differential-input buffered and transconductance amplifier (DBTA), the current follower transconductance amplifier (CFTA), the z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA), the generalized current follower differential input transconductance amplifier (GCFDITA), the voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA), and the minus-type current-controlled third-generation voltage conveyor (CC-VCIII–). Using the proposed ABBs, novel structures of first-order all-pass filters, second-order universal filters, KHN-equivalent circuits, inverse filters, active grounded inductance simulators, and quadrature sinusoidal oscillators working in the current-, voltage-, or mixed-mode are presented. The behavior of the proposed circuits has been verified by SPICE simulations and in selected cases also by experimental measurements.