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Mem-Elements Emulator Design With Experimental Validation and Its Application

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ABSTRACT An emulator circuit of Memristor, Memcapacitor, and Meminductor commonly termed as mem-elements has been demonstrated in this article. The circuit has been realized using the technique of current mode, which provides better performance over voltage mode counterparts. The current mode analog building blocks, along with a few passive components, have been used in the presented circuit implementation. The fingerprint characteristics have been observed in both simulation and experimental results, validating the theoretical analysis. The robustness of the presented design has been supported by performing different types of analysis like process corner, temperature, and non-volatility behavior. The mem-elements emulator design has been simulated using 0.18 μm TSMC process parameter, and $\pm$1.2 V power supply has been used. The commercial ICs AD844 and CA3080 are used for the experimental demonstration of the proposed mem-elements design by making a prototype on a breadboard. A layout area of 4829 μm^2, 8098 μm^2, and 8061 μm^2 respectively is required for the Memristor, Memcapacitor, and meminductor circuit. The power consumed by the mem-elements circuit is also provided. A chaotic has been implemented using mem-elements to show the usefulness of the emulator design.

INDEX TERMS Memristor, memcapacitor, meminductor, pinched hysteresis loop, Chua's circuit.

I. INTRODUCTION

Memristor was originally postulated by Leon Chua in 1971 as the fourth passive circuit element describing the missing relationship between the magnetic flux (φ) and electric charge (q). The unique non-linear feature of the Memristor [1]–[6] was not observed in the existing basic passive elements. Chua's paper caught the attention of worldwide researchers after the announcement of memristor fabrication in Hewlett-Packard (HP) laboratories using TiO_2 [1] by Williams *et al.* in 2008. The ideal characteristics of the memristive system [3]–[5] were postulated and derived by Kang. Memristor possesses three main characteristics [6], which can be stated as (a) pinched hysteresis loop in the current-voltage plane (b) an inverse relationship between the hysteresis curve area and frequency (c) memristor behaves like a linear resistor at high frequency. Non-volatility is an important characteristic of an ideal memristor defined by preserving the memristance value when no input signal is applied. The emulator corresponds to a circuit that imitates the mem-element characteristics. Memcapacitor and Meminductor [4] have been derived from the concept of Memristor and possess similar properties of storing energy by virtue of its capacitance and inductance without power source requirement. The analog memory field finds newer technology advancements with the introduction of these mem-elements having wide application areas such as chaotic signal generators [7], [8], and many more. The relation of the time integral of charge ($\sigma(t)$) against the time integral of voltage ($\varphi(t)$) is the nature of memcapacitive elements. Meminductor has been put under the special category of memory element wherein the flux is taken as the time integral of induced voltage across the inductor. The memristor [9]–[14] emulator design in literature consists of several analog building blocks. In [9], the memristor circuit consists

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of 1 CBTA and 1 multiplier with few passive components which can work in only grounded conditions. The memristor circuit in [10] has been designed using MO-OTA having 3 ended outputs with few passive components, but it can only be configured in decremental configurations. In [11], the memristor design has been implemented using CCTA and CCII as an active block with few passive components which can work in only floating conditions. The memristor circuit using 2 CFOAs and 1 OTA with few passive components has been designed in [12], but it can only be configured in incremental configuration. In [13], BJT-based implementation of the memristor circuit has been done using 2 AD844 and 1 multiplier. The memristor design in [14] consists of CCII and OTA, but it can work in only grounded conditions. In this article, a memristor circuit has been proposed, which can be configured in both grounded as well as floating conditions and can be made to operate in both incremental as well as decremental configurations. The memcapacitor emulator [15]–[22] circuit in literature has been designed using different active blocks such as DXCCDITA [15], 4 CCIIs and 1 Op-amp [16], 3 CCIIs, 3 TOAs and 1 MR [17], 2 CCIIs, and 1 multiplier [18], 2 CCIIs and 1 MR [19], first design with 2 CCIIs, 1 multiplier and second design with CCII, OTA, multiplier [20] and 2 MO-OTAs and 1 multiplier [21]. The existing circuit in literature comprises either more number of active block or contains a multiplier, which makes the design complex, and it supplies around $1/10^{\text{th}}$ of the product term that eventually results in a reduced loop area of the hysteresis curve. The memcapacitor design proposed in this article consists of 2 CCII and 1 OTA with few passive components without using any mutator or multiplier circuit. The meminductor [22]–[26] emulator circuit in literature has been designed using different analog active building blocks. The meminductor circuit in [22]–[25] consists of either a BJT-based circuit using more than one type of active block or a mutator-based design. In [26], the meminductor emulator has been designed using two OTAs out of which one simple output and one multi-output, one grounded capacitor and one floating capacitor, one grounded and one floating resistor, an analog multiplier. The circuit uses more commercial ICs to perform the experimental validation. The presented mem-elements circuit in [32] is complex due to the presence of more ICs and discrete components. The meminductor emulator design proposed in this article comprises 2 CCII and 1 OTA with few passive components and experimentally validated. Memristor (MR), memcapacitor (MC), and meminductor (MI) are commonly known as mem-elements. The design and implementation difficulty in fabricating these nanoscale devices is the main hurdle in the path of the emergence of these mem-elements in the near future. Hence, the study of simulation models and emulator circuits is necessary for exploring the application of these three mem elements. The application of mem-elements to chaotic [7], [8] circuits is an important research topic. Various chaotic oscillations have been generated by introducing a memristor emulator to different chaotic circuits. The characteristics of Memcapacitor and Meminductor supported by the simulation results indicate the potential of these mem-elements in chaotic and hyperchaotic phenomena.

The objective of this paper is to provide the circuit implementation of all three mem-elements and their simulation and experimental validation. The proposed mem-elements design can be used to explore the real-world application without the need for a mutator. Moreover, the layout of the emulator design has been laid out, and the consumed chip area has been provided. At the same time, the power consumed by these mem-elements has also been provided. The presented design has been used in the implementation of the chaotic circuit for secure communication in order to show the usefulness of the design.

II. BUILDING BLOCK AND ITS PROPERTIES

The current mode circuit provides better performance to rival its voltage mode counterparts in a wide range of applications. The technique of the current-mode circuit has been utilized in the implementation of the presented mem-elements emulator design. Unlike their voltage mode counterparts, current conveyors offer high linearity, have a wider dynamic operating range, high-frequency range, and have a unity gain magnitude response. A CCII [28]–[31] is a three-terminal active element whose port relationship is given as

$$I_Y = 0, \quad V_X = V_Y, \quad I_Z = I_X \tag{1}$$

Ideally, Z and Y nodes show infinite impedance, whereas the X node has a zero impedance. The input stage is the translinear voltage follower and an important part of CCII to obtain a large dynamic range. The output Z copies the current flowing through port X and is realized in the conventional manner using two complementary mirrors as current follower. The OTA is a voltage-controlled current source whose differential input voltage yields an output current by means of its transconductance (g_m). The port relationship and transconductance parameter of OTA is given by

$$I_{O\pm} = \pm g_m \left(V_P - V_N\right), g_m = \frac{k}{\sqrt{2}} \left(V_B - V_{ss} - 2V_{th}\right) \tag{2}$$

where k is a parameter of MOS device given by

$$k = \mu_n C_{OX} \frac{W}{L}$$

Here, μ_n denotes the carrier mobility in the channel region while W/L and C_{OX} are the aspect ratio and oxide capacitance per unit area of the MOSFET, respectively. The CMOS-based schematic structure of CCII [28]–[31] and M-OTA [27] has been shown in Figure. 1 and Figure. 2, which is used to design the mem-elements emulator circuits. The aspect ratio of the MOS transistors used in the implementation of CCII and M-OTA is given in Table-1.

III. MATHEMATICAL MODEL OF MEM-ELEMENTS AND CIRCUIT DESCRIPTION

In this section, mem-elements emulator circuit design has been proposed, which consists of CCII and OTA as an analog

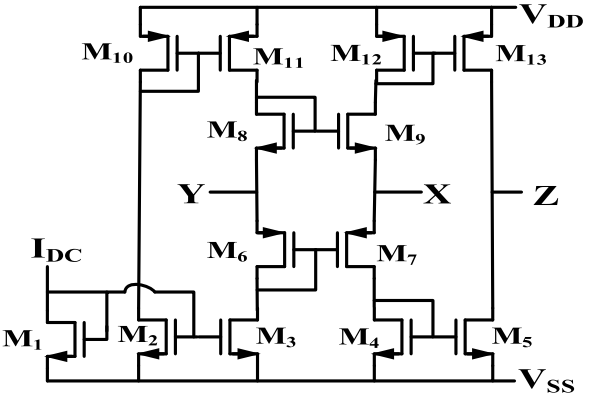

FIGURE 1. CMOS schematic structure of CCII.

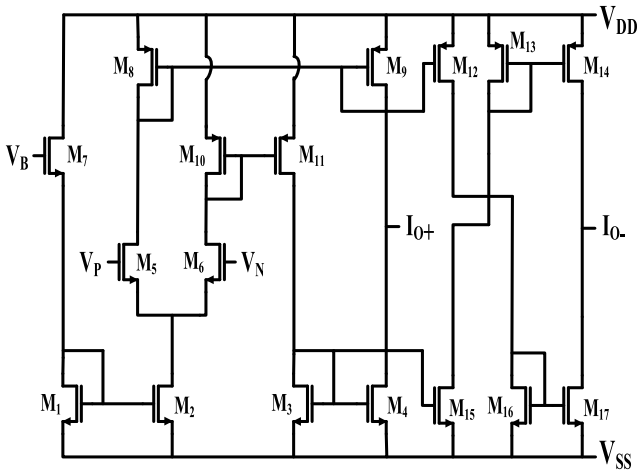

FIGURE 2. CMOS schematic structure of M-OTA.

TABLE 1. Aspect ratio of MOS transistors.

	Transistors	W/L (µm)
CCII	M_1 - M_5	7/0.35
	M_6 - M_7	37.8/0.35
	M_8 - M_9	4/0.35
	M_{10} - M_{13}	27/0.35
M-OTA	M_1 - M_4	14/0.5
	M_5 - M_7	4/0.5
	M_8 - M_{11}	17/0.37
	M_{12} - M_{14}	18/0.37
	M_{15} - M_{17}	12/0.37

active building block with few passive elements, and their mathematical model has been discussed. The connections at the input terminal of OTA are interchanged in order to operate the emulator circuit in incremental and decremental configurations. The Memcapacitor and Meminductor emulator design has been presented without using the mutator or multiplier in order to explore the follow-up application of these mem-elements such as compatible memory elements for real-time applications.

A. MEMRISTOR

The presented circuit of a memristor emulator circuit design can be configured to work in both floating and grounded types and can operate in both incremental and decremental modes by interchanging the switch connected at the input terminal of OTA. The grounded circuit of a memristor emulator [24] has been extended by replacing OTA with multiple output OTA, and thus the circuit works in both floating and grounded environments. The incremental and decremental configuration has been provided by connecting the switch S to N terminal for incremental and switch S to P terminal for decremental while another input terminal of OTA is grounded. The proposed design of the emulator has been shown in Figure. 3. Considering the ideal behavior of the circuit operating in the incremental mode, A and B is the floating terminal of the presented design, the routine analysis yields the potential developed at the Z terminal of CCII is equal to the biasing voltage of M-OTA [27]. The potential at these terminals can be written as

$$V_Z = V_B = \frac{\varphi_{in}}{RC} \tag{3}$$

Since the switch is connected at the N terminal of M-OTA, the current flowing through the output terminal (O+) of M-OTA is the same but opposite in polarity to that of the input current. Using the transconductance equation (2), the memductance offered by the floating type Memristor emulator circuit in its incremental mode of operation can be written as

$$W(\varphi_m) = \frac{I_{in}}{V_{in}} = -\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th}) + \frac{k}{\sqrt{2}}\frac{\varphi_{in}}{RC} \tag{4}$$

The grounded memristor design can be obtained by shorting terminal B to the ground. It can be deduced from equation (4) that the voltage or current signal applied across the Memristor controls the memductance value. The memductance consists of time-invariant and time-variant parts. The time-variant part

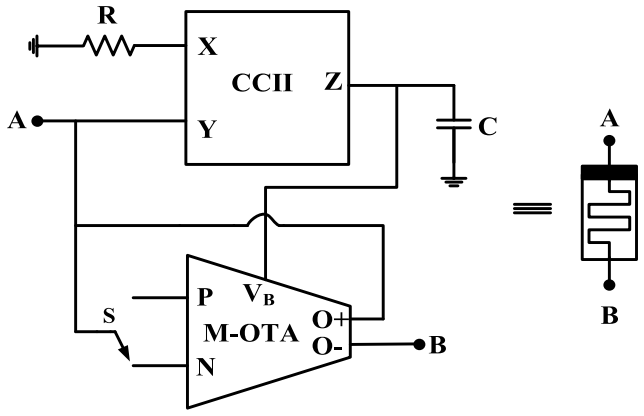

FIGURE 3. Flux-controlled memristor emulator circuit.

depends on the flux (φ_{in}), so it is flux controlled memristor emulator. The general expression of memductance for both incremental/decremental configuration for floating/grounded type emulator can be written as

$$W(\varphi_m) = \frac{I_{in}}{V_{in}} = \mp\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th}) \pm \frac{k}{\sqrt{2}}\frac{\varphi_{in}}{RC} \quad (5)$$

Negative sign in time-invariant part and positive sign in time-variant part corresponds to incremental configuration while positive sign in time-invariant part and negative sign in time-variant part corresponds to decremental configuration. Frequency response analysis of the presented memristor design has been performed when a sinusoidal signal $V_{in}(t)=A_m\sin(\omega t)$ has been applied where A_m is the amplitude of the input signal, and $\omega=2\pi f$ is taken as the frequency value so as to study the frequency characteristics of the proposed Memristor emulator design. The memductance equation becomes

$$W(\varphi_m) = -\frac{k}{\sqrt{2}}(V_{SS} + 2V_{th}) + \frac{kA_m\cos(\omega t - \pi)}{2\sqrt{2}\pi fRC} \quad (6)$$

It can be observed from equation (6) that there is an inverse relation of the time-variant part with frequency and capacitor. Therefore, the time-invariant part dominates over the time-variant part when the frequency is increased i.e., the Memristor starts to act like a linear resistor. Considering nonidealities and parasitic impedances present at the terminal of the analog building block, the port relationship of these blocks can be written as

$$I_Y = 0, V_X = \alpha V_Y, I_Z = \beta I_X, I_{O\pm} = \pm g_m(\gamma_1 V_P - \gamma_2 V_N) \quad (7)$$

Ideally, the parasitic capacitances and resistances present in parallel to the terminals of the CCII and OTA are approximately equal to zero and infinity, respectively. The parasitic impedance at the X terminal of CCII tends to zero ideally. The parasitic resistances, capacitances, and nonidealities due to mismatching of transistors will influence the overall performance of the design. $R_{eq}=R+R_X$ and $C_{eq}=C+C_z+C_{VB}$ represent the equivalent resistance and capacitance. The memductance equation considering these parameters can be written as

$$W(\varphi_m) = \left(\frac{\alpha\beta\varphi_{in}}{R_{eq}C_{eq}} - V_{SS} - 2V_{th}\right)\frac{k\gamma_{2+}}{\sqrt{2}} \quad (8)$$

It can be observed from equation (8) that the value of memductance is more affected at higher frequencies due to these errors and least affected at a lower frequency.

B. MEMCAPACITOR

The presented charge-controlled Memcapacitor emulator circuit has been designed using 2 CCII and 1 OTA with few passive elements. The general form of the charge controlled memcapacitor emulator with initial value as β and incremental/decremental term as α approximated as $(\beta \pm \alpha\sigma(t))q(t)$. OTA plays a crucial role as a multiplier by exploiting the transconductance stage to attain the general form. The proposed design of Memcapacitor has been shown in Figure. 4. The incremental and decremental configuration has been provided by connecting the switch S to P terminal for incremental and switch S to N terminal for decremental while another input terminal of OTA is grounded.

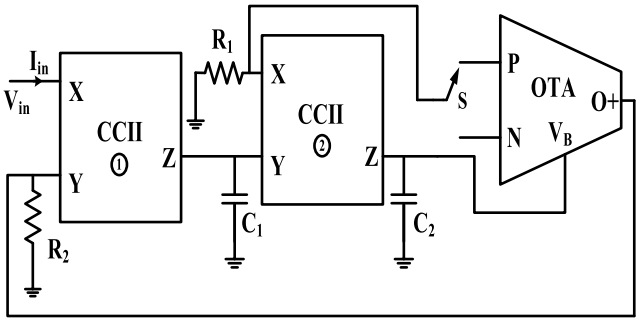

FIGURE 4. Charge-controlled memcapacitor emulator circuit.

Considering the ideal behavior of the circuit operating in the incremental mode, the routine analysis yields that the current at terminal X and Z of CCII-1 is the same using port relationship equation (1), and this current is equal but 180° out of phase with the input current I_{in}. The current at the Z terminal of CCII-1flows into the capacitor C_1 since the Y terminal of CCII-2 is at high impedance, and therefore a potential is developed across the capacitor C_1. The voltage at terminal X and Y of CCII-2 is equal to the voltage produced across capacitor C_1 since the Z terminal of CCII-1 is sorted with the Y terminal of CCII-2. The potential at these terminals can be written as

$$V_{Z1} = V_{Y2} = V_{X2} = -\frac{1}{C_1}\int I_{in}dt = -\frac{q(t)}{C_1} \quad (9)$$

The current at terminal X and Z of CCII-2 is equal, and this current flows into the capacitor C_2, and as a result, a potential is developed across the capacitor C_2. The terminal Z of CCII-2 is sorted with the controlling voltage V_B of OTA, and therefore the potential at these terminals is the same and can be written as

$$V_{Z2} = V_B = -\frac{1}{C_2}\int\frac{q(t)}{R_1C_1}dt = -\frac{\sigma(t)}{R_1C_1C_2} \quad (10)$$

where $\sigma(t)$ is the time integral of charge in the above equation. The terminal X of CCII-2 is sorted with the terminal P of OTA in case of incremental configuration while another input terminal of OTA is grounded, and therefore the voltage at these terminals is the same as written in equation (9). The output current of OTA can be written as

$$I_O = g_m(V_P - V_N) = -g_m\frac{q(t)}{C_1} \quad (11)$$

Using the transconductance (g_m) expression written in equation (2) of OTA and replacing the value of V_B with equation (10) in it, the equation (11) can be re-written as

$$I_O = -\frac{k}{\sqrt{2}}\left(-\frac{\sigma(t)}{R_1C_1C_2} - V_{SS} - 2V_{th}\right)\frac{q(t)}{C_1} \quad (12)$$

The output terminal of OTA is sorted with the Y terminal of CCII-1, which is at high impedance. Therefore, the output current of OTA flows into the resistor R_2 and a voltage is developed across the resistor R_2. Using the port relationship written in equation (1), the voltage at terminal Y and X of CCII-1 is the same and it is equal to the applied input voltage. The potential at these terminals can be written as

$$V_{in} = V_{Y1} = \frac{kR_2q(t)}{\sqrt{2}C_1}(V_{SS} + 2V_{th}) + \frac{kR_2\sigma(t)q(t)}{\sqrt{2}R_1C_1^2C_2} \quad (13)$$

On rearranging equation (13), the value obtained for memcapacitance is written as:

$$C_M^{-1}(q(t)) = \frac{V_{in}}{q(t)} = \frac{kR_2}{\sqrt{2}C_1}(V_{SS} + 2V_{th}) + \frac{kR_2\sigma(t)}{\sqrt{2}R_1C_1^2C_2} \quad (14)$$

It can be observed from equation (14) that the obtained memcapacitance follows the general form of charge-controlled Memcapacitor. In order to analyze the frequency behavior of the presented memcapacitor design, the emulator circuit is excited with an input current such that the charge developed across the Memcapacitor is $q(t) = V_M \sin(\omega t)$ where V_M and ω represent respectively the signal amplitude and operating frequency. The equation (14) can be re-written as

$$C_M^{-1}(q(t)) = \frac{kR_2}{\sqrt{2}C_1}(V_{SS} + 2V_{th}) + \frac{kR_2V_M}{\sqrt{2}R_1C_1^2C_2\omega}\cos(\omega t - \pi) \quad (15)$$

It can be observed that equation (15) consists of linear time-varying and time-invariant parts. The linear time-variant part is inversely proportional to the frequency and therefore the linear time-invariant portion shows clear dominance over the linear time-variant counterpart as the frequency is increased. With frequency tending to infinity, the linear nature of the curve is produced between the charge and voltage. The magnitude of the time-variant memcapacitance term can be written as

$$C_M^{-1}(q(t)) = \frac{kR_2V_M}{\sqrt{2}R_1C_1^2C_2\omega} = \frac{1}{\tau f} \quad (16)$$

where $\tau = 2\sqrt{2}\pi R_1C_1^2C_2/kR_2V_M$ represents the time constant of the Memcapacitor. It is this time constant that is responsible for controlling the loop area of the pinched hysteresis loop. Following cases shows the relationship between the time constant and input frequency:

1. When the frequency tends to infinity, the time-varying linear resistance vanishes that in turn reduces the Memcapacitor to its original capacitor behavior.
2. When $\tau = 1/f$ indicates that the time constant and the input frequency are matched, leading to maximum pinched hysteresis loop.
3. When $\tau \leq 1/f$ indicates that the time constant of the Memcapacitor is fairly less than the frequency of the applied signal which eventually reduces the pinched hysteresis loop.

Considering nonidealities and parasitic impedances present at the terminal of the analog building block in equation (7), the memcapacitance equation can be written as

$$C_M^{-1}(q(t)) = \left(\frac{\alpha_2\beta_1\beta_2\sigma(t)}{R_{eq1}C_{eq1}C_{eq2}} + V_{SS} + 2V_{th}\right) \times \frac{k\alpha_1\alpha_2\beta_1\gamma_1R_{eq2}}{\sqrt{2}C_{eq1}} \quad (17)$$

where $R_{eq1}=(R_1+R_X)\,R_P$, $R_{eq2}=R_O+R_{Y1}$, $C_{eq1}=C_1+C_{Z1}+C_{Y2}$, $C_{eq2}=C_2+C_{Z2}+C_{VB}$. It can be observed from equation (17) that the value of memcapacitance is more affected at higher frequencies due to these errors and least affected at a lower frequency. The memcapacitor can be designed as either a voltage-controlled memcapacitive system or charge controlled memcapacitive system. The circuit design can be implemented using both mechanisms and provides comparative results.

C. MEMINDUCTOR

The proposed flux-controlled Meminductor emulator circuit comprises two CCII along with a single OTA in addition to few passive components. Meminductor is amongst the three mem-elements having constitutive parameters such as flux ($\varphi(t)$), ($\rho(t)$) which is the integration of flux with respect to time and current ($I(t)$). The most common representation of the flux controlled Meminductor with initial values (β) along with an incremental/decremental part (α) is governed by relation $I(t)=(\beta \pm \alpha\rho(t))\varphi(t)$. Capacitor plays a crucial role in providing the time integral of flux. The integration of voltage (φ) with respect to the time and time integral of flux (ρ) is essential for implementing the Meminductor circuit. The presented design of the Meminductor emulator circuit has been shown in Figure. 5. The circuit can be configured in both incremental and decremental configurations by connecting the switch S to N terminal for incremental and switch S to P terminal for decremental while another terminal of OTA is grounded.

Considering the general model and ideal behavior of the circuit operating in the incremental mode, the routine analysis

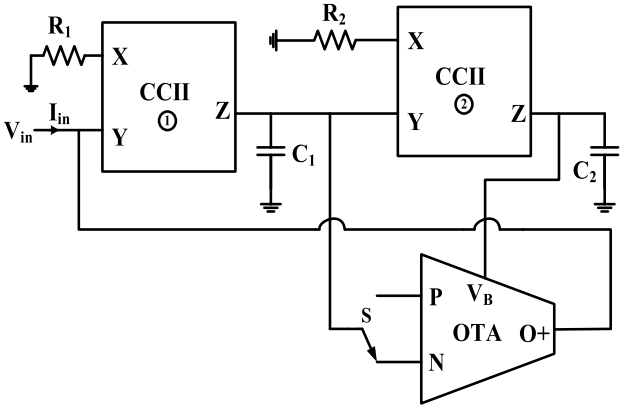

FIGURE 5. Flux-controlled meminductor emulator circuit design.

yields the same voltage at the X and Y terminal of CCII-1 using the port relationship equation (1), and this voltage is equal to the applied input voltage. The current at terminal X of CCII-1 can be evaluated using resistor R_1 and the same current flows at terminal Z of CCII-1. Since the Z terminal of CCII-1 and Y terminal of CCII-2 is sorted and the Y terminal is at high impedance, therefore Z terminal current flows into the capacitor (C_1), and a voltage is developed across it. The voltage at terminal X and Y of CCII-2 is equal to the voltage across the capacitor (C_1) using the port relationship. The voltages at these terminals can be written as

$$V_{X2} = V_{Y2} = V_{C1} = \frac{1}{C_1}\int \frac{V_{in}}{R_1}dt = \frac{\varphi_{in}}{R_1 C_1} \tag{18}$$

The current at terminal X and Z of CCII-2 is the same and can be evaluated by using resistor R_2. The current at terminal Z of CCII-2 flows into the capacitor (C_2), and potential is developed across it. The terminal Z of CCII-2 is sorted with the externally controlled terminal V_B of OTA, and therefore same voltage appears at these terminals, which can be written as

$$V_{Z2} = V_B = V_{C2} = \frac{1}{C_2}\int \frac{\varphi_{in}}{R_1 R_2 C_1}dt = \frac{\rho(t)}{R_1 R_2 C_1 C_2} \tag{19}$$

The switch S is connected to terminal N of OTA for incremental configuration while the P terminal is grounded. The potential at terminal N of OTA is equal to the voltage across the capacitor (C_1) given in equation (18). The output current of OTA is the same but opposite in polarity to that of the input current. The current at these terminals can be written as

$$I_O = -I_{in} = -g_m \frac{\varphi_{in}}{R_1 C_1} \tag{20}$$

Using the transconductance value of OTA given in equation (2) and replacing the value of V_B in it using equation (19), the current equation (20) can be modified as

$$I_{in} = \frac{k}{\sqrt{2}}\left(\frac{\rho(t)}{R_1 R_2 C_1 C_2} - V_{SS} - 2V_{th}\right)\frac{\varphi_{in}}{R_1 C_1} \tag{21}$$

By rearranging the above equation, the obtained meminductance can be written as

$$L_M^{-1}(\varphi(t)) = -\frac{k}{\sqrt{2}R_1 C_1}(V_{SS} + 2V_{th}) + \frac{k\rho(t)}{\sqrt{2}R_1^2 R_2 C_1^2 C_2} \tag{22}$$

The above equation represents the flux-controlled memristor. The incremental/decremental mode of operation can be achieved by appropriate switching between N and P terminals of OTA. The proposed emulator circuit has been designed without using the multiplier. The AD633 multiplier IC supplies around $1/10^{th}$ of the product term that eventually results in a reduced loop area of the hysteresis curve. The transconductance term of the operational transconductance amplifier has been utilized to perform the multiplication operation. Using this method, the multiplication operation can be achieved without the need for the multiplier. Furthermore, the frequency behavior of the proposed Meminductor circuit design has been examined. Let us assume that the Meminductor circuit is stimulated with the voltage source so that the flux is stated as $\varphi(t)=V_M\sin(\omega t)$ where V_M and ω represent the amplitude and frequency of the signal. The equation (22) can be re-written as

$$L_M^{-1}(\varphi(t)) = -\frac{k}{\sqrt{2}R_1 C_1}(V_{SS} + 2V_{th}) + \frac{kV_M\cos(\omega t - \pi)}{\sqrt{2}R_1^2 R_2 C_1^2 C_2 \omega} \tag{23}$$

It can be observed that equation (23) consists of linear time-invariant and linear time-variant parts. The linear time-variant part is inversely proportional to the frequency, and therefore the linear time-invariant part dominates the time-variant part when the frequency increases. The magnitude of the time-varying meminductance term can be written as

$$\frac{kV_M}{\sqrt{2}R_1^2 R_2 C_1^2 C_2 \omega} = \frac{1}{\tau f} \tag{24}$$

where $\tau = 2\sqrt{2}\pi R_1^2 R_2 C_1^2 C_2/kV_M$ is the time constant of the proposed Meminductor emulator circuit, which in turn controls the area of the pinched hysteresis loop. The relationship of the time constant with input frequency is examined for the following cases:

1. It can be seen that the linear time-variant part of meminductance value disappears as the frequency tends to zero.
2. The area under the pinched hysteresis curve will be maximum at τ =1/f.
3. There may be losses in the pinched hysteresis characteristic if the time constant is less than the signal frequency.

Considering nonidealities and parasitic impedances present at the terminal of the analog building block in equation (7), the meminductance equation can be written as

$$L_M^{-1}(\varphi(t)) = \left(\frac{\alpha_1\alpha_2\beta_1\beta_2\rho(t)}{R_{eq1}R_{eq2}C_{eq1}C_{eq2}} - V_{SS} - 2V_{th}\right) \times \frac{k\alpha_1\beta_1\gamma_2}{\sqrt{2}R_{eq1}C_{eq1}} \tag{25}$$

where $R_{eq1}=R_1+R_X$, $R_{eq2}=R_2+R_{X2}$, $C_{eq1}=C_1+C_{Z1}+C_{Y2}+C_N$, $C_{eq2}=C_2+C_{Z2}+C_{VB}$. It can be observed from equation (25) that the value of meminductance is more affected at higher frequencies due to these errors and least affected at a lower frequency.

IV. MEM-ELEMENTS SIMULATION RESULTS AND DISCUSSION

In this section, the performance and functional correctness of the mem-elements emulator circuit have been simulated in the analog design environment of the Cadence tool using TSMC 180 nm process with the supply voltage of ±1.2 V to justify the theoretical explanations. The complementary MOS-based internal structure and aspect ratios of the fundamental analog building block such as CCII and OTA are discussed in [27]. The CMOS implementation of the element contains transistors in the saturation region of operation.

A. MEMRISTOR RESULTS AND DISCUSSION

The functional verification of the proposed design of floating/grounded memristor emulator of Figure 3 has been performed and simulated in the Analog Design Environment of Cadence Virtuoso using 180 nm TSMC standard CMOS process parameter with ±1.2 V as the nominal supply voltage. A sinusoidal signal of amplitude 800 mV at different frequencies has been applied across the Memristor to observe the frequency-dependent pinched hysteresis behavior. The value of passive components considered are R = 25 kΩ and C varies from 100 pF to 160 pF. The transient response of the proposed memristor emulator design has been shown in Figure. 6. The simulation has been performed at a different frequency as shown in Figure. 7. The lobe area under the hysteresis curve is inversely related to the frequency of the applied signal validating the theoretical analysis in equation (6). The inverse relation of the capacitor with the memductance has been shown in equation (6) and describes that the pinched hysteresis loop area decreases with an increase in the value of capacitance. The behavior of the presented emulator design at different temperatures has been analyzed at 1 kHz frequency as shown in Figure. 8. It can be observed that the hysteresis loop area of the Memristor has an inverse relation with the temperature level. It has been deduced that

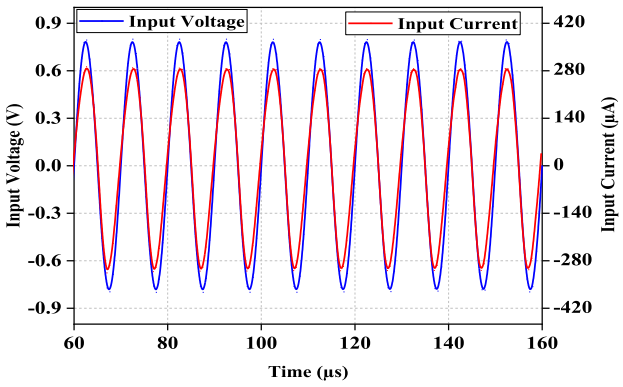

FIGURE 6. Transient response of the proposed memristor emulator.

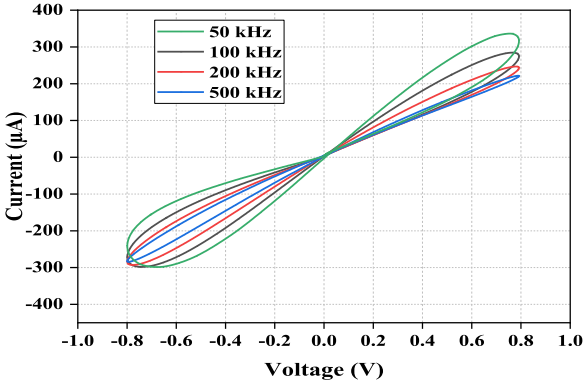

FIGURE 7. Frequency-dependent pinched hysteresis loop in a current-voltage plane at a different frequency.

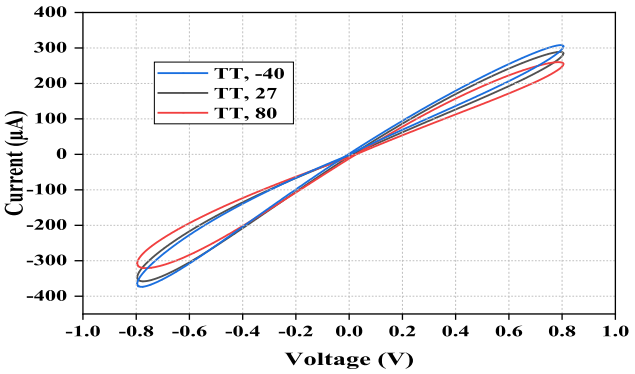

FIGURE 8. Frequency-dependent pinched hysteresis loop for different temperature.

the operating temperature is responsible for the change in leakage current and therefore proportional to absolute temperature (PTAT) biasing voltage source is used to reduce the effect of leakage current on the pinched hysteresis loop. In order to verify the robustness of the presented design, corner analysis has been carried out to check its consequences on the memristor design as shown in Figure. 9. The pinched hysteresis loop has been obtained for different SS, TT, and FF corner analyses at the same temperature. It can be observed that the hysteresis loop area is small showing less current flow in the case of process corner SS while in the case of process corner FF, a comparatively larger loop area has been observed as expected. The non-volatility is another characteristic of the memristor circuit apart from the frequency dependency of the pinched hysteresis loop. The non-volatility property states that the Memristor holds its last memductance value for a long time when no input signal is applied. The non-volatility behavior of the Memristor has been verified by applying a pulse train with an amplitude of 800 mV having a pulse width of 25 ms and a time period of 100 ms across the Memristor as shown in Figure. 10. The non-volatile nature of the memductance has been noted, and it is inferred that the variation is negligible over the entire non-pulse period.

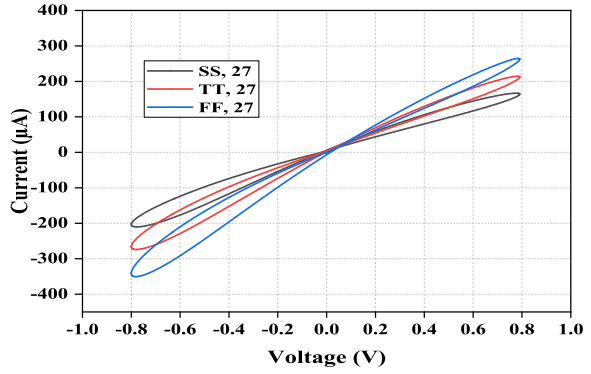

FIGURE 9. Pinched hysteresis loop at different process corners.

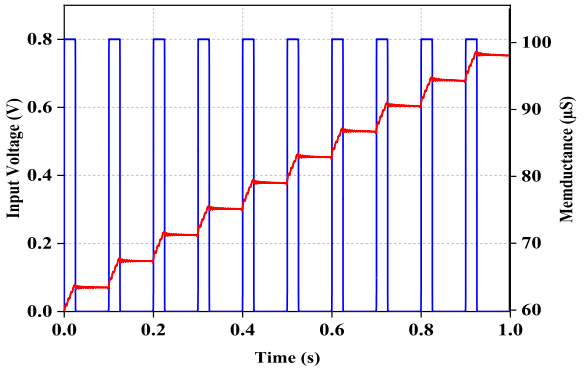

FIGURE 10. Memductance variation in incremental mode when a pulse train is applied across the emulator circuit.

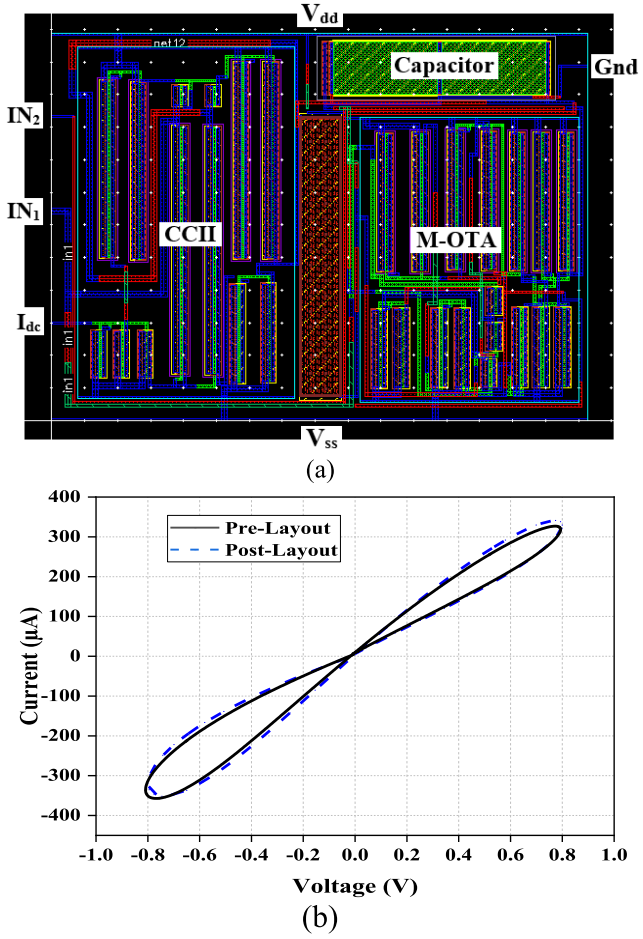

FIGURE 11. (a) Layout of memristor circuit (b) Pre and post-layout simulation results.

The value of the memductance has been preserved in the absence of the input signal showing the non-volatility property of the proposed design. The layout of the proposed memristor emulator design has been laid out, and post-layout simulations have been performed as shown in Figure. 11 to check the parasitic impact on the overall performance. It consumes an effective layout area of $4829\mu m^2$. It can be observed that there is a slight variation in the hysteresis loop of pre and post-layout results showing the presence of parasitic. The total power consumption is 9.843 mW.

B. MEMCAPACITOR

In order to verify the theoretical aspect of the presented memcapacitor emulator design in Figure 4, simulation has been carried out in Cadence design environment software using 0.18 μm TSMC process with the supply voltage of ± 1.2 V. The memristor input terminal is subjected to an AC sinusoidal input which yields a pinched hysteresis loop in the voltage-current plane. A similar loop is observed in the memcapacitor case across sinusoidal input voltage and the voltage across the capacitor. A sinusoidal signal of amplitude 800 mV at different frequencies has been applied across the memcapacitor emulator circuit to observe the frequency-dependent characteristic of the pinched hysteresis phenomena. The value of passive components considered $R_1 = 25$ kΩ, $R_2 = 1$ kΩ and capacitor varies from 30 pF to 300 pF. The capacitor voltage is taken across C_1. Figure. 12 shows the frequency-dependent characteristic of the pinched hysteresis curve of Memcapacitor at different frequencies. It can be observed that the area spanned by pinched hysteresis loop of proposed memcapacitor emulator design shows an inverse relation with the frequency validating the theoretical proposition. An increase in the frequency suppresses the linear time-varying part in comparison to the linear time-invariant part, thereby validating the equation (15). At very high frequency, the area under the C-V curve decreases, and the Memcapacitor now replicates its original behavior. In order to verify the robustness of the presented design, corner analysis has been studied and carried out in order to validate the effectiveness of the memcapacitor design as depicted in Figure. 13. The pinched hysteresis loop is thus obtained for different process corners such as SS, TT, SF, and FF at room temperature. It is seen that the hysteresis loop area is small, showing less current flow in the case of process corner SS while in the case of process corner FF, a comparatively larger loop area has been observed as expected. The behavior

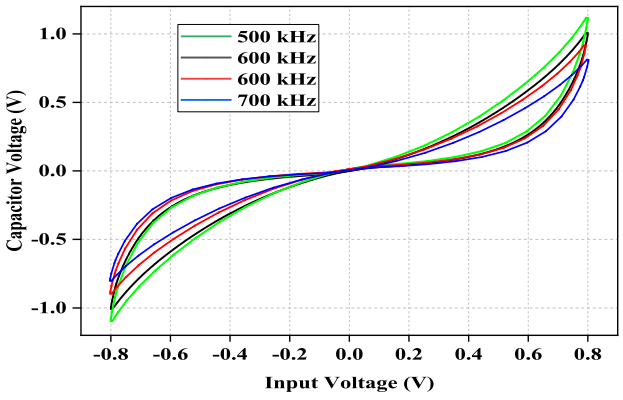

FIGURE 12. Pinched hysteresis loop at a different frequency 500 kHz, 600 kHz, 700 kHz, and 800 kHz.

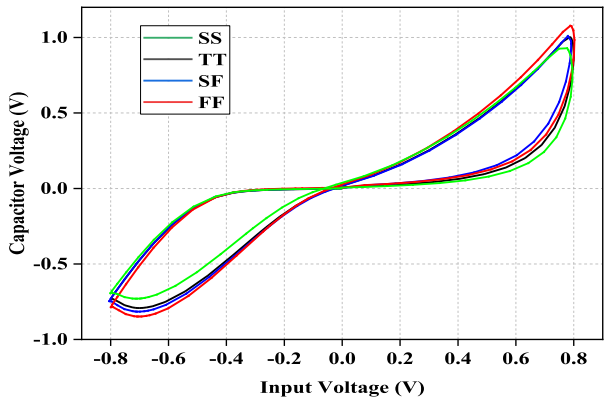

FIGURE 13. Pinched hysteresis loop obtained at different process corner SS, TT, SF, and FF.

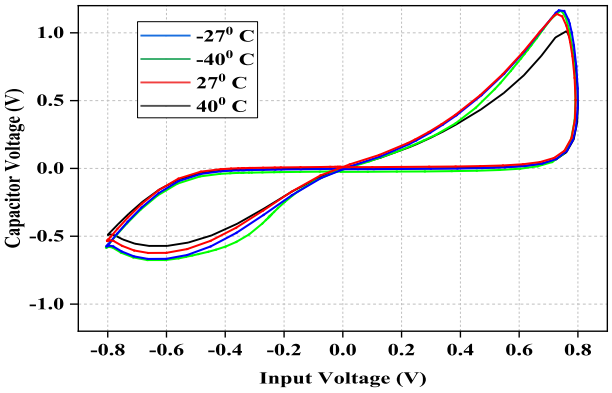

FIGURE 14. Frequency-dependent pinched hysteresis loop at different temperature.

of the presented memcapacitor emulator design at different temperatures has been analyzed at 500 kHz frequency as shown in Figure. 14. It can be observed that the emulator design is still operational within acceptable limits. The layout of the proposed memcapacitor emulator design has been laid out, and post-layout simulations have been done as shown in Figure. 15 to check the parasitic impact on the overall performance. It has a layout area of 8098 μm^2. The pre and post-layout outcomes show a slight variation in the hysteresis loop, which indicates the presence of parasitic as observed from the graph. The total power consumption is 14.741 mW.

C. MEMINDUCTOR

For the justification of theoretical explanations, the proposed design of the Meminductor emulator circuit shown in Figure. 5 has been simulated in ADE (Analog Design Environment) of Cadence Virtuoso design software using 180 nm TSMC standard CMOS process under the supply voltage of ±1.2 V. A sinusoidal signal of amplitude 800 mV at different frequency has been applied across the Meminductor circuit to observe the frequency-dependent pinched hysteresis behavior. The value of passive components considered

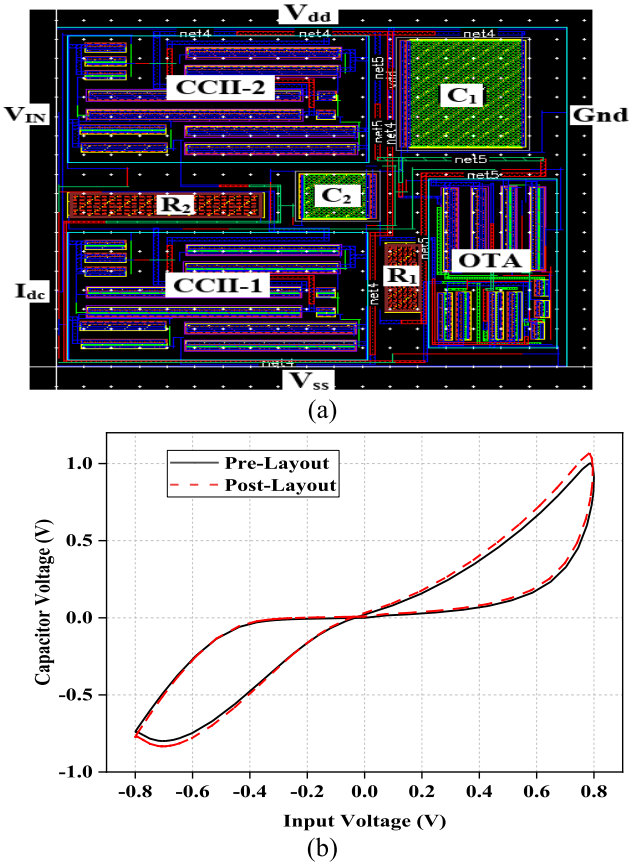

FIGURE 15. (a) The layout of memcapacitor emulator circuit (b) Pre and post-layout simulation results.

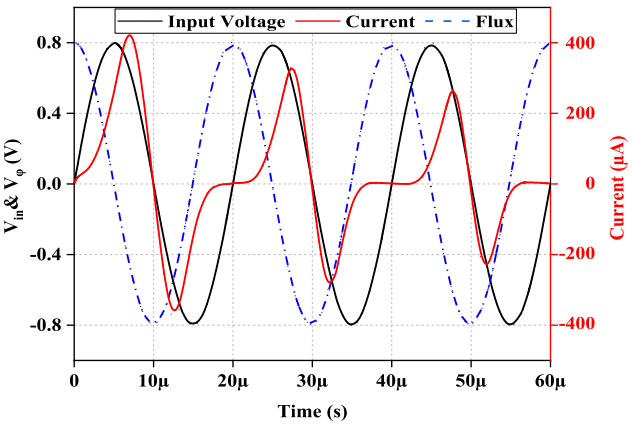

FIGURE 16. Transient response of Meminductor at 50 kHz.

$R_1 = 15$ kΩ, $R_2 = 75$ kΩ and capacitor varies from 30 pF to 300 pF.

The transient analysis of the proposed meminductor design has been carried out as shown in Figure. 16 with the sinusoidal input of amplitude 800 mV at 50 kHz frequency. It can be observed that there is a 90 degree phase shift in the obtained flux waveform with respect to the applied input voltage waveform. The transient response has been performed

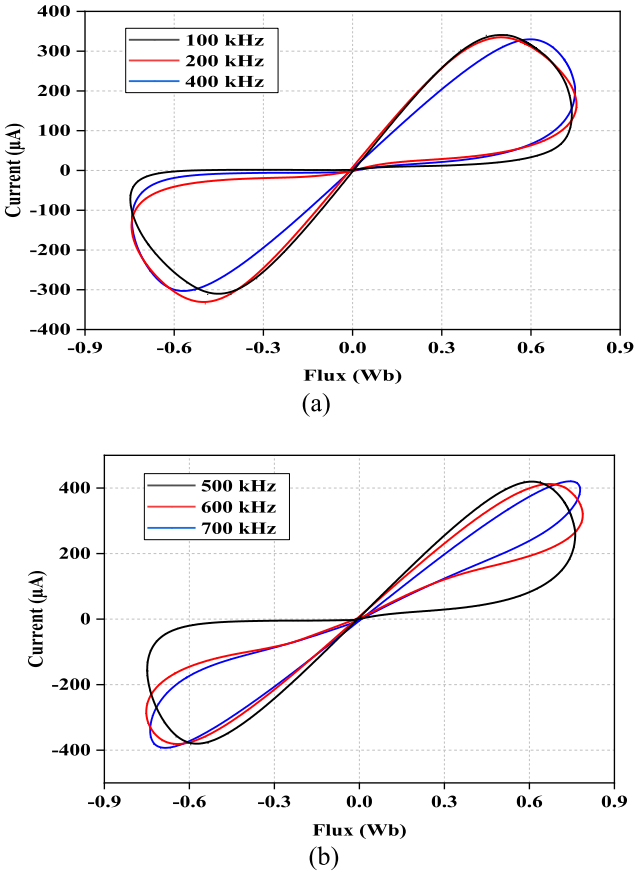

FIGURE 17. Frequency-dependent pinched hysteresis loop at a different frequency (a) 100 kHz, 200 kHz, 400 kHz (b) 500 kHz, 600 kHz, 700 kHz.

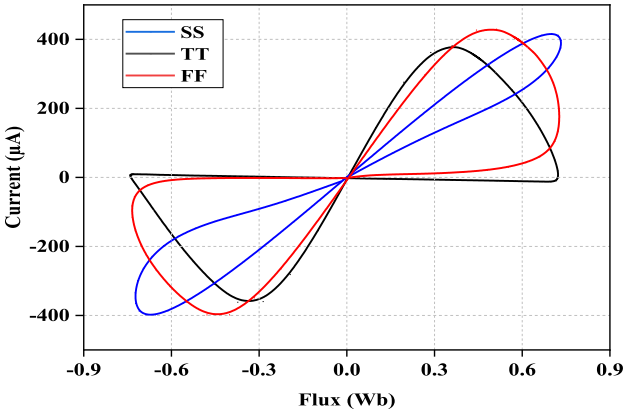

FIGURE 18. Frequency-dependent hysteresis loop variation at different process corners at room temperature.

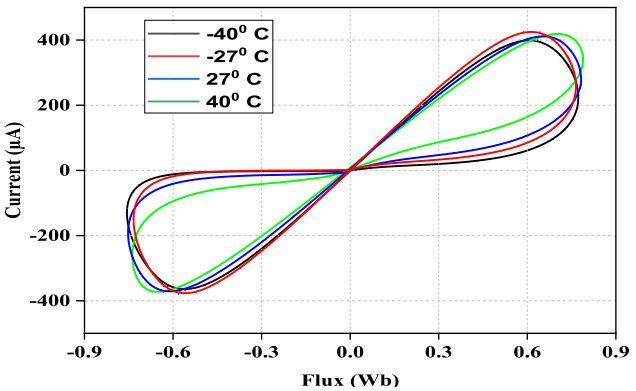

FIGURE 19. Frequency-dependent pinched hysteresis loop variation at various temperatures.

for three cycles of the input signal. To ensure the ease of plot between the flux and current, the voltage V_φ is taken as flux and current as I_{in}. It is verified from Figure. 16 that the voltage leads the flux and current similar to what is seen in the traditional inductor but the current does not show a sinusoidal behavior as the inductance changes with respect to time.

The simulation has been performed at a different frequency as shown in Figure. 17 and the corresponding pinched hysteresis loop has been observed. It can be noted that with increasing frequency, the area of the pinched hysteresis loop shrinks and gets narrower. The presented circuit design has been simulated for different process corner analyses at room temperature to examine the robustness of the Meminductor emulator design. Process variation is a crucial feature to be considered when a design is to be monolithically integrated. The corner analysis for the transistors is slow N, slow P abbreviated as SS, slow N, fast P (SF), and fast N, fast P (FF). The process variation performance has been shown in Figure. 18. It can be observed that the loop area of the pinched hysteresis in the case of FF mode is more than SS mode, indicating a higher flow of current in FF as expected. The proposed Meminductor design shows hysteresis loop behavior pinched at the origin in all process corners despite area variation. The parameters like threshold voltage, mobility of charge carriers, saturation velocity, and hence the drain current are greatly hindered by the temperature variations in IC's. It is of utmost importance to gain an insight into the temperature effect on the responses of the presented mem-inductor as the proposed mem-inductor emulator is composed of CMOS CCII and OTA. Figure. 19 shows the hysteresis curve pinched at the origin at different values of temperature. This also depicts the negligible temperature effect of the mem-inductor presented. Non-volatility is another essential feature of mem elements. Henceforth, it is crucial to analyze its non-volatile nature. Further analysis has been done with 800 mV signal amplitude having pulse width 25 ns and interval of 100 ns. Figure. 20 presents the variation in meminductance with respect to time with an applied input signal. It is clearly seen that the meminductance which is nothing but the ratio of current and flux varies significantly during the ON time of the input pulse signal and is fairly constant over the entire OFF time of the input pulse signal. This concept is a clear justification of the non-volatile nature of the proposed Meminductor circuit design. Since the proposed Meminductor circuit is composed of passive components as well as transistors, a deviation in the meminductor characteristics is observed owing to the change in values of the passive components, temperature, and process

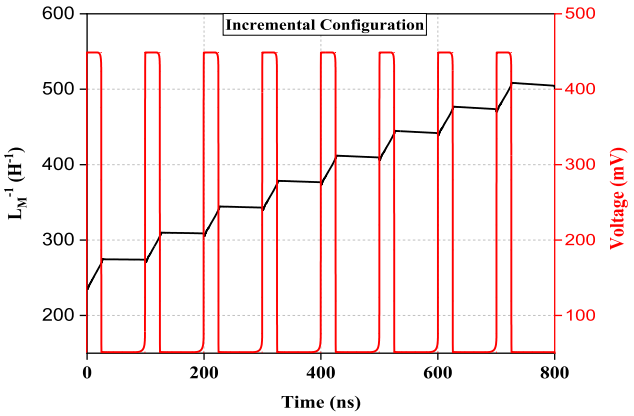

FIGURE 20. Non-volatility nature of proposed Meminductor.

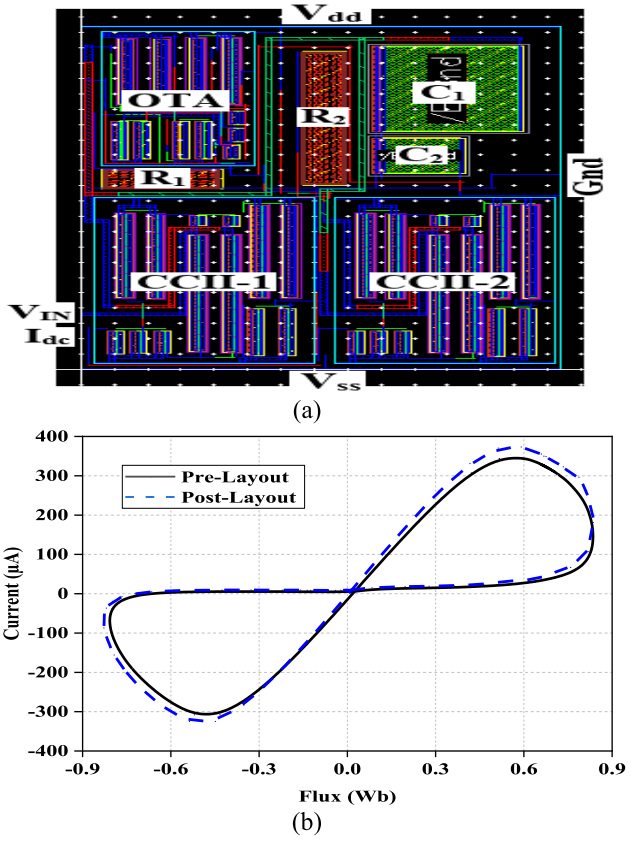

FIGURE 21. (a) Layout of Meminductor emulator circuit (b) Pre and post-layout simulation results.

parameter variations. The layout of the proposed meminductor emulator circuit design has been laid out, and post-layout simulations have been performed as shown in Figure. 21 to check the parasitic impact on the overall performance. The layout consumes an effective area of 8061 μm^2. It can be observed that there is a slight variation in the hysteresis loop of pre and post-layout results showing the presence of parasitic The total power consumption of meminductor design is 14.359 mW.

V. EXPERIMENTAL TESTS OF MEM-ELEMENTS MODEL

In order to validate the correctness and performance of the proposed mem-elements emulator circuits, experimental verification has been done where the mem-elements are well examined through a breadboard implementation of commercially existing integrated circuits namely CA3080 and AD844AN. The DC power supply voltage for the proper operation of the mem-elements circuits is ±15 V. The transconductance parameter (g_m) of the OTA can be kept under control by the bias current. The input bias current is provided through a passive resistor connected between a constant voltage (direct current source) and the input terminal of the CA3080 integrated circuit. The variation here is responsible for controlling the transconductance value. The proposed Memristor emulator circuit design is viable for both CMOS realization as well as breadboard implementation using discrete circuit elements. AC signal is applied at the input terminals of the mem-element circuit as a result of which frequency-dependent pinched hysteresis curve is obtained. The nominal values for the supply voltages and resistor are ±15V, 40 kΩ respectively, while the capacitor values are adjusted in accordance with the operating frequency values. The pinched hysteresis loop at different frequencies has been obtained in the digital storage oscilloscope using Keysight - DSOX2022A. The experimental validation of the memristor emulator circuit design shown in Figure. 3 has been performed at frequency 600 kHz as shown in Figure. 22. It is further observed that the hysteresis loop somewhat gets deformed owing to the deviation from the setpoint value, existing parasitic, transistor mismatch that results in an asymmetrical behavior. On increasing the values to a certain extent, the hysteresis loop suffers from distortion due to the frequency limitation imparted by the IC's. As the frequency is increased further, the hysteresis loop gets narrower and narrower.

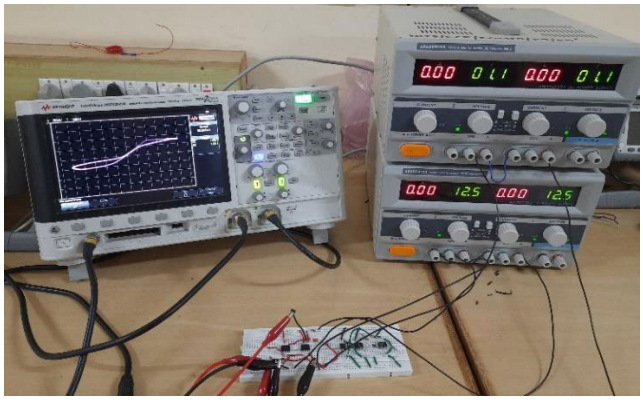

FIGURE 22. Experimental results of memristor circuit obtained at the frequency 600 kHz.

Figure. 23 depicts the experimental pinched hysteresis loop of the proposed memcapacitor emulator circuit obtained at frequency 400 kHz. It can be noted that the input voltage is plotted against the capacitor voltage, which ultimately

FIGURE 23. Pinched hysteresis loop of memcapacitor circuit obtained at a different frequency 400 kHz.

FIGURE 24. Pinched hysteresis loop of meminductor circuit obtained at the frequency 400 kHz.

reflects the charge across the capacitor. Figure. 24 shows the hysteresis loop obtained experimentally at frequency 400 kHz for the proposed Meminductor emulator circuit design. In order to obtain the frequency-dependent loop of presented Meminductor circuit elements, the input signal is provided with a 90° phase shift to easily obtain the flux (V_φ) and time integral of flux (V_ρ). Since these commercial ICs have frequency limitation and therefore the experimental setup is bound with a frequency around 2 MHz. Several offset elimination method or biasing technique of transistors minimizes the deviation observed in the desired output. The parasitic effect due to interconnection is also responsible for the frequency limitation of the experimental setup. It can be observed from the obtained waveform that the loop area of the hysteresis curve depends on the operational frequency and at very high frequency, it behaves linearly validating the theoretical analysis and simulation results of the mem-elements.

VI. COMPARISON

The performance of the proposed mem-element emulator circuit design has been compared with the available emulator circuit in literature as shown in Table 2 in terms of technology used, power supply, number of active/passive elements, and topology. It can be observed from Table 2 that the presented mem-element has been implemented using CCII and OTA with few passive elements. However, the proposed emulator circuit design has been validated by both CMOS and BJT technology. It can be observed from Table 2 that the presented design works in both incremental and decremental configurations. The active elements required for Memcapacitor and Meminductor circuit implementation are less compared to another existing circuit in literature. The advantage of the proposed mem-element design is that the used active element is available in the form of commercially available ICs AD844 and CA3080. The layout of the presented design requires a total chip area of 4829 μm^2, 8098 μm^2, and 8061 μm^2 respectively for Memristor, Memcapacitor, and meminductor circuits. The total power consumed by the presented emulator circuit is 9.843 mW, 14.741 mW, and 14.359 mW respectively for Memristor, Memcapacitor, and meminductor emulator circuit design.

VII. APPLICATIONS

Finally, the feasibility of the proposed mem-elements circuit design has been demonstrated as chaotic and hyperchaotic oscillations. From a practical viewpoint, the Memristor circuit can be applied in various signal processing applications, waveform generation, and shaping circuits. Some specific instruments that find an inherent use of such waveforms are sampling oscilloscope and transistor curve tracer. Memristive circuits can be further used for both signal detection and switching applications. The increasing attention on the Memristor circuit due to its various dynamical characteristics such as non-volatility, non-linearity, etc makes it the most preferred and common choice as a fundamental building block for the chaotic circuit. Chua's circuit can be transformed into a simple mem-element-based circuit through the replacement of the non-linear component with Memristor / Meminductor / Memcapacitor. The simplest electronic circuit used to model the chaos theory study is the famous Chua's circuit. The onset of chaotic, hyperchaotic, attractors and bifurcation behavior on numerous scenarios has been manifested by Chua's circuit thereby making it very useful in dynamically rich non-linear systems. Figure. 25 shows the circuit diagram for generating Chua's non-periodic oscillations. The circuit implementation comprises a linear resistor, a linear inductor, capacitor C_1, and C_2 along with a non-linear mem-element. The dynamics of

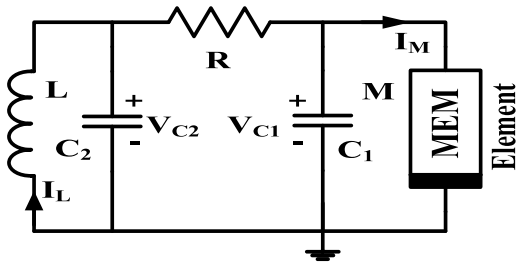

FIGURE 25. Mem-elements based chaotic circuit.

TABLE 2. Comparison of the proposed mem-elements emulator circuit with existing building block based mem-element in literature.

Ref.	*Type of Mem-Element*	*No. of active components*	*No. of passive components*	*Sim. / Exp.*	*Technology used*	*Incremental/ Decremental*	*Power supply Mode*
[9]	Memristor	1 CBTA, 1 MUL	R=2 C=1	Sim	CMOS	Both	±0.9 V
[10]	Memristor	1 OTA	C=1	Sim	CMOS	Decremental	±0.9 V
[11]	Memristor	1 CCII, 1 CCTA	R=3 C=1	Both	CMOS	Both	±1.5 V
[12]	Memristor	2 CFOAs, 1 OTA	R=3 C=2	Both	BJT	Incremental	±12 V
[13]	Memristor	2 AD844s, 1 MUL	R=2 C=1	Both	BJT	Both	±10 V
[14]	Memristor (Grounded)	1 CCII, 1 OTA	R=1 C=1	Both	CMOS	Both	±1.2 V
Work-1	**Memristor (Floating/Grounded)**	**1 CCII, 1 M-OTA**	**R=1 C=1**	**Both**	**CMOS**	**Both**	**±1.2 V**
[15]	Memcapacitor	1 DXCCDITA	R=1 C=2	Sim	CMOS	Both	±1.25 V
[16]	Memcapacitor	4 CCIIs, 1 Op-amp	R=6 C=2	both	BJT	Incremental	±3 V
[17]	Memcapacitor	3 CCIIs, 3 TOAs, 1 MR	R=3 C=1	Sim	BJT	Incremental	±15 V
[18]	Memcapacitor	2 CCIIs, 1 MUL	R=1 C=3	Both	CMOS	Both	±10 V
[19]	Memcapacitor	2 CCIIs 1 MR	R=1 C=1	NA	BJT	NA	NA
[20]	Memcapacitor	1 CCII, 1 OTA, 1 MUL	C=3	Both	BJT	Both	±20 V
[21]	Memcapacitor	2 MO-OTA, 1 MUL	R=2 C=2	Sim	CMOS	Incremental	±1.25 V
Work-2	**Memcapacitor**	**2 CCII, 1 OTA**	**R=2 C=2**	**Both**	**CMOS**	**Both**	**±1.2 V**
[19]	Meminductor	2 DOCCII, 1 MR	R=1 C=1	NA	BJT	NA	NA
[22]	Meminductor	4 AD844s, 2 Op-amp, 1 AD633	R=7 C=2	Both	BJT	NA	±15 V
[24]	Meminductor	1 AD633, 3 Op-amp, 12 NMOS	R=2 C=2 L=1	Sim	BJT	Incremental	±5 V
[25]	Meminductor	1 Op-amp, 1 MR	R=1 C=1	Sim	BJT	NA	NA
[26]	Meminductor	2 MO-OTA, 1 MUL	R=2 C=2	Both	CMOS	Incremental	±1.25 V
Work-3	**Meminductor**	**2 CCII, 1 OTA**	**R=2 C=2**	**Both**	**CMOS**	**Both**	**±1.2 V**

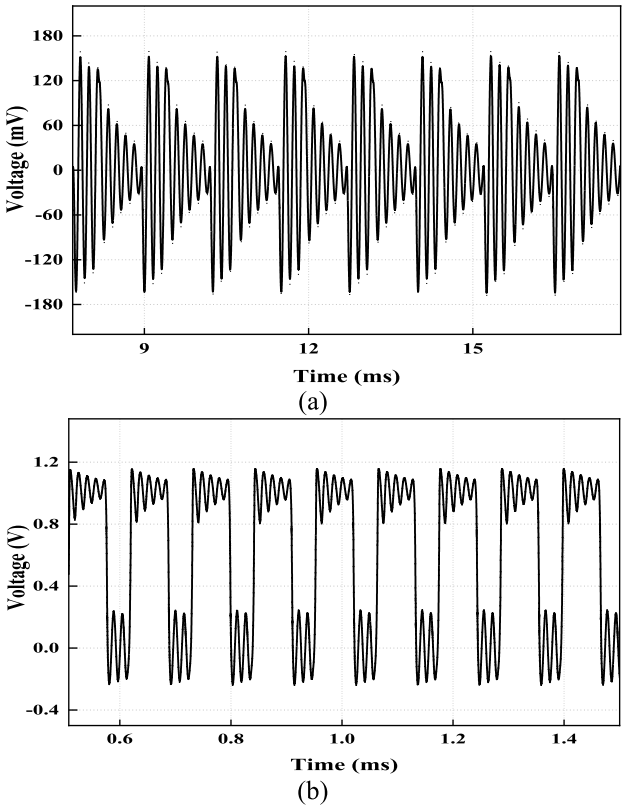

FIGURE 26. The response of mem-elements based Chua's oscillator (a) Chaotic output obtained at V_{C1} (b) Chaotic output obtained at V_{C2}.

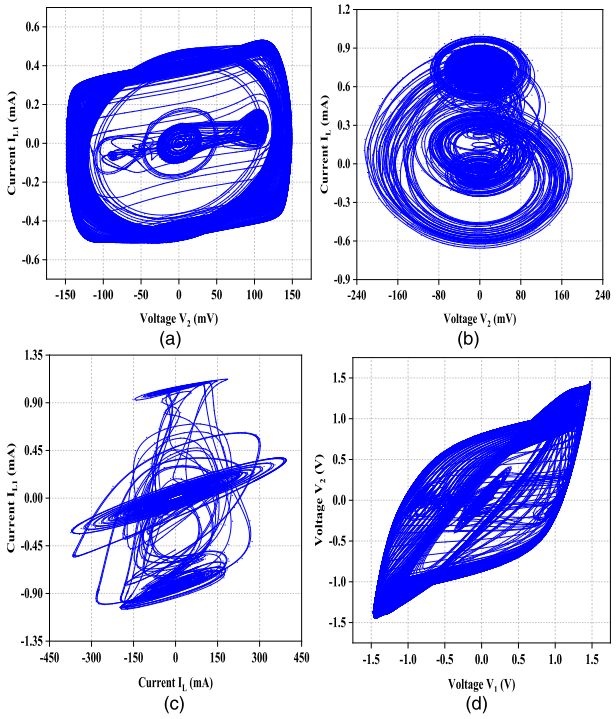

FIGURE 27. Chaotic attractor of the 5D system. Response for values of (a) $C_2 = 68$ nF and $L_1 = 112$ mH, (b) $C_2 = 76$ nF and L = 8.5 mH, (c) $C_1 = 7.2$ nF and $C_2 = 74$ nF, (d) L = 7 mH and $L_1 = 98$ mH.

the circuit is governed by the following set of equations:

$$\begin{aligned} \frac{d\varphi}{dt} &= V_{C1} \\ \frac{dV_{C1}}{dt} &= \frac{1}{C_1}\left[\frac{V_{C2}-V_{C1}}{R} - I_M\right] \\ \frac{dV_{C2}}{dt} &= \frac{1}{C_2}\left[\frac{V_{C1}-V_{C2}}{R} - I_L\right] \\ \frac{dI_L}{dt} &= \frac{V_{C2}}{L} \end{aligned} \tag{26}$$

The values of the linear elements i.e R, L, C_1, and C_2 are 1.735 kΩ, 5.9 mH, 4.8 nF, and 72 nF respectively. V_{C1} and V_{C2} signify the chaotic non-periodic oscillation voltages as shown in Figure. 26. The chaotic system in general offers a predictable system behavior for a short while but later on depicts a seemingly random course of events. The non-linear irregularities existing between the region of periodicity and randomness are defined as Chaos. Nevertheless, some chaotic systems tend to appear regularly and in order whereas some may appear apparently random in nature. After a short while, the system predominantly becomes unpredictable that can be governed by deterministic laws. Mem-elements are regarded as one of the most favorable candidates for designing novel chaotic as well as hyper-chaotic systems. Unlike that of the lower dimensional chaotic circuits/systems, the higher dimensional system attractors possess somewhat difficult identifiable structures. It is for this reason that the hyper-chaotic system, which is a higher-dimensional entity becomes highly applicable in secure communications [7]. However, it is observed that the introduction of a mem-element makes the dynamic behavior even more complex and entirely different from the prevailing hyper-chaotic system. The obtained attractors have been shown in Figure 27. Mem-elements emulator circuit can be used to investigate the dynamics of the chaotic and hyperchaotic system.

The realization of the chaotic circuit using mem-elements circuits has a crucial role to play when applied to diverse chaos-based system applications like image encryption schemes. A path planning generator is another chaos-based application that is used in autonomous mobile robots or random bit generators.

VIII. CONCLUSION

This work proposes a mem-elements emulator circuit built-in around ready-to-use electronics components that can be made incremental or decremental simply by adjusting the input connections of the OTA. The theoretical study is further verified through software simulation as well as experimental trial and testing. The impact of parasitic behavior and output variations from the set point on the functionality of the proposed Memristor emulator circuit has been evaluated. Furthermore, to ensure the robustness of the design, corner analysis has been carried out. A commercially available integrated circuit model of the design using AD844AN and

CA3080 was made on a breadboard to demonstrate the correct functionality and practicability of the circuit. One of the most fingerprint characteristics i.e the non-volatility of the mem-element has also been assessed and tested which in turn confirms the theoretical studies conducted. The mem-elements circuit has been laid out using 180 nm TSMC CMOS process parameters of the Cadence Virtuoso software spanning over limited layout dimensions with the chip are of 4829 μm^2, 8098 μm^2, and 8061 μm^2 respectively for Memristor, Memcapacitor, and meminductor design. The maximum power consumption of the proposed mem-elements emulator design is around 9.843 mW, 14.741 mW, and 14.359 mW respectively for the Memristor, Memcapacitor, and meminductor circuit. Chaotic systems have been designed to show the potential applications of the proposed mem-element emulator circuit.

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