Extremely low-voltage low-power differential difference current conveyor using multiple-input bulk-driven technique

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Abstract

In this paper, a new differential difference current conveyor (DDCC) with ultra-low voltage and low-power capability is presented. The DDCC is designed by using a non-tailed differential pair with multiple-input bulk-driven MOS transistor technique to obtain a rail-to-rail input common-mode swing and extremely low supply voltage. The MOS transistors biased in the sub-threshold region have been used to achieve extremely low power consumption. The performance of the proposed DDCC is evaluated by simulation results using SPICE program and MOS transistors parameters provided by a standard n-well 0.18 µm CMOS process from TSMC. A rail-to-rail input common-mode range was shown and a high accuracy was expressed. The bandwidth was 2.2 kHz and the total harmonic distortion was 1 % for an input signal with amplitude of 240 mV_{p-p}, obtained at supply voltage of 0.3 V and power dissipation of 28.6 nW. The proposed DDCC has been used to realize a sixth-order low-pass filter for application to electrocardiogram (ECG) applications.

Keywords:

Differential difference current conveyor; subthreshold technique; bulk-driven technique; multiple-input bulk-driven technique; low voltage and low power; high-order filter; analog circuit

1. Introduction

The second generation current conveyor (CCII) is a basic building block which can find many applications in analog signal processing applications such as continuous-time filters, signal generators, nonlinear circuits, electrical elements (resistance, inductance, memristance) simulators/emulators circuits and data converters [1]-[7]. In comparison to operational amplifier (op-amp)-based circuits, CCII-based circuits offer several advantages: simple circuit structure, alleviating the need for both floating passive components and matched resistors, wide frequency bandwidth, versatile and high accuracy in realizing the intended characteristics, large dynamic range and low supply voltage requirement [8]. A number of CCIIs is available in open literature [9]-[19]. The early structure of CCII is a conventional CCII which offers three terminals, namely y-, x- and z-terminals [9]. The unity voltage gain can be obtained between y- and x-terminals while the unity current gain can be obtained between x- and z-terminals. However, a single CCII may be limited for some applications: obtaining differential voltage or current input signals requirements, positive and negative for feedback connections and alleviating the need for floating resistors, etc. Therefore, there are several structures of CCIIs which have been developed to increase the performance of conventional CCII: differential difference current conveyor (DDCC) [10], differential voltage current conveyor (DVCC) [11], dual X second generation current conveyor (DX-CCII) [12], extra X second generation current conveyor (EX-CCII) [13], differential second generation current conveyor (DCCII) [14], fully differential second-generation current conveyor (FDCCII) [15]. These structures improved the performance of conventional CCII, which has one y-terminal, one x-terminal and one z-terminal, by adding y-terminal and/or x-terminal to obtain adding/subtracting voltage and current differencing capability. This work focuses on the DDCC which provides the advantages of conventional CCII and arithmetic operation capability of differential difference amplifier (DDA) [16] into single device. Thus, the conventional DDCC has three y-terminals, one x-terminal and one z-terminal, where adding and subtracting voltage can be obtained through two plus-type y-terminals and one minus-type y-terminal. The DDCC with both plus-type and minus-type y-terminals is convenient for realizing positive and negative feedback applications such as negative feedback for filters and positive feedback for oscillators. There are DDCC based analogue circuits that have been reported in literature in recent years, for example, see [17]–[21]. Unfortunately, these circuits do not provide ultra-low voltage and ultra-low power operation.

At present, the analogue circuits operating with ultra-low supply voltage and ultra-low power consumption are of grown interest, due to the fact that these circuits can be applied in

portable electronics and biomedical devices [22]. The analogue signal processing circuits such as continuous-time filters [23]–[25], amplifiers [26]-[27], precision rectifiers [28]–[29], are usually required for applications. There are many active devices operating with ultra-low supply voltage and ultra-low power consumption available in open literature such as operational transconductance amplifiers (OTAs) [30]–[32], current conveyors [33]–[34], DDA [35] etc.

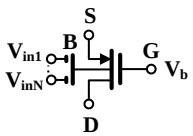
Focusing on DDCC operated with ultra-low supply voltage and ultra-low power consumption, this device has been already introduced using different MOS techniques [36]–[41]. Several DDCCs based on bulk-driven (BD) MOS technique [36], [37], quasi-floating gate (QFG) [36], BD QFG MOS technique [36], [38], multiple-input bulk-driven (MIBD) QFG MOS technique [39], [40], multiple-input bulk-driven (MIBD) [40], have been proposed. If consider the supply voltage and power consumption, the circuits in [36], [37] use 0.6 V (±0.3) of supply voltage and consume about 18.5 µW of power, the circuit in [38] uses a 1 V of supply voltage and consumes 37 µW of power, the circuit in [39] uses a 0.5 V of supply voltage and consumes 1.7 µW and the circuits in [40] uses a 0.4 V of supply voltage and consumes 0.14 µW of power. It should be noted in [36]–[40] that the supply voltage and power consumption, respectively, of DDCCs are scaled down from 1 V to 0.4 V and 37 µW to 0.14 µW. Until now, DDCC operating with 0.3 V supply voltage and consuming 38 nW of power is introduced [41]. The input stage of DDCCs in [36]–[40] is realized based on differential structure which needs a tail current. A tail current is usually implemented by a MOS transistor, which increases the minimum supply voltage by at least $V_{DS(sat)}$. Thus, the lowest supply voltage of these DDCCs [36]–[40] is around 0.4 V [40]. Unlike the DDCCs in [36]–[40], the DDCC in [41] is based on a non-tailed differential amplifier, and is able to operate from supply voltage as low as 0.3 V, which cannot be achieved for a DDCC with a tail current differential amplifier. The circuit in [41] can operate with extremely low supply voltage, but shows relatively poor accuracy of the voltage/current gains, which is the result of its simple structure and low open-loop voltage gain of the y-x amplifier. This also results in relatively low value of the resistance R_x, seen from its x terminal.

In order to overcome the above issues, a high performance DDCC which can operate with ultra-low supply voltage and ultra-low power consumption has been proposed in this paper. The proposed DDCC can operate from supply voltage as low as 0.3-V, which is possible thanks to the use of non-tailed differential pair in its input stage. The multiple-input bulk-driven technique is also used to reduce a number of MOS differential pairs. The DDCC shows ultra-low supply voltage and ultra-low power consumption using three techniques,

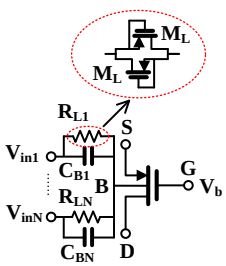
namely, subthreshold biasing, dynamic threshold MOS and bulk-driven MOS techniques. The bulk-driven technique is used in the input stage and thanks to this a rail-to-rail input common-mode range can be obtained. The performance of the proposed DDCC was evaluated by simulation, using SPICE and transistors parameters for a standard n-well 0.18 μm CMOS process from TSMC. Simulations showed the bandwidth of 2.2 kHz and the total harmonic distortion of 1 % for an input signal with amplitude of 240 mV_{p-p}, obtained at supply voltage of 0.3 V and power dissipation of 28.6 nW. The proposed DDCC has been used to realize a sixth-order low-pass filter for electrocardiogram (ECG) applications.

2. Proposed ultra-low voltage MIBD DDCC

In this work the multiple-input bulk-driven (MIBD) MOS transistor (MOST) technique, [40] was applied. The symbol and implementation of the MIBD MOS are shown in Figs. 1(a) and Fig. 1(b) respectively. The MIBD MOST is a multiple-input device which is realized using parallel connections of capacitors C_{Bi} and resistors R_{Li}, where i = 1, 2, …, N, while its gate terminal is properly biased with DC voltage V_b. Assuming that an n-well CMOS process was applied in the design , only the p-channel MOS transistors can be controlled in such a way. The resistor R_L should possess high resistance value which can be implemented using two transistors M_L operating in cut-off region as shown in Fig. 1(b). The small-signal model of the MIBD MOST that has been used for AC small-signal analysis is shown in Fig. 1(c). The g_{mb} is the bulk transconductance, r_o is the output resistance, the capacitances C_{BS}, C_{BD}, C_{BSUB} are respectively the parasitic capacitances bulk-source, bulk-drain and bulk-substrate. The capacitance C_{Mi} is the parasitic capacitance between gate and drain of the transistor M_{Li}, the resistance R_{Mi} is the output resistance of the transistor M_{Li} while the capacitance C_{Bi} is the input capacitance.



(a)



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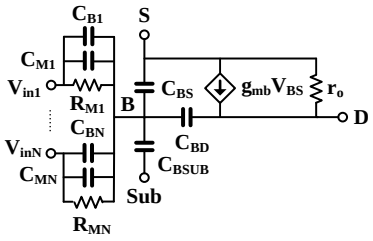

(c)

Fig. 1. MIBD PMOST [40]: (a) symbol of MIBD, (b) MIBD implementation, (c) small-signal model.

From Fig. 1(c), assuming $1/\omega C_{Bi} << R_{Li}$, $C_{Mi} << C_{Bi}$ the input transconductances (g_{mi}) of MIBD MOST can be given [40] by

$$\boldsymbol{g_{mi} = \frac{C_{Bi}}{C_{TOT}} g_{mb}} \tag{1}$$

where $\boldsymbol{C_{TOT}}$ is the total capacitance looking into input port which can be given by

$$\boldsymbol{C_{TOT} = C_{BS} + C_{BD} + C_{BSUB} + \sum_{i=1}^{N} C_{Mi} + \sum_{i=1}^{N} C_{Bi}} \tag{2}$$

The voltage at bulk terminal $\boldsymbol{V_B}$ can be given by

$$\boldsymbol{V_B \approx \sum_{i=1}^{N} \frac{C_{Bi}}{C_{TOT}} V_{in,i}} \tag{3}$$

The relation between the inputs-referred noise powers of the MIBD MOST $\boldsymbol{\overline{v_{n,i}^2}}$ compared to the BD MOST $\boldsymbol{\overline{v_{n,B}^2}}$ can be expressed by

$$\boldsymbol{\overline{v_{n,i}^2} = \left(\frac{C_{TOT}}{C_{B,i}}\right)^2 \overline{v_{n,B}^2}} \tag{4}$$

where $\boldsymbol{C_{TOT}}$ is the total capacitance looking into the input port. It can be concluded from (4) that the input-referred noise of the MIBD MOST is increased by $\boldsymbol{C_{TOT}/C_{B,i}}$, but the maximum input signal range is also increased with the same ratio, hence the dynamic range (DR) is not affected by this ratio.

Fig. 2 shows the circuit symbol of DDCC and its port relations can be expressed by

$$\begin{pmatrix} I_{y1} \\ I_{y2} \\ I_{y3} \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \\ 0 & 0 & 0 & \alpha & 0 \end{pmatrix} \begin{pmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \\ V_z \end{pmatrix} \tag{5}$$

where $\beta_1 = 1 - \varepsilon_{1v}$, $\beta_2 = 1 - \varepsilon_{2v}$, $\beta_3 = 1 - \varepsilon_{3v}$ represent the voltage gain between x-terminal and y_1-, y_2-, y_3-terminals, respectively, $\alpha = 1 - \varepsilon_i$ represents the current gain

between z-terminal and x-terminal, whereas ε_{1v}, ε_{2v}, ε_{3v} ($|\varepsilon_{1v}|$, $|\varepsilon_{2v}|$, $|\varepsilon_{3v}| \ll 1$ and $|\varepsilon_i| \ll 1$) represent respectively voltage and current tracking errors. For ideal case, $\beta_1 = \beta_2 = \beta_3 = \alpha = 1$.

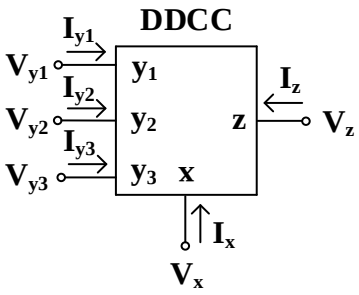

Fig. 2. Electrical symbol of DDCC.

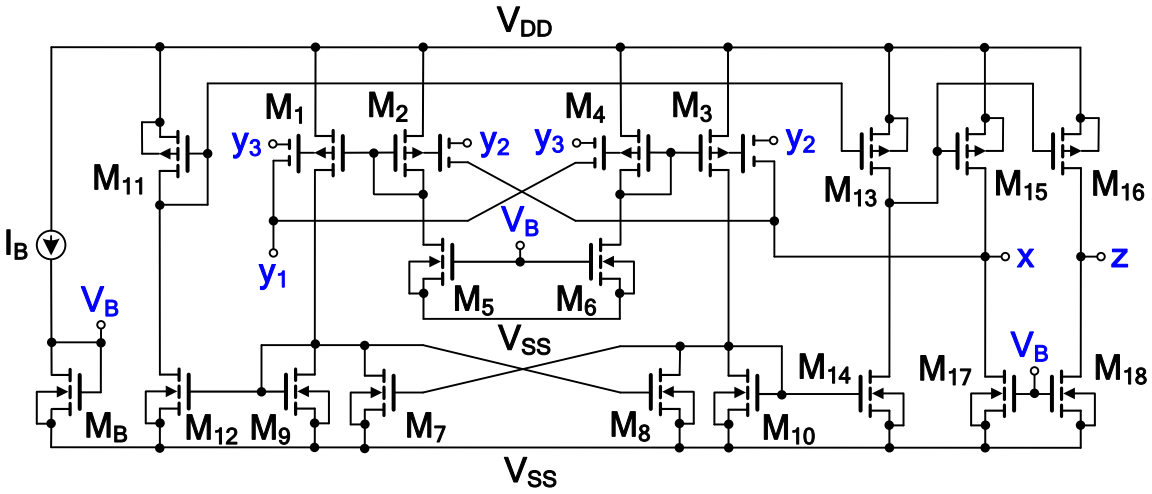

Fig. 3. Proposed 0.3 V MIBD DDCC.

The proposed internal structure of the DDCC is shown in Fig. 3. The transistors, M_1-M_6, of the circuit form a non-tailed bulk-driven differential amplifier [42] which is realized using the MIBD MOST technique to obtain multiple-input differential amplifier and to reduce a number of MOS transistor pairs. This non-tailed architecture provides a good CMRR [32], [35], [42], which can improve the accuracy of DDCC when it is connected in a negative feedback unity-gain configuration. The non-tailed differential amplifier provides an ultra-low supply voltage of the circuit because the voltage across tail current source is absent [35]. The cross-coupled transistors M_7 and M_8 are added to form a positive feedback and provide some increment for the DC gain and gain bandwidth product (GBW) performance of differential amplifier. These transistors will generate negative conductance, i.e. $-g_{m7}$ and $-g_{m8}$, for decreasing the total conductance at the drain terminals of M_9 and M_{10}. The diode-connected

transistors M_9 and M_{10} are used for the load of differential amplifier which decreasing the total conductance by $-g_{m7}$ and $-g_{m8}$ and consequently to improving the DC gain and GBW of differential amplifier [35].

The transistors M_{11}-M_{14} are used to mirror the output currents of differential amplifier and converted current signals into a single voltage at the drain terminals of M_{13} and M_{14}. The output stage consists of transistors M_{15}-M_{18} when transistors M_{15} and M_{16} work as output amplifier operating in class-AB, loaded with the current source using transistors M_{17} and M_{18}. The high current driving capability can be obtained by increasing the quiescent drain currents of M_{17} and M_{18}. To obtain a unity-gain voltage follower, the output terminal (drain of transistor M_{15}) is connected to the input bulk terminals of transistors M_2 and M_3 thus forming a negative feedback loop. The unity-gain current follower can be obtained using complementary transistors M_{16} and M_{18} to mirror the current from x-terminal to z-terminal.

The minimum supply voltage $\boldsymbol{V_{DD\min(in)}}$ of the input stage is given by

$$\boldsymbol{V_{DD\min(in)} = \max\left(V_{GS,Mi} + V_{DS(sat),Mj}\right)} \tag{6}$$

where i = 2, 4, 9, 10 and j = 1, 3, 5, 6. Letting $V_{DS(\mathrm{sat})} = V_{DS(sat),M15-M18}$, the minimum supply voltage $V_{DD\min(\mathrm{out})}$ of the output stage is approximately $V_{DD\min(\mathrm{out})} = 2V_{DS(\mathrm{sat})}$. Assume that circuit is biased in sub-threshold region and letting $|V_{GS}|_{,M2-M4} = V_{GS,M9-M10} = V_{DS(\mathrm{sat})}$, the $\boldsymbol{V_{DD\min}}$ of both input and output stages is $2V_{DS(\mathrm{sat})}$ which is approximately equal to 6 to 8 U_T [35], where U_T is about 26 mV at room temperature.

Assuming perfect symmetry of the first stage (M_1 – M_{14}), the voltage transfer ratios β_1, β_2, β_3, can be expressed by:

$$\boldsymbol{\beta_i = \frac{V_x}{V_{yi}} = \frac{A_{oi}}{1+A_{oi}}} \tag{7}$$

where A_{oi} (i = 1…3) is the open-loop voltage gain of the internal differential difference amplifier (M_1-M_{15} and M_{17}) from i -th input, that is given by:

$$\boldsymbol{A_{oi} = \frac{g_{mi}}{g_{ds13}+g_{ds14}} \cdot \frac{g_{m15}}{g_{ds14}+g_{ds15}}} \tag{8}$$

where, g_{dsi} and g_{mi} are respectively the output conductance and the gate transconductance of M_i respectively (i = 1…N). The transconductance g_{mi} represents the transconductance of the first stage from i-th input, which can be approximated as:

$$\boldsymbol{g_{mi} \cong 2g_{mb1,3}\frac{g_{m12,14}/g_{m9,10}}{(1-m)+g_{\Sigma}/g_{m9,10}} \cdot \left(\frac{C_{Bi}}{C_{TOT}}\right)} \tag{9}$$

where g_{mbi} denotes the bulk transconductance of M_i, $m=g_{m7,8}/g_{m9,10}$, $g_{\Sigma} = gd_{s1,3} + g_{ds7,8} + g_{ds9,10}$. The current transfer ratio α of the overall DDCC can be expressed as:

$$\boldsymbol{\alpha = \frac{g_{m16}}{g_{m15}}} \tag{10}$$

The open-loop bandwidth of the internal differential-difference amplifier mentioned above is limited mainly by the three parasitic poles associated with internal nodes of this circuit. The first pole is associated with the drain node of M_9 (M_{10}):

$$\boldsymbol{p_1 = -\frac{g_{m9,10}\left[(1-m)+g_{\sum}/g_{m9,10}\right]}{C_{\sum 1}} \cdot \left(\frac{C_{Bi}}{C_{TOT}}\right)} \tag{11}$$

where $C_{\Sigma 1}$ is the total capacitance associated with this node. The second pole is associated with the output of the first gain stage (drain terminal of M_{13}):

$$\boldsymbol{p_2 = -\left(1+\frac{g_{m15}}{g_{ds15}+g_{ds17}}\right) C_{gd15} + C_{\sum 2}} \tag{12}$$

where $C_{\Sigma 2}$ is the total capacitance associated with this node, except C_{gd15}. The third pole is associated with the x terminal of the DDCC:

$$\boldsymbol{p_3 = -\frac{g_{m15}}{C_x}} \tag{13}$$

where C_x is the total capacitance associated with the x terminal.

Assuming that the DDCC is properly frequency compensated, the poles p_1 and p_3 should be located well above the 3-dB frequency of the y-x follower. In such a case, the 3-dB frequency of the voltage gain of this follower is approximately equal to the GBW product of the internal differential-difference amplifier mentioned earlier and can be approximated as:

$$\boldsymbol{f_{3dB} = \frac{g_{mi}}{C_{gd15}}} \tag{14}$$

The 3-dB frequency of the x-z current follower is also limited by the above mentioned effects, and for y and z terminals shorted to ground for AC signals can be approximated by (14) as well.

The i-*th* input referred thermal noise of the proposed DDCC can be approximated by:

$$\overline{v_n^2} = \frac{1}{2} \cdot \frac{8kT}{3\left(g_{mb1,3}^2\right)} \Bigg[g_{m1,3} + \left(g_{m2,4} + g_{m5,6}\right)\left(\frac{g_{m1,3}}{g_{m2,4}}\right)^2 + g_{m7,8} + g_{m9,10} + (1 - m)^2 \left(\frac{g_{m9,10}}{g_{m12,14}}\right)^2 \left(g_{m12,14} + g_{m11,13}\right) \Bigg] \left(\frac{C_{TOT}}{C_{B,i}}\right)^2 \tag{15}$$

It is worth noting, that the optimum noise performance is obtained when all transistors M_1-M_4 are identical [42].

The input resistance seen from the x-terminal can be approximated as:

$$\boldsymbol{R_x \approx \frac{r_{ds14} \| r_{ds15}}{A_{oi}}} \tag{16}$$

where it is assumed that A_{oi} is identical for every i=1..3.

Finally, the output resistance of the DDCC seen from the z-terminal is given by:

$$R_z \approx r_{ds16} \| r_{ds18} \tag{17}$$

3. Simulation results

The proposed DDCC was designed and simulated using PSPICE, assuming a standard n-well 0.18 µm CMOS process. The supply voltage was 0.3 V (V_{DD} = -V_{SS} = 0.15 V). The transistor aspect ratios are given in Table 1. The bias current I_B was 5 nA and the values of capacitances C_B and C_C were 0.5 pF and 8 pF, respectively.

Table 1. Transistor aspect ratios for Fig. 3.

MOS Transistor	W/L (µm/µm)
M_1, M_2, M_3, M_4	15/1
M_5, M_6, M_7, M_8, M_B	15/0.5
M_9, M_{10}	25/0.5
M_{11}, M_{13}	60/0.5
M_{12}, M_{14}	20/0.5
M_{15}, M_{16}	500/0.2
M_{17}, M_{18}	100/0.5
M_L	5/4

The simulated DC curves V_x against V_{y1} (with V_{y2} and V_{y3} grounded) and the voltage error are shown in Fig. 4. From this figure, when the voltage V_{y1} was varied from –150 to 150 mV, the simulated voltage offset at V_{y1} = 0 was –178 µV and the voltage errors were respectively 4.3 mV and –2.9 mV when V_{y1} = +150 mV and –150 mV and the voltage errors will be less than 0.37 mV when V_{y1} = ± 100 mV.

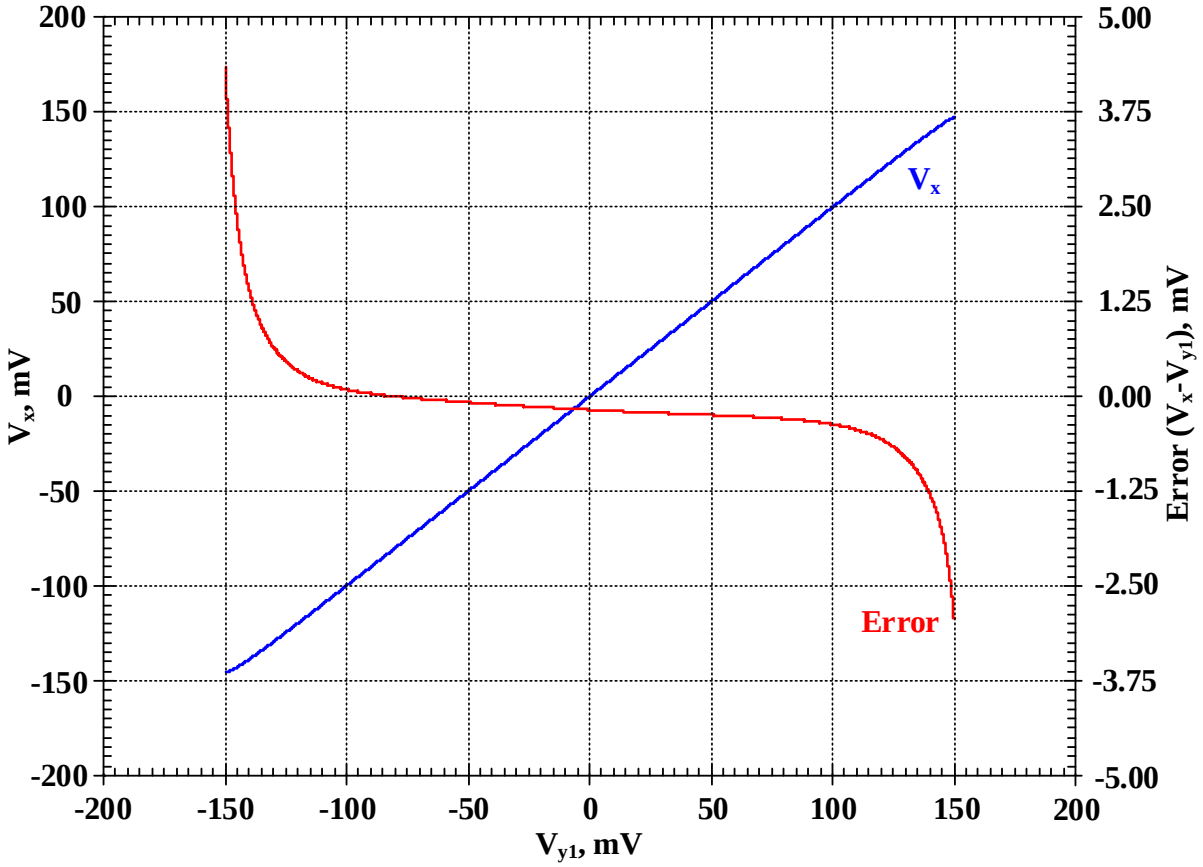

Fig. 4. DC characteristic V_x against V_{y1} (with V_{y2} and V_{y3} grounded).

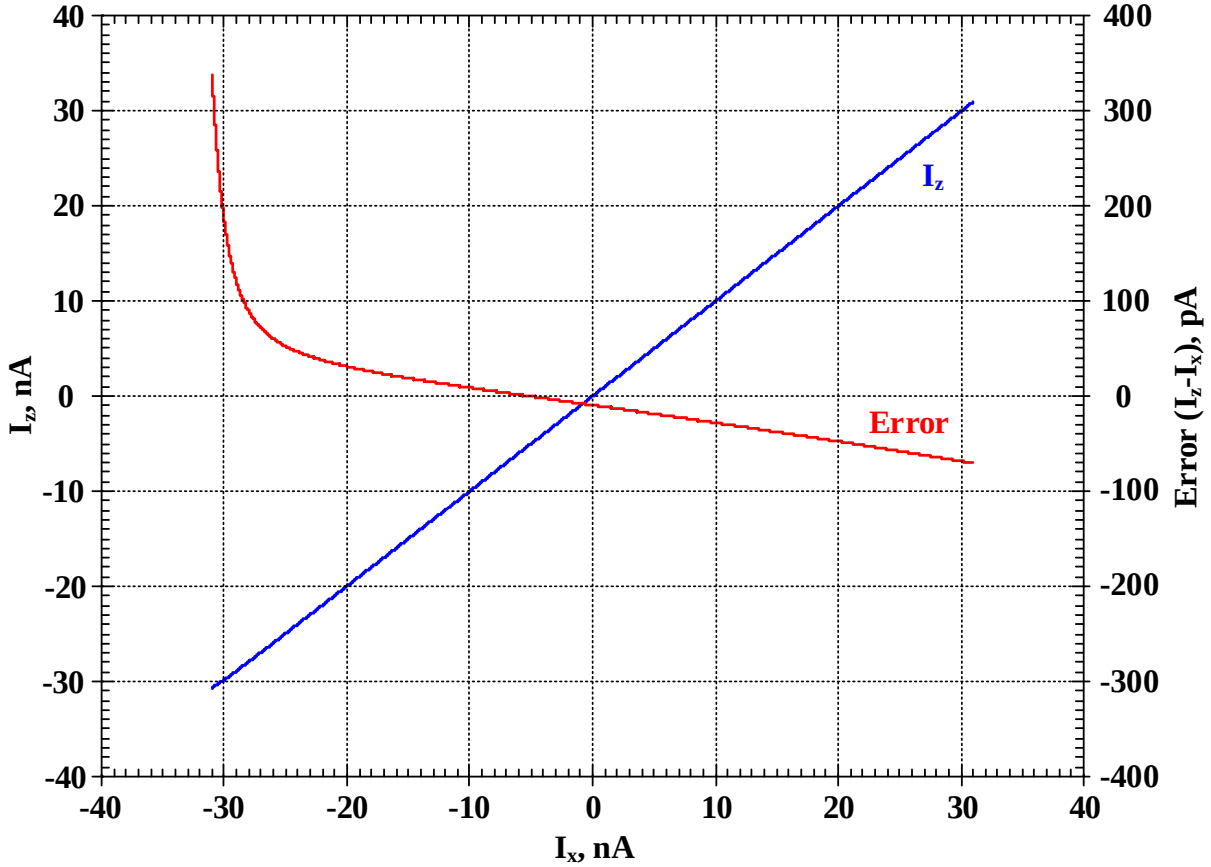

Fig. 5. DC characteristic I_z against I_x and the current error.

The simulated DC curves I_z against I_x and the current error are shown in Fig. 5. From this figure, when the voltage I_x was varied from –30 to 30 nA, the simulated current offset at I_x = 0 was –9.5 pA and the current errors were respectively 196 pA and –68.3 pA when I_x = +30 nA and –30 nA and the voltage errors will be less than 47 pA when I_x = ± 20 nA.

Fig. 6 shows the simulated frequency responses of the voltage gains V_x/V_{y1}, V_x/V_{y2}, V_x/V_{y3} with 30 pF load capacitance at x-terminal. The low frequency voltage gains for V_x/V_{y1}, V_x/V_{y2}, V_x/V_{y3} were 0.998, 0.997 and 0.998 respectively. The 3-dB bandwidth was about 2.2 kHz. This cut-off frequency is the major limitation of bandwidth of the proposed DDCC. The low frequency current gain for I_z/I_x was also simulated. From our investigation, the current gain was 0.984 and its 3-dB bandwidth was about 54 kHz.

The total harmonic distortion (THD) of the output signal at x terminal was 1 %, for the input signal of 240 mV_{pp} amplitude and 100 Hz frequency, for the load capacitance of 30 pF.

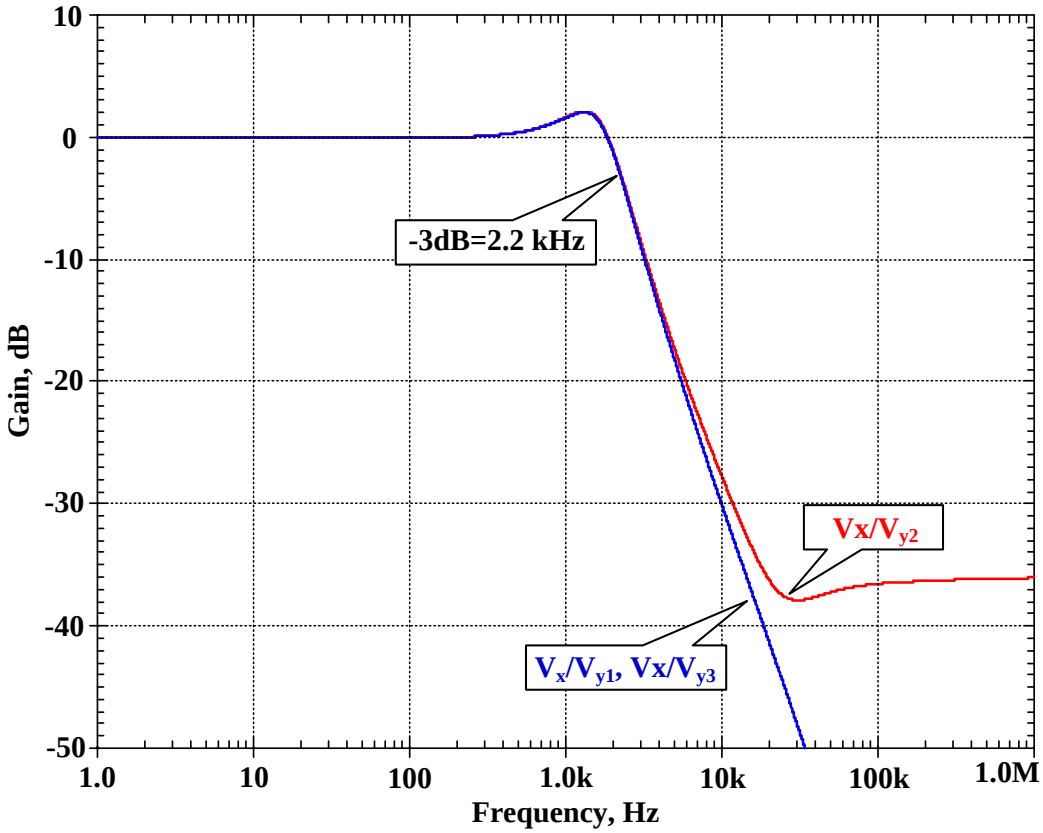

Fig. 6. Frequency responses of voltage gains; V_x/V_{y1}, V_x/V_{y2}, V_x/V_{y3}.

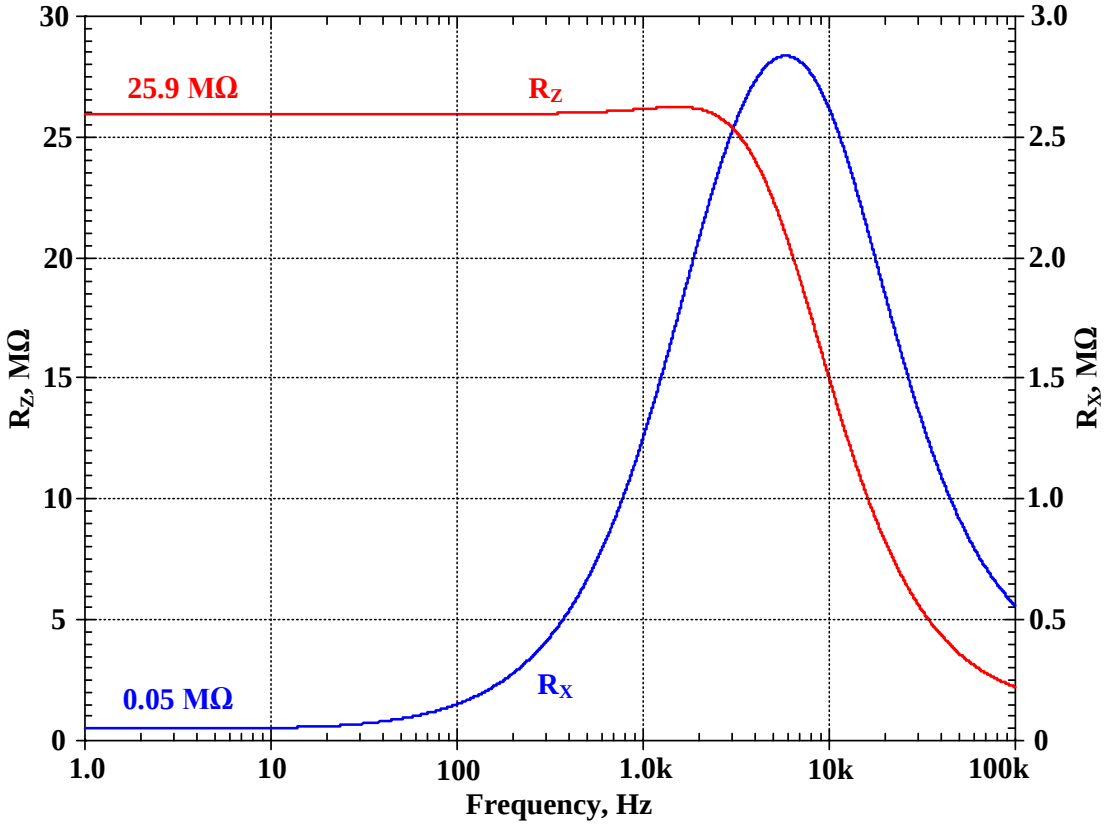

Fig. 7. Frequency dependence of parasitic impedances of z and x terminals.

Fig. 7 shows the frequency dependence of parasitic impedances of z and x terminals. From this figure, the resistance of z terminal was about 25.9 MΩ and the resistance of the x terminal was about 50.7 kΩ. The resistance of the x terminal must be taken in consideration during circuit design. The performance summary of the proposed DDCC and comparison with some previous works was shown as Table 2. The proposed DDCC operates with the lowest supply voltage of 0.3 V. If compared with DDCC in [41], the proposed DDCC offers better accuracy of voltage gain, lower DC offset and lower power consumption.

Table 2. Performance summary of the proposed DDCC compared to some previous low-voltage DDCCs.

Parameters	**Unit**	**This work**	**Ref. [37]**	**Ref. [39]**	**Ref. [40]**		**Ref. [41]**
Technique		MIBD	BD	MIBD-QFG	MIBD (Fig. 3c)	MIBD-QFG (Fig. 3d)	MIBD
Technology	µm	0.18	0.18	0.18	0.18	0.18	0.18
Power supply	V	0.3	0.6	0.5	0.4	0.4	0.3
Static power consumption	W	28.6E-9	18E-6	1.7E-6	140E-9	140E-9	38E-9
Voltage gains:							
V_x/V_{y1},	-	0.998	1	0.999	0.998	0.999	0.977
V_x/V_{y2},	-	0.997	1	0.998	0.999	0.999	0.959
V_x/V_{y3}	-	0.998	1	0.993	0.998	0.999	0.977
Current gain: I_z/I_x	-	0.984	1	0.999	0.999c	0.999c	0.998
DC voltage range	V	±150E-3	±150E-3	450E-3	400E-3	400E-3	±150E-3
Voltage offset	V	-0.17E-3	<93E-6	-	3.7E-9	3.9E-9	4.1E-3
DC current range	A	±30E-9	±8E-6	±1E-6	±95E-9	±95E-9	±50E-9
Current offset	A	-9.5E-12	<3E-9	-	0.3E-9	0.4E-9	0.497E-9
-3dB bandwidth:							
V_x/V_{y1}, V_x/V_{y2}, V_x/V_{y3}	Hz	2.2E3	27E6	149E3	10.99E3	19.05E3	4.9E3
I_z/I_x	Hz	54E3	27E6	250E3	15.3E3c	24.4E3	98E3
Parasitic parameters:							
R_x	kΩ	50.7	1.6	-	37c	12c	76.96
R_z	MΩ	25.9	10.38	-	40c	40c	48.8
Load capacitance	pF	30	-	30	30	30	30
$(V_{TH}/V_{DD})\times100$ (%)	%	166	66.66	100	100	100	166
Chip area	mm^2	-	-	0.0273	0.017628	0.0273	0.017
Obtained results	-	Sim.	Sim.	Meas.	Meas.	Meas.	Sim.

5. Sixth-order Butterworth low-pass filter

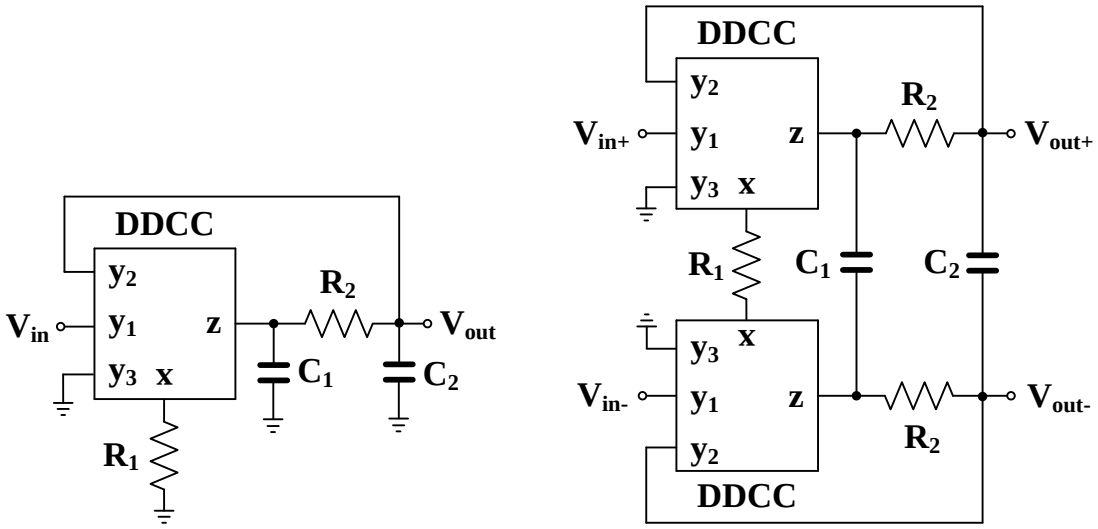

Fig. 8. Second-order low-pass filter: (a) single-ended filter, (b) fully differential filter.

A sixth-order Butterworth low-pass filter proposed in this work and based on the proposed DDCC is a cascade connection of three second-order low-pass filters shown in Fig. 8. Figs. 8 (a) and (b) show a single-ended and fully-differential versions of the filter respectively. The transfer function of the filter in Fig. 8 (a) can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{C_1C_2R_1R_2}}{s^2+s\frac{1}{C_1R_1}+\frac{1}{C_1C_2R_1R_2}} \tag{15}$$

The natural frequency (ω_o) and the quality factor (Q) are given by

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{16}$$

$$Q = \sqrt{\frac{C_1R_1}{C_2R_2}} \tag{17}$$

The fully differential version of the filter shown in Fig. 8(b) offers many advantages especially for ultra-low supply voltage circuits. It can increase the dynamic range, provide immunity to external noise and decrease nonlinear distortion. Fig. 9 shows the realization of the proposed fully-differential sixth-order Butterworth low-pass filter.

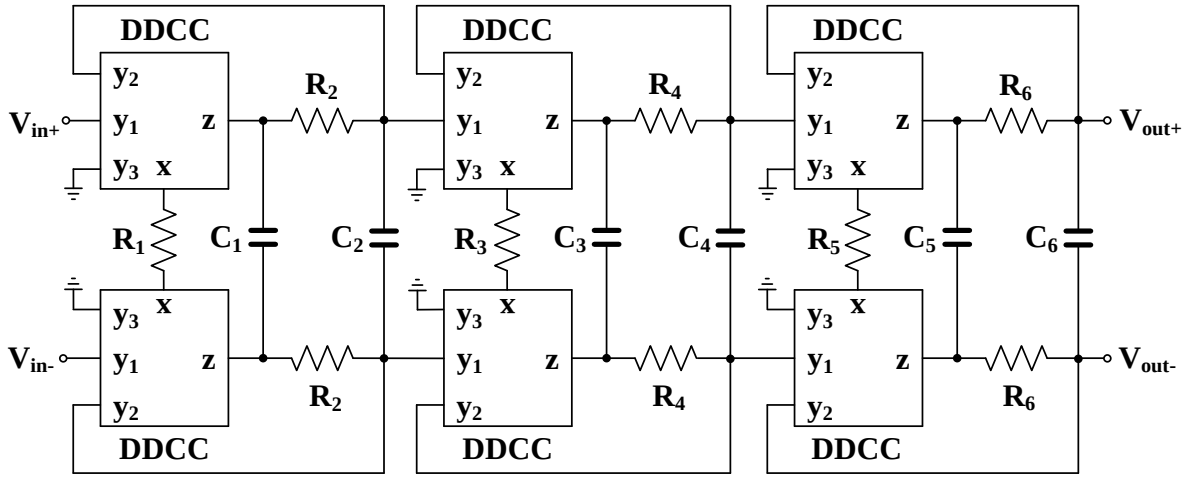

Fig. 9. Sixth-order Butterworth low-pass filter.

The sixth-order maximally flat low-pass filter was designed by cascading three second-order low-pass filters, which are arranged as follows: stage 1, frequency scaling factor (FSF) = 1, Q = 0.518: stage 2, FSD = 1, Q = 0.707: stage 3, FSF = 1, Q = 1.932. Therefore, the normalized transfer function of sixth-order Butterworth low-pass filter is:

$$\frac{V_{out(s)}}{V_{in(s)}} = \left(\frac{1}{s^2+1.93s+1}\right)\left(\frac{1}{s^2+1.414s+1}\right)\left(\frac{1}{s^2+0.518s+1}\right) \quad (19)$$

The proposed sixth-order Butterworth low-pass filter was designed with the cut-off frequency f_o of 100 Hz. The first stage, second stage and the third stage were designed with the cut-off frequencies of 70 Hz, 100 Hz and 148 Hz, respectively. The value of capacitances C_1 and C_2 of each stage will be equalled and the value of resistances R_1 and R_2 of each stage will be used to adjust the value of quality factor. Thus the filter in Fig. 9 was designed as follows: $C_1 = C_2$ = 300 pF, R_1 = 5.8 MΩ, R_2 = 3 MΩ, $C_3 = C_4$ = 220 pF, R_3 = 5.8 MΩ, R_4 = 2.5 MΩ, $C_5 = C_6$ = 220 pF, R_5 = 1.8 MΩ, R_6 = 14 MΩ. In practice, these high values of resistances and large values of capacitance can be implemented off-chip. The high values of resistances were used because the high linearity and wide input range of filter can be obtained.

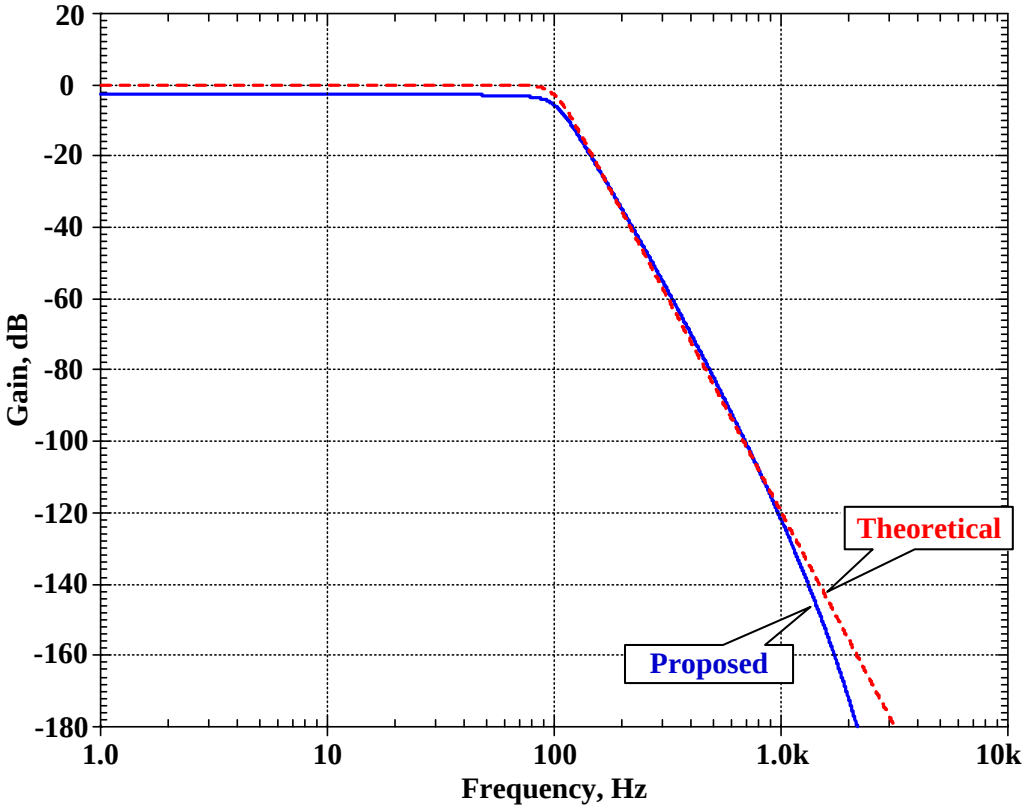

Fig. 10. Simulated frequency response of the sixth-order Butterworth low-pass filter.

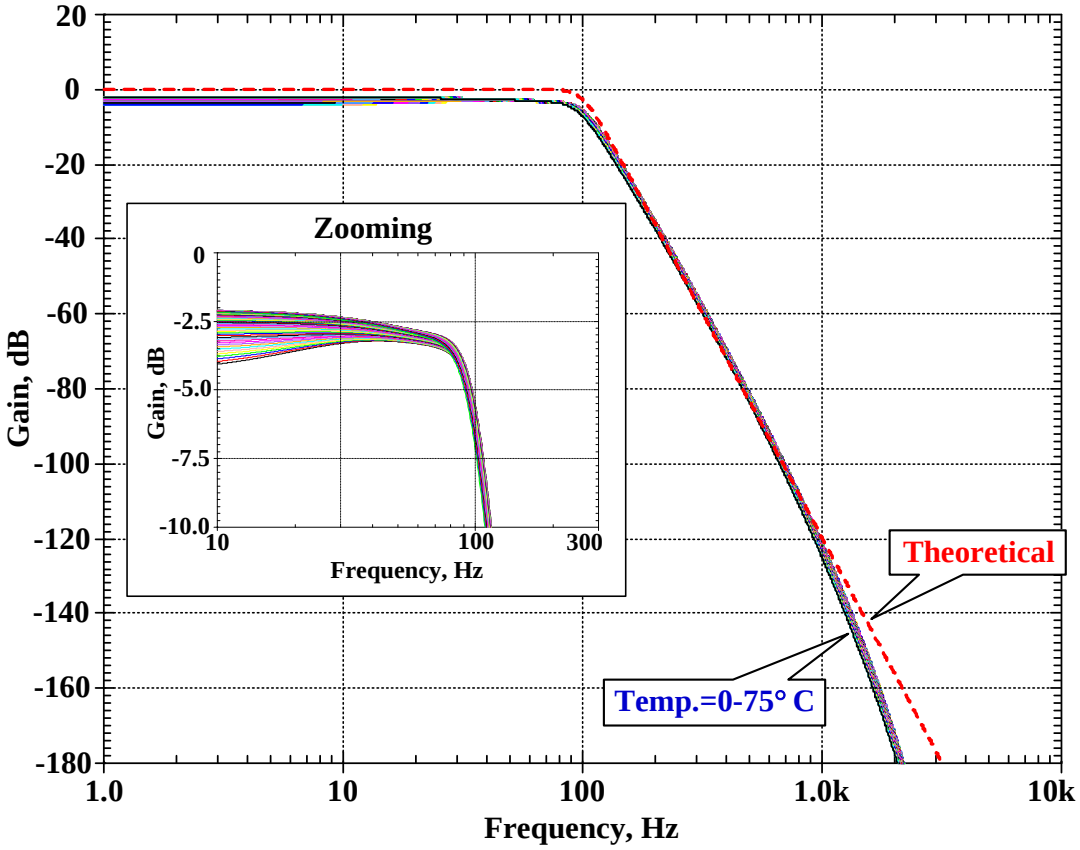

Fig. 11. Simulated frequency response of the sixth-order Butterworth low-pass filter for different temperature.

Fig. 10 shows the simulated frequency responses of the proposed sixth-order Butterworth low-pass filter. The cut-off frequency of the filter was 99 Hz and the DC voltage gain was -2.4 dB while the filter consumed 172 nW of power**.** The simulated frequency response was also compared with theoretical curve. Fig. 11 shows the variations of the frequency response for temperature varied from 0 to 75 °C. The simulation result shows that the DC voltage gain varied between -2.12 dB and -4.34 dB, whereas the variations of the cut-off frequency of the filter were negligible.

Fig. 12 shows the simulated transient response of the filter when the 10 Hz sinusoidal input voltage signal with the amplitude of 240 mV (peak-to-peak) was applied. This result can be shown the operation of input voltage swing of 240 mV (peak-to-peak) with the total harmonic distortion (THD) of 1.09 %.

To test the linearity of the proposed filter, a single tone test and two-tone test have been investigated. Fig. 13 shows the results of the single tone test of the proposed filter when the input frequency of 10 Hz was supplied whereas amplitude of input sinusoidal voltage was varied. The THD was 1.09 % when the amplitude of input voltage was increased to 240 mV (peak-to-peak). The two-tone test has been investigated by applying two input frequencies of 50 Hz and 60 Hz into the circuit and the amplitude of input sinusoidal voltages was varied. The simulated 3^{rd} inter-modulation distortion (IMD) was shown in Fig. 14. It can be found that amplitude of the output signal for a 2% 3^{rd} IMD was 50 mV while the amplitude of the input signal was 140 mV (peak-to-peak).

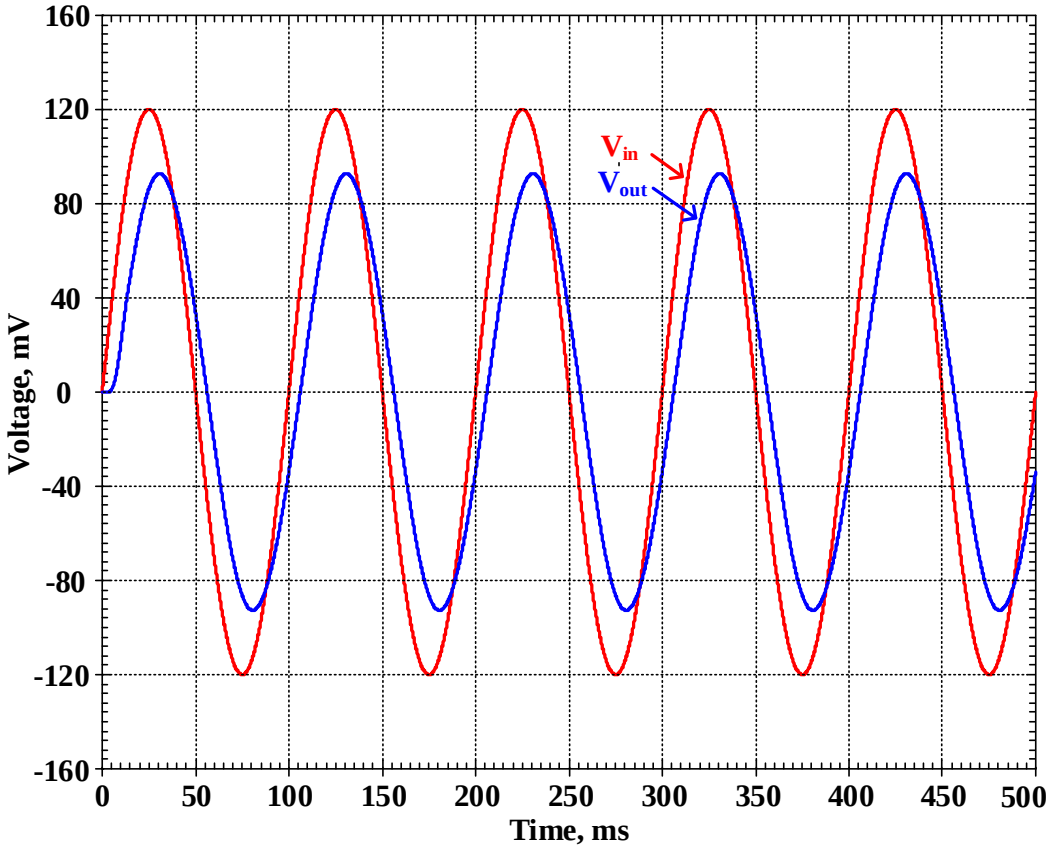

Fig. 12. Simulated transient response with input voltage swing.

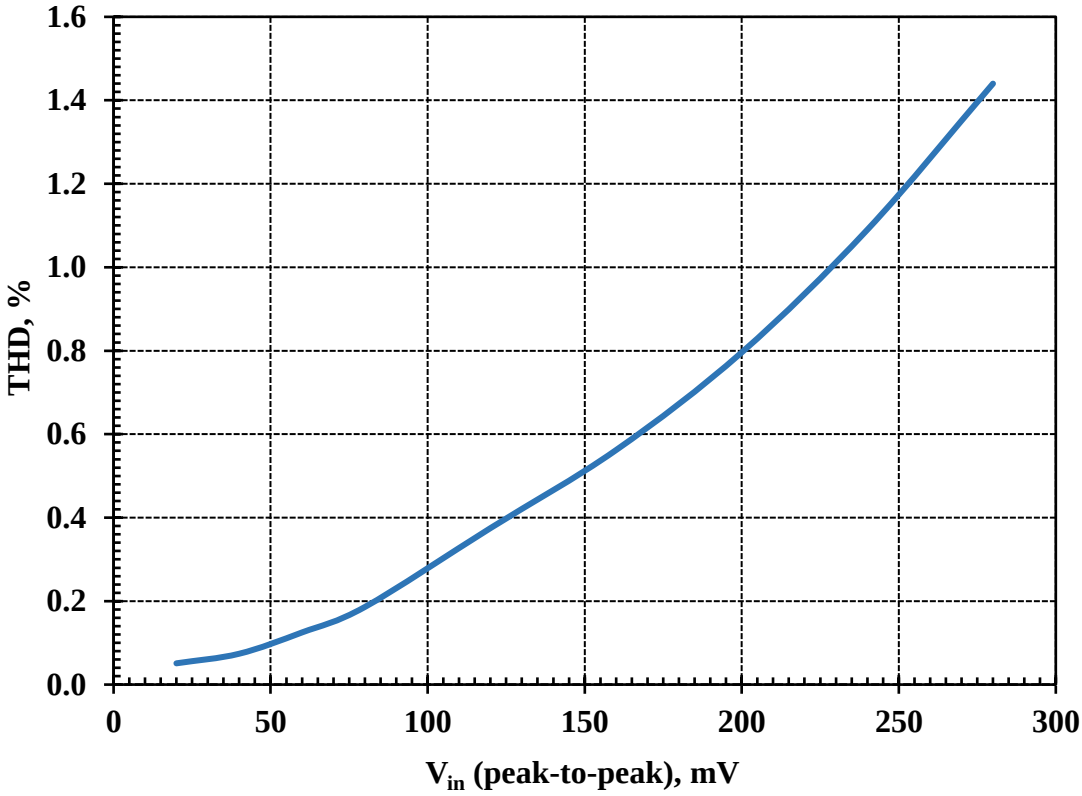

Fig. 13. THD variation versus amplitude of the input sinusoidal voltage at 10 Hz.

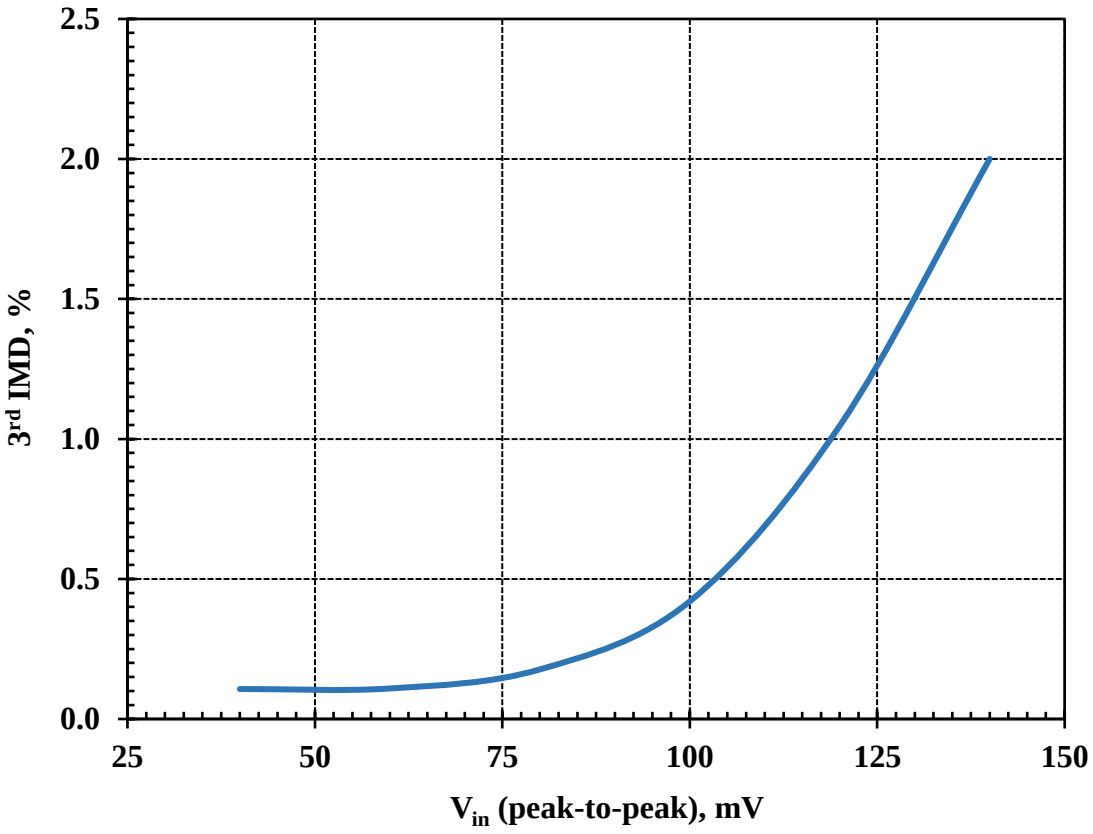

Fig. 14. The third-order IMD versus the input voltage.

In case of noise testing, the proposed sixth-order Butterworth low-pass filter was simulated to evaluate the integrated input reference noise for the bandwidth of 100 Hz. From our simulation, it can be found that an input-referred noise voltage was 338 μV_{rms} whereas an output- referred noise voltage was 238 μV_{rms}. If a single-tone test has been used to define the dynamic range (DR), at THD of 1.09 % (V_{in} = 84.8 mV_{rms}), the DR was 48 dB.

The proposed sixth-order low-pass filter has been compared with previous works [23], [24], [43]-[45] as shown in Table II. It can be shown that the proposed DDCC can be applied to biomedical systems because the circuit can operate with ultra-low supply voltage and ultra-low power consumption. In order to evaluate and compare the performance of the filters in Table II, the following standard Figure of Merit (FoM) [46] was used

$$FoM = \frac{P \times V_{DD}}{N \times f_c \times DR} \quad (20)$$

Table II. Comparison of the proposed filter to some previous sixth-order low-pass filters.

	This work	2000 [43]	2014 [44]	2019 [23]	2019 [24]	2019 [45]
Technology [µm]	0.18	0.8	0.35	0.13	0.18	20
Supply voltage [V]	0.3	±1.5	0.5	0.25	1	10
Topology	CMOS	CMOS	CMOS	CMOS	CMOS	a-IGZO TFT
Number of active	6-DDCC	8-OTA	50-MOS	5-FDDTA, 1-OTA	6-OTA	3-DDA
Number of passive	9-R & 6-C	6-C	6-C	5-C	5-C	15-C, 24-MSW†
Filter order	6^{th} LP (Butterworth)	6^{th} LP (Butterworth)	6^{th} LP (Bessel)	5^{th} LP (Butterworth)	5^{th} LP (Butterworth)	6^{th} LP (Butterworth)
Architecture	Fully diff.	Single-ended	Single-ended	Fully diff.	Fully diff.	Fully diff.
Bandwidth [Hz]	99	2.4	2.4	100	250	272
Noise [μV_{rms}]	339	<50	0.43E-12 A*	4.7	134	-
DC gain [dB]	-2.5	-10	0	~ -6	-7	-0.65
Power consumption [W]	172E-9	10E-6	7.21E-9	603E-9	41E-9	0.537E-3
Dynamic range [dB]	48@1%THD	60@0.5%THD	51.1@4%THD	57	61.2	-
FOM	1.76E-12	3.47E-8	4.9E-12	5.29E-12	5.47E-13	-

Note: * current-mode filter, † MSW = MOS switch,

a-IGZO TFT = amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistor (TFT)

DDA = differential difference amplifier, R = resistor, C = capacitor

FDDTA = fully differential difference transconductance amplifier,

OTA = operational transconductance amplifier

5. Conclusion

This paper presents a new differential difference current conveyor (DDCC) with ultra-low voltage and low-power capability for application to biomedical systems. The DDCC is designed by using a non-tailed differential pair with multiple-input bulk-driven MOS transistor technique to obtain a rail-to-rail input common-mode range and extremely low supply voltage. The MOS transistors biased in the sub-threshold region have been used to achieve ultra-low power consumption. The proposed DDCC is capable of operating with a supply voltage as low as 0.3 V and consumes about 28.6 nW of static power. The proposed DDCC has been used to realize a sixth-order Butterworth low-pass filter for application to electrocardiogram systems as application example. The performance of the proposed DDCC is evaluated by simulation results using SPICE program and MOS transistors parameters provided by a standard n-well 0.18 µm CMOS process from TSMC.

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