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0.5 V Current-Mode Low-Pass Filter Based on Voltage Second Generation Current Conveyor for Bio-Sensor Applications

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ABSTRACT This paper presents a low-voltage low-power current-mode third-order low-pass filter (LPF) based on voltage second generation current conveyor (VCII). The VCII utilizes the bulk-driven MOS transistor technique to achieve a wide input voltage range at low supply voltage of 0.5 V. Also, the VCII operates in the subthreshold region to achieve nano-power consumption of 390 nW. A third-order low-pass filter that is presented as an application of the VCII can operate as both current- and transimpedance-mode filters. The filter consumes 2.73 μW and the total harmonic distortion (THD) is below 1 % for sine-wave input signal below 350 nA_{pp} @ 10 Hz. The post-layout simulation results based on TSMC 0.18 μm CMOS process are presented and confirms the futures of the filter.

INDEX TERMS Voltage second generation current conveyor, third-order low-pass filter, current-mode filter, low-voltage low-power, analog circuit.

I. INTRODUCTION

Recently, there is a gaining research interest for current-mode technique of the filter design. Compared with the voltage-mode counterparts the current-mode filters have been presented in the literature exhibiting improved performance [1]. There are several current-mode building blocks for realization high-order current-mode filters such as current differencing buffered amplifier (CDBA) [2], current-mirror [3] and current differencing transconductance amplifier (CDTA) [4], [5] available in literature. The developed filter topologies provide a higher maximum frequency of operation and a more accuracy of transfer function due to smaller parasitic parameters compared with the filters realized using voltage-mode op-amp configurations [6].

The high-order filter can be applied to biomedical systems devoted to applications in electroencephalographic (EEG), electromyographic (EMG), and electrocardiographic (ECG) systems. The frequency/amplitude ranges for EEG, EMG and ECG signals are respectively 0.05−60 Hz/15−100 μV, 10−200 Hz/0.1−5 mV and 0.05−250 Hz/100 μV−5 mV [7]. Since these signals attributes small amplitude and low frequency, high-order filters for applications to these systems should be designed to meet high dynamic range and low-power consumption. The analog low-pass filter is usually required to select the frequency range and eliminate out-of-band noise in the front-end of biomedical systems. The high-order filter based on the RLC prototype is usually required due to lower pass-band sensitivity compared with the cascade approach using biquads.

Voltage second generation current conveyor (VCII) was introduced in [8]–[10]. Conventional VCII has three terminals (y, x, and z), the first stage between y and x terminals is a current follower and cascaded by a voltage follower between x and z terminals as the second stage. This device is designed to obtain a low impedance voltage output node for avoiding an extra voltage buffer for application requiring a voltage output signal [11]. The required additional voltage buffer can lead to higher power consumption and a large chip area. A number of VCII structures have been reported recently in literature [11]–[18]. Unfortunately, these structures are designed by rather high supply voltage and high-power consumption such as ±1.65 V/330 μW in [11], ±0.9 V/120 μW in [12], ±1.65 V/320 μW in [13], ±0.9 V/664 μW in [16],

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±0.45 V/79.3 μW in [18]. Therefore, these VCIIs are not suitable for applications to ultra-low power analog signal processing. There are interesting applications of VCII available literature such as simulated inductor [15], universal filter [19]–[21], first-order all-pass filter [22], capacitance sensors [23], and full wave rectifier [24].

In this work, a current-mode third-order low-pass filter based on voltage second generation current conveyor for bio-sensor applications is proposed. The proposed VCII is designed using bulk-driven (BD) MOS technique to provide wide input voltage range while the MOS operates in subthreshold region to obtain low-voltage low-power operation. The VCII is designed to work with voltage supply $V_{DD} = 0.5$ V and power consumption is 390 nW. The proposed third-order filter was designed and simulated in the Cadence environment using a 0.18 μm CMOS process from TSMC. Post-layout Simulation results show that the filter offers a bandwidth (BW) of 250 Hz, and a power consumption of 2.73 μW.

II. PROPOSED CIRCUIT

A. 0.5 V VCII

Fig. 1(a) shows the symbol of VCII and its equivalent circuit is shown in Fig. 1(b). The relation between the terminal voltages and current can be described by

$$\begin{pmatrix} i_X \\ v_Y \\ v_Z \end{pmatrix} = \begin{pmatrix} 1/r_x & \beta & 0 \\ 0 & r_y & 0 \\ \alpha & 0 & r_z \end{pmatrix} \begin{pmatrix} v_X \\ i_Y \\ i_Z \end{pmatrix} \tag{1}$$

where β is the current gain and α is the voltage gain of VCII (unity for the ideal case). It should be noted from (1) that the relation between x and y terminals is the current follower and the relation between z and x is the voltage follower, where r_y, r_x, and r_z are respectively the parasitic resistance at y, x, and z terminals.

Fig. 2 shows the proposed VCII that is consists of two op-amps operating in unity gain feedback, firstly presented in [25], [26]. The first op-amp has two outputs and is created by transistors M_1-M_4 and M_9-M_{12} that ensure the unity gain current transfer $I_x = I_y$. The second op-amp is created by M_5-M_7 and M_{13}-M_{15} that ensure the unity gain voltage transfer $V_z = V_x$. The bias current I_B and transistor M_8 set the currents of the VCII. For the first op-amp, transistor M_1, M_2 create non-tailed differential amplifier loaded by current mirrors M_9, M_{10}, the second stage is created by transistor M_3 loaded by the current source M_{11}. The bulk-drain terminals of M_3 and the bulk terminal of M_2 are connected together that creates a negative unity feedback connection. Transistors M_4, M_{12} create a copy of the current M_3, M_{11}. The minimum voltage supply of this structure is:

$$V_{DDmin} = \max\left(V_{SGM2} + V_{DSsatM10}\right) \tag{2}$$

where V_{SG} and V_{DSsat} are the source-gate voltage and saturation voltage of the MOS transistor, respectively.

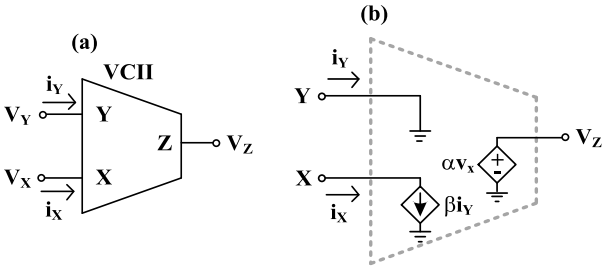


FIGURE 1. VCII (a) symbol, (b) equivalent circuit.

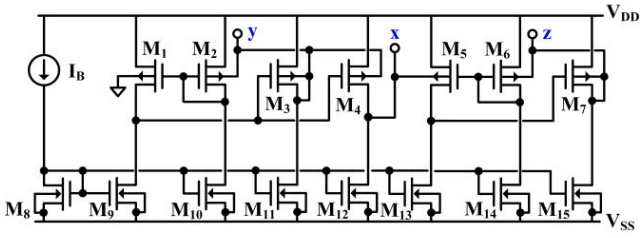


FIGURE 2. Proposed VCII.

The output resistances of the y, x and z terminals can be calculates as:

$$r_y \cong \frac{g_{oM1} + g_{oM6}}{g_{mM3} g_{mbM1}} \tag{3}$$

$$r_x = \frac{1}{g_{oM4} + g_{oM12}} \tag{4}$$

$$r_z \cong \frac{g_{oM5} + g_{oM13}}{g_{mM7} g_{mbM6}} \tag{5}$$

where g_m, g_{mb}, g_o are the transconductance, bulk transconductance and output conductance of the MOS transistor, respectively.

The input referred thermal noise is determined by the input noise of the input differential stage:

$$\bar{v}_n^2 = 2\frac{2nkT}{g_{mbM1}^2}\left(g_{mM1,M2} + g_{mM9,M10}\right) \tag{6}$$

where n is the subthreshold slope factor, k is the Boltzmann constant and T is the temperature.

B. PROPOSED FILTER

Fig. 3 shows the doubly terminated RLC ladder third-order low-pass filter by R_s and R_L are connecting at the input and output ports respectively. Using KCL routine analysis the voltage and current relationship in several nodes can be written as:

$$I_1 = I_{in} - \frac{V_1}{R_s} - I_2 \tag{7}$$

$$V_1 = \frac{I_1}{sC_1} \tag{8}$$

$$I_2 = \frac{V_1 - V_2}{sL_2} \tag{9}$$

$$V_3 = \frac{I_2 - I_{RL}}{sC_2} \tag{10}$$

$$I_3 = I_2 - I_{RL} \tag{11}$$

where $I_{RL} = I_{out}$ and $V_3 = V_{out}$. Using (7)-(9), signal flow graph of RLC low-pass filter can be shown in Fig. 4. It should be noted that three lossless integrators are required for realizing third-order low-pass filter.

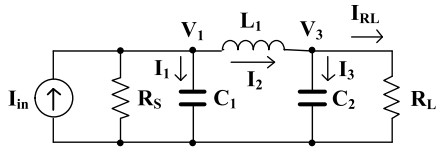


FIGURE 3. Third-order RLC prototype.

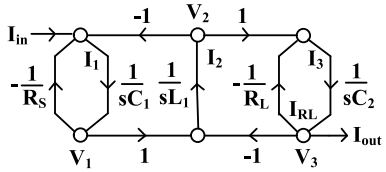


FIGURE 4. Signal flow graph of RLC prototype low-pass filter.

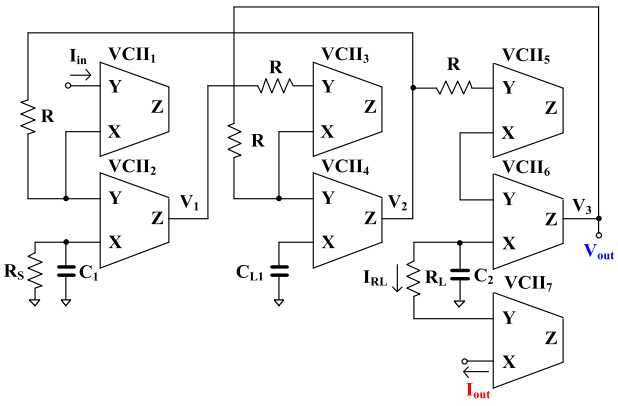


FIGURE 5. Proposed third-order filter based on VCII.

Fig. 5 shows the proposed current-mode third-order low-pass filter using VCIIs. The $VCII_1$, $VCII_2$, C_1 are worked as a first integrator while $VCII_3$, $VCII_4$, C_{L1} are worked as a second integrator and $VCII_5$, $VCII_6$, C_2 are worked as a third integrator. The inductor L_2 in the RLC prototype can be converted to the capacitor C_{L1} through the VCII and R by $L_2 = C_{L1}R^2$. The $VCII_7$ is used to provide high-output impedance for current-mode circuit. Thus, the proposed current-mode filter offers low-input impedance and high-output impedance which is meet for current-mode circuit. From the property of VCII such as $V_z = V_x$, node V_3 can also be used as output voltage terminal (V_{out}). In this case, the filter works as a transimpedance-mode filter which is meet a low-input impedance and a low-output impedance. The $VCII_7$ can be vanished and the resistor R_L must be connected to ground if it works as a transimpedance-mode filter.

III. SIMULATION RESULTS

The VCII was designed and verified in Cadence Analog Environment using 0.18 μm TSMC CMOS technology. The supply voltage was 0.5 V ($V_{DD} = -V_{SS} = 0.25$ V) and the bias current I_B was 20 nA. The transistors aspect ratio in μm/μm were for M_1, M_2, M_5, M_6, M_8 = 50/1, M_3, M_4, $M_7 = 5 \times 50.1$, M_9, M_{10}, M_{13}, M_{14} = 100/1, M_{11}, M_{12}, $M_{15} = 5 \times 100.1$. The layout of the VCII is shown in Fig. 6 with chip area 158 μm$\times$ 140 μm.

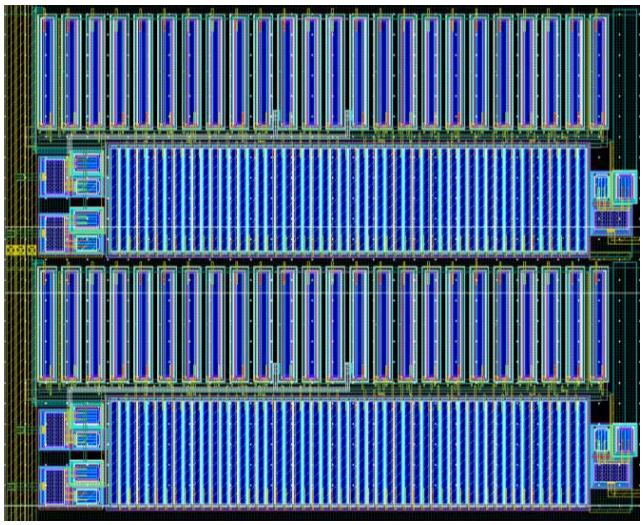


FIGURE 6. The layout of the VCII.

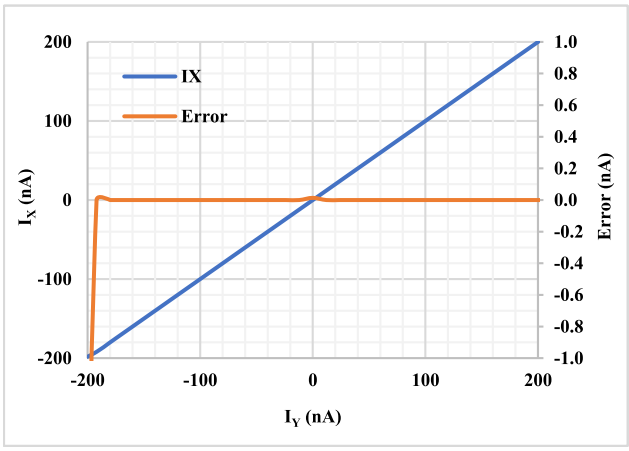


FIGURE 7. DC current characteristic and current error of the VCII.

The DC current characteristic of I_X versus I_Y and current error are shown in Fig. 7. The circuit has good linearity in the range of $\pm$190 nA. Note, that even though the input current range is relatively low, it is sufficient for the proposed application. Fig. 8 shows the DC voltage characteristic of V_Z versus V_X and voltage error. The low voltage error is evident for $\pm$200 mV voltage range.

The impedance frequency characteristics of Z_X, Z_Y and Z_Z are shown in Fig. 9. At low frequencies the X terminal

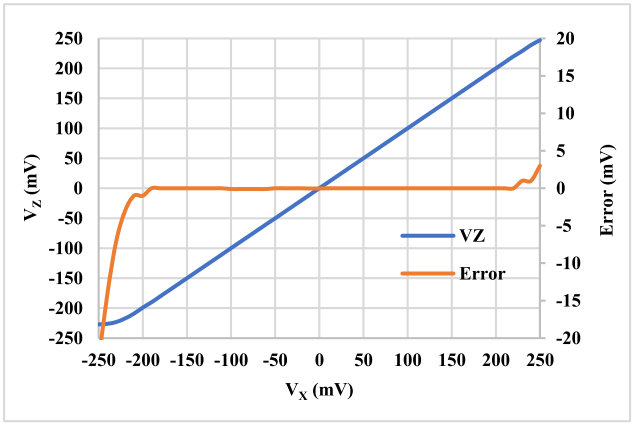
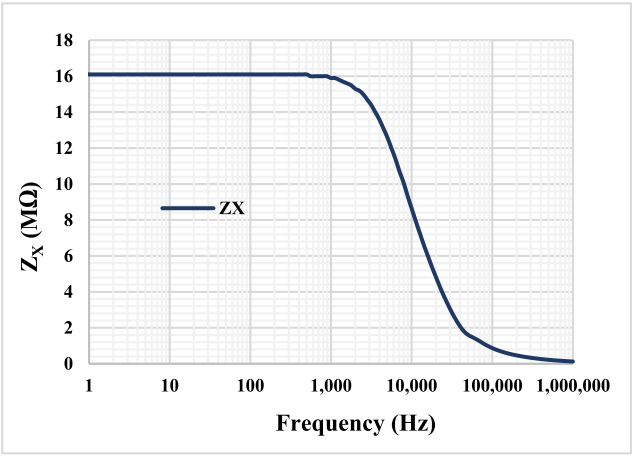
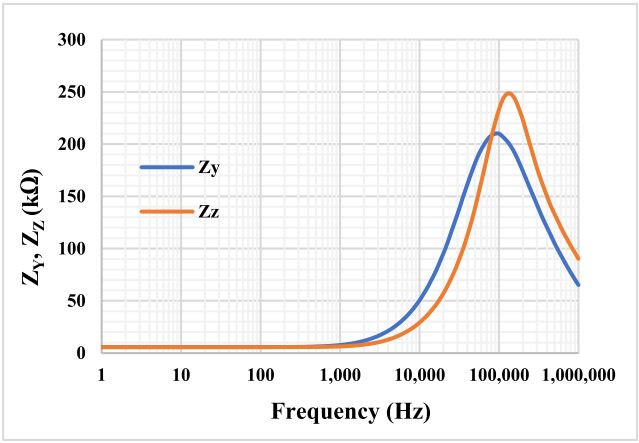


FIGURE 8. DC voltage characteristic and voltage error of the VCII.



(a)



(b)

FIGURE 9. The impedance frequency characteristics of a) Z_X, and b) Z_Y and Z_Z of the VCII.

enjoys high output resistance $R_X = 16.1$ MΩ while the resistances $R_Y = R_Z = 5.63$ kΩ. The value of these parasitic resistances of Y and Z terminals should be taken into account during the design of the applications. The voltage and current input-referred noises (IRN) of the VCII at Z and X node, respectively, are shown in Fig. 10. The voltage IRN is 500nV, while the current IRN is 0.481pA @ 1 kHz.

The performances of the VCII are presented in the Table 1 and compared to most recent VCIIs presented in the literature [12], [13], [18], [22]. It is evident that the proposed structure has the lowest supply voltage, lowest power consumption with extended input voltage range ±200 mV that make it suitable for bio-sensor applications. Also the efficient of the design and the low voltage operation capability are confirmed by the figure of merits $(V_{TH}/V_{DD}) \times 100$ (%) and $(V_{in\text{-}max}/V_{DD}) \times 100$ (%).

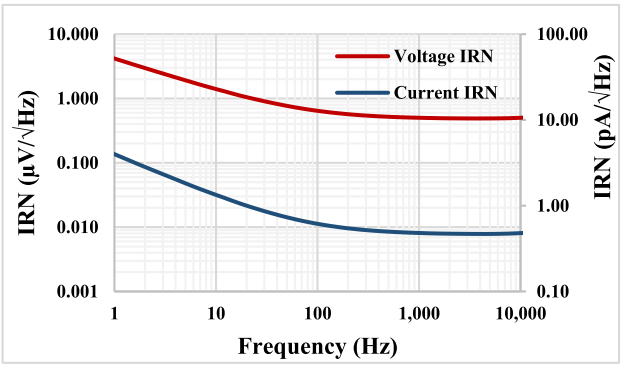


FIGURE 10. Voltage and current input-referred noises.

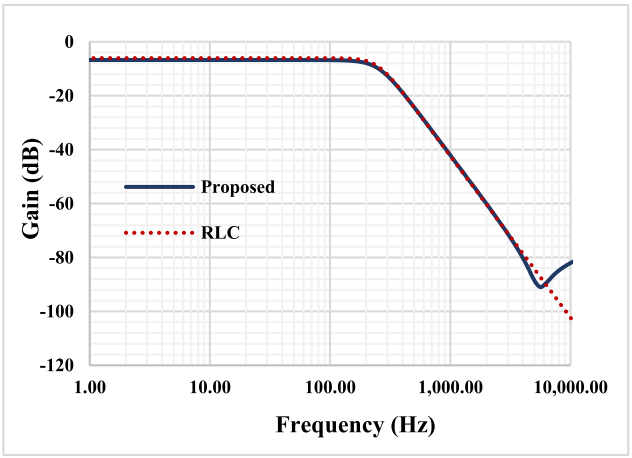


FIGURE 11. Frequency characteristics of the proposed and RLC filter.

Fig. 11 shows the frequency characteristics of the proposed and the RLC filter. The gain at low frequencies is −6.7 dB and −6.02 dB for the proposed and RLC filter, respectively, while the −3 dB is 248.2 Hz for both filters. The tuning capability with R varied from 440 kΩ to 1440 kΩ is shown in Fig. 12 the −3 dB is varied form 360.6 Hz to 96.17 Hz, respectively.

The histograms of Monte-Carlo (MC) 200 runs for gain and −3 dB bandwidth are shown in Fig. 13. The mean value of the gain is around −6.713 dB with standard deviation around 113.6 mdB. For the −3 dB BW the mean

TABLE 1. Compassion between proposed VCII and others.

	Proposed	CSSP [18] 2021	IET [22] 2020	[12] 2019	[13] 2020
Technology (μm)	0.18	0.18	0.18	0.15	0.35
Voltage supply (V)	0.5	0.9	1.8	1.8	3.3
Power consumption (nW)	390	79 300	458 000	120 000	320 000
Current gain β	0.999	0.987	1.017	0.996	0.987
Voltage gain α	0.999	0.972	0.978	0.973	0.992
DC linearity of current gain (nA)	±190	±25000	NA	±500000	NA
DC linearity of voltage gain (mV)	±200	±60	NA	±800	NA
Bandwidth of current gain (kHz)	351.8	225 000	NA	165 000	22 400
Bandwidth of voltage gain (kHz)	74.3	49300	NA	55000	220 000
r_y (kΩ)	5.63	2.7	0.0237	0.023	2E-6
r_x (MΩ)	16.1	0.1565	0.00068	522	0.37
r_z (kΩ)	5.63	0.0382	0.0237	0.16	2E-6
Offset voltage (mV)	2*	NA	NA	NA	NA
Offset current (nA)	1.73*	300	NA	NA	NA
Voltage IRN (nV/√Hz)	500 @ 1 kHz	21.67 @ 10 MHz	NA	NA	154
Current IRN (pA/√Hz)	0.481 @ 1 kHz	4.96 @ 10 MHz	NA	NA	NA
Chip area (μm^2)	22 120	509.6	NA	NA	75 155
$(V_{TH}/V_{DD})\times100$ (%)	100	55.5	27.7	33.3	21.2
$(V_{in\text{-}max}/V_{DD})\times100$ (%)	80	6.6	NA	88.8	NA
Achieved result	Post-layout	Post-layout	Pre-layout	Pre-layout	Pre-layout

* 3sigma

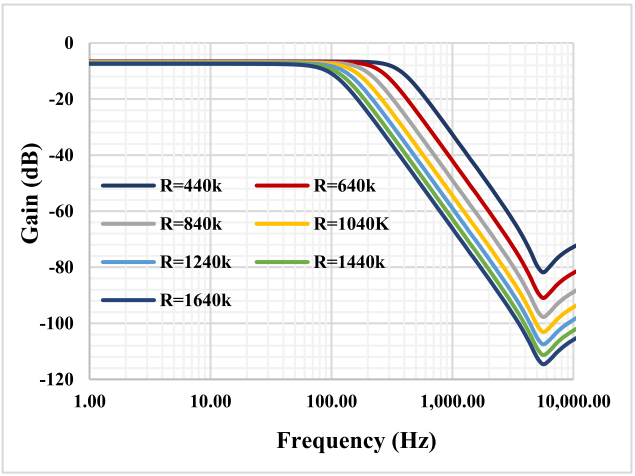


FIGURE 12. Frequency characteristics of the proposed filter with various R.

value is around 248.3 Hz with standard deviation around 1.93 Hz.

The process, voltage and temperature (PVT) corners analysis were carried out with transistor corners: ss, sf, fs, ff, voltage supply corners ±10% of V_{DD}, and temperature corners −20 °C to 70 °C. The results of the frequency characteristics of the proposed filter with PVT corner analysis are shown in Fig. 14. The minimum −3dB BW = 238.2 Hz and the maximum = 250 Hz. The minimums and maximum gain were around −6.67dB and −6.98 dB, respectively.

The transient analysis of the filter is shown in Fig. 15. The input sine wave signal applied to the filter In = 50 nA_{pp} @10 Hz. The THD of the output signal is 0.09 %. The filter was tested for different peak-to-peak signal

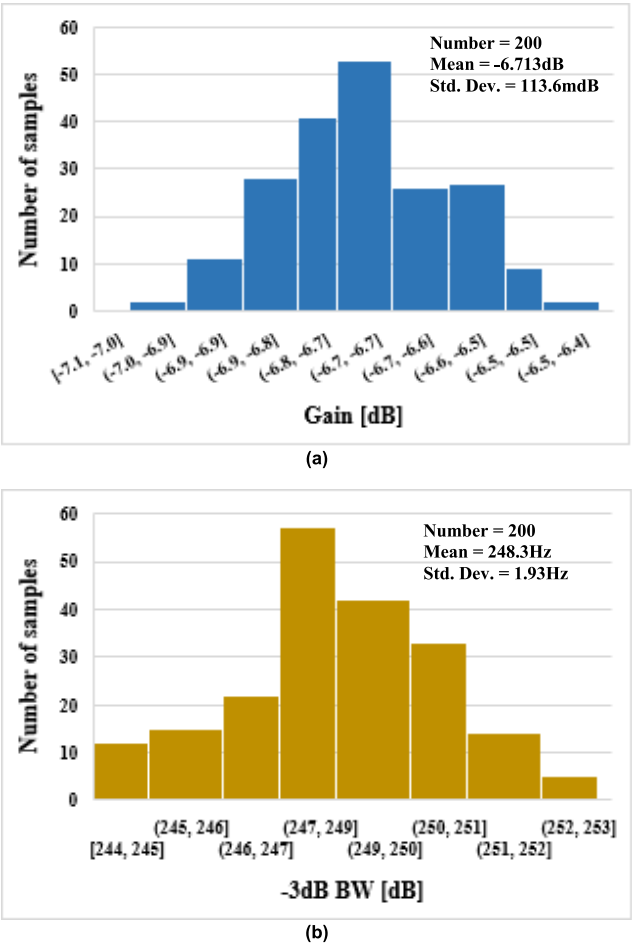


FIGURE 13. The histogram of the filter: a) gain and b) −3dB bandwidth.

and with 100 Hz, the results of THD is shown in Fig. 16. The THD is below 1 % for input signal below 350 nA_{pp}.

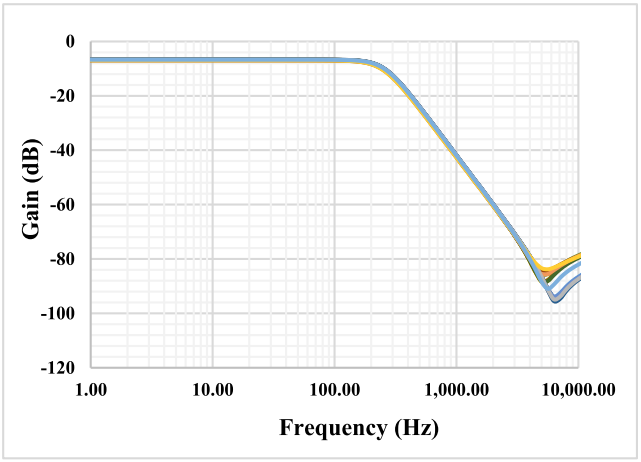


FIGURE 14. Frequency characteristics of the proposed filter with PVT corner analysis.

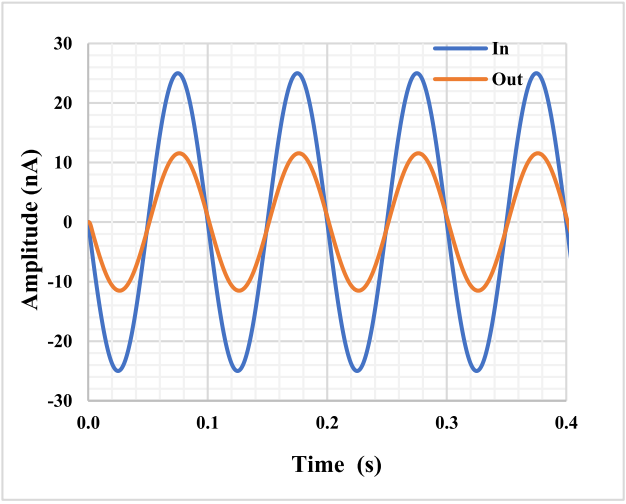


FIGURE 15. Transient analysis of the proposed filter.

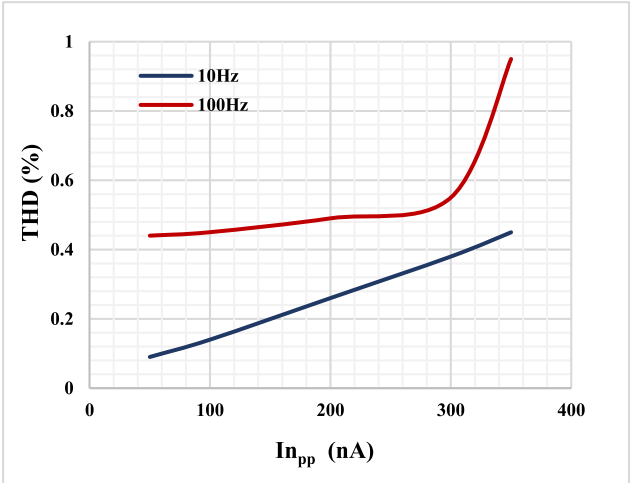


FIGURE 16. THD versus In_{pp}.

IV. CONCLUSION

This paper presents a third order low pass filter based on low-voltage low-power VCII. The VCII is capable to work with supply voltage of 0.5V while offering a wide input voltage range thanks to using the bulk-driven MOST technique operating in the subthreshold region. The filter can be operated as both current-mode and transimpedance-mode filters. The filter consumes 2.73 μW and the THD is below 1 % for input signal below 350 nA_{pp} @ 10Hz. Intensive postlayout simulation including MC and corner analysis confirm the performance of the filter.

REFERENCES

[1] G. W. Roberts and A. S. Sedra, "All current-mode frequency selective circuits," *Electron. Lett.*, vol. 25, no. 12, pp. 759–761, Jun. 1989, doi: 10.1049/el:19890513.
[2] W. Tangsrirat, W. Surakampontorn, and N. Fujii, "Realization of leapfrog filters using current differential buffered amplifiers," *IEICE Trans. Fundamentals Electron., Commun. Comput. Sci.*, vol. E86-A, pp. 318–326, Feb. 2003.
[3] G. Souliotis and C. Psychalinos, "Current-mode linear transformation filters using current mirrors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 6, pp. 541–545, Jun. 2008, doi: 10.1109/TCSII.2007.914909.
[4] A. Uygur and H. Kuntman, "Seventh-order elliptic video filter with 0.1 dB pass band ripple employing CMOS CDTAs," *AEU-Int. J. Electron. Commun.*, vol. 61, no. 5, pp. 320–328, May 2007, doi: 10.1016/j.aeue.2006.06.002.
[5] Y. Li, "A modified CDTA (MCDTA) and its applications: Designing current-mode sixth-order elliptic band-pass filter," *Circuits, Syst., Signal Process.*, vol. 30, no. 6, pp. 1383–1390, Dec. 2011, doi: 10.1007/s00034-011-9329-2.
[6] C. Toumazou, F. J. Lidgey, and D. G. Haigh, *Analogue IC Design: The Current-Mode Approach*. London, U.K.: Peter Peregrinus, 1990.
[7] J. G. Webster, *Medical Instrumentation: Application and Design*, 4th ed. Hoboken, NJ, USA: Wiley, 2010, pp. 11–12.
[8] T. Dostál and J. Pošpíil, "Hybrid models of 3-port immittance convertors and current and voltage conveyors," *Electron. Lett.*, vol. 18, no. 20, pp. 887–888, 1982, doi: 10.1049/el:19820601.
[9] I. M. Filanovsky, "Current conveyor, voltage conveyor, gyrator," in *Proc. 44th IEEE Midwest Symp. Circuits Systems. MWSCAS*, Dayton, OH, USA, Aug. 2001, pp. 314–317, doi: 10.1109/MWSCAS.2001.986176.
[10] I. M. Filanovsky and K. A. Stromsmoe, "Current-voltage conveyor," *Electron. Lett.*, vol. 17, no. 3, pp. 129–130, Feb. 1981, doi: 10.1049/el:19810092.
[11] L. Safari, G. Barile, V. Stornelli, and G. Ferri, "An overview on the second generation voltage conveyor: Features, design and applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 4, pp. 547–551, Apr. 2019, doi: 10.1109/TCSII.2018.2868744.
[12] G. Barile, V. Stornelli, G. Ferri, L. Safari, and E. D'Amico, "A new rail-to-rail second generation voltage conveyor," *Electronics*, vol. 8, no. 11, p. 1292, Nov. 2019, doi: 10.3390/electronics8111292.
[13] G. Barile, G. Ferri, L. Safari, and V. Stornelli, "A new high drive class-AB FVF-based second generation voltage conveyor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 3, pp. 405–409, Mar. 2020, doi: 10.1109/TCSII.2019.2915814.
[14] M. Kumngern, U. Torteanchai, and F. Khateb, "CMOS class AB second generation voltage conveyor," in *Proc. IEEE Int. Circuits Syst. Symp. (ICSyS)*, Kuantan, Malaysia, Sep. 2019, pp. 1–4, doi: 10.1109/ICSyS47076.2019.8982420.
[15] L. Safari, E. Yuce, S. Minaei, G. Ferri, and V. Stornelli, "A second-generation voltage conveyor (VCII)–based simulated grounded inductor," *Int. J. Circuit Theory Appl.*, vol. 48, no. 7, pp. 1180–1193, Jul. 2020, doi: 10.1002/cta.2770.
[16] A. Yesil and S. Minaei, "New simple transistor realizations of second-generation voltage conveyor," *Int. J. Circuit Theory Appl.*, vol. 48, no. 11, pp. 2023–2038, Nov. 2020, doi: 10.1002/cta.2879.
[17] V. Stornelli, L. Safari, G. Barile, and G. Ferri, "A new extremely low power temperature insensitive electronically tunable VCII-based grounded capacitance multiplier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 1, pp. 72–76, Jan. 2021, doi: 10.1109/TCSII.2020.3005524.
[18] A. Yesil, S. Minaei, and C. Psychalinos, "±0.45 V CMOS second-generation voltage conveyor based on super source follower," *Circuits, Syst., Signal Process.*, Oct. 2021, doi: 10.1007/s00034-021-01867-7.

[19] L. Safari, G. Barile, G. Ferri, and V. Stornelli, "High performance voltage output filter realizations using second generation voltage conveyor," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 28, no. 9, Nov. 2018, doi: 10.1002/mmce.21534.
[20] L. Safari, G. Barile, G. Ferri, and V. Stornelli, "A new low-voltage low-power dual-mode VCII-based SIMO universal filter," *Electronics*, vol. 8, no. 7, p. 765, Jul. 2019, doi: 10.3390/electronics8070765.
[21] P. Rani and R. Pandey, "Voltage conveyor based electronically tunable multifunction biquadractic filter," in *Proc. 7th Int. Conf. Signal Process. Integr. Netw. (SPIN)*, Noida, India, Feb. 2020, pp. 1110–1113, doi: 10.1109/SPIN48934.2020.9071041.
[22] E. Yuce, L. Safari, S. Minaei, G. Ferri, and V. Stornelli, "New mixed-mode second-generation voltage conveyor based first-order all-pass filter," *IET Circuits, Devices Syst.*, vol. 14, no. 6, pp. 901–907, Sep. 2020, doi: 10.1049/iet-cds.2019.0469.
[23] G. Barile, L. Safari, G. Ferri, and V. Stornelli, "A VCII-based stray insensitive analog interface for differential capacitance sensors," *Sensors*, vol. 19, no. 16, p. 3545, Aug. 2019, doi: 10.3390/s19163545.
[24] L. Safari, G. Barile, V. Stornelli, and G. Ferri, "A new versatile full wave rectifier using voltage conveyors," *AEU-Int. J. Electron. Commun.*, vol. 122, Jul. 2020, Art. no. 153267, doi: 10.1016/j.aeue.2020.153267.
[25] T. Kulej and F. Khateb, "Sub 0.5-V bulk-driven winner take all circuit based on a new voltage follower," *Analog Integr. Circuits Signal Process.*, vol. 90, no. 3, pp. 687–691, 2017, doi: 10.1007/s10470-016-0898-7.
[26] F. Khateb, T. Kulej, and M. Kumngern, "0.3 V bulk-driven current conveyor," *IEEE Access*, vol. 7, pp. 65122–65128, 2019, doi: 10.1109/ACCESS.2019.2916897.

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