

Article

# 0.5 V, nW-Range Universal Filter Based on Multiple-Input Transconductor for Biosignals Processing

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**Abstract:** This paper demonstrates the advantages of the multiple-input transconductor (MI- $G_m$ ) in filter application, in terms of topology simplification, increasing filter functions, and minimizing the count of needed active blocks and their consumed power. Further, the filter enjoys high input impedance, uses three MI- $G_m$ s and two grounded capacitors, and it offers both inverting and non-inverting versions of low-pass (LPF), high-pass (HPF), band-pass (BPF), band-stop (BS) and all-pass (AP) functions. The filter operates under a supply voltage of 0.5 V and consumes 37 nW, hence it is suitable for extremely low-voltage low-power applications like biosignals processing. The circuit was designed in a Cadence environment using 180 nm CMOS technology from Taiwan Semiconductor Manufacturing Company (TSMC). The post-layout simulation results, including Monte Carlo and process, voltage, temperature (PVT) corners for the proposed filter correlate well with the theoretical results that confirm attractive features of the developed filter based on MI- $G_m$ .

**Keywords:** OTA; multiple-input MOS transistor; low-voltage low-power; universal filter; biosignals processing



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## 1. Introduction

The innovations in circuit design techniques for low-voltage supply and low-power consumption for portable electronics, energy harvesting, biomedical monitoring, and autonomous sensor applications are vital [1–4]. For biosignal processing electronics, where the bio-signals spectrum lies between sub-hertz up to 10 kHz, the extremely low-voltage supply and low-power consumption of such electronics are rather beneficial since it prolongs the operating lifetime of these applications. Figure 1 shows a conceptual diagram of biosignals processing, where the biosignals with very low amplitude (in the range from  $\mu\text{V}$  up to mV) are sensed by actuators/sensors. Then, the sensed signals are amplified by a low-noise amplifier (preamplifier), and the unwanted noise is removed by a suitable analog filter, which is the target of this paper. Next, the digital signal processing includes an analog-to-digital converter (ADC) and a central processing unit (CPU). The resulting data are displayed or wirelessly transmitted.

The operational transconductance amplifier (OTA), also known as the transconductor ( $G_m$  stage), is a basic block for electronic applications like filters and oscillators [5–10]. Unlike the standard and well-known single-input OTA, the multiple-input OTA/transconductor (MI-OTA/MI- $G_m$ ) offers increased arithmetic operation at the input that results in a reduced number of active elements, power consumption, and simplification of the filter

topology. It is worth noting that for designers in CMOS, it is a challenge to design a circuit operating with supply voltage  $V_{DD}$  around or even below the threshold voltage  $V_{TH}$  of the MOS transistor without sacrificing the performance of the circuit. The use of multiple-input transconductors to reduce the number of components in the design of OTA-C filters was confirmed in the literature [5,6]. It was shown that the multiple-input OTA can reduce the number of components, silicon area, and power dissipation by approximately factor  $k$ , where  $k$  is the number of OTA inputs [5]. Multiple-input transconductor can be obtained by the following techniques: 1. using extra differential pairs [5,6], or 2. using a multiple-input floating-gate transistor (MIFG) [7–10]. While the first technique increases the count of transistors, current branches, and the complexity of the design, the second technique suffers from the high-voltage offset, incapability of processing DC signals, and becomes unsuitable for modern deep-nanoscale CMOS technology with gate leakage [11]. A promising technique that offers multiple-input OTA without the above-mentioned limitations is the multiple-input MOS transistor (MI-MOS), firstly presented and experimentally confirmed in [12–14]. The multiple-input MOS transistor is shown in Figure 2. The multiple-input terminals  $V_1, V_2$ , etc. can be obtained from: a. the gate while the bulk is biased by voltage  $V_{BB}$ , b. from the bulk while the gate is biased by  $V_{BG}$ , c. from the bulk-gate (known as dynamic threshold MOS transistor “DTMOS”) without biasing or d. from the bulk-gate (known as quasi-floating-gate “QFG”) with different biasing voltages  $V_{BB}$  and  $V_{BG}$  for bulk and gate, respectively [15].

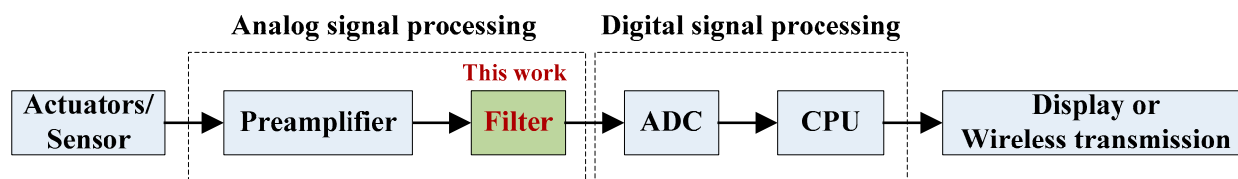


Figure 1. The conceptual diagram for processing biosignals.

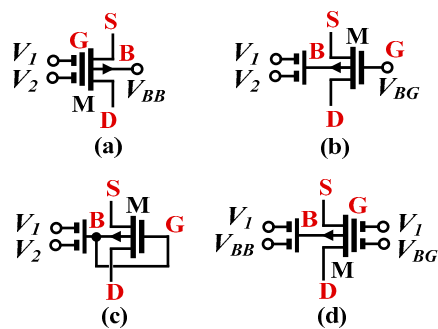


Figure 2. Symbol of the multiple-input MOS transistor: gate (a), bulk (b), DTMOS (c) and QFG (d).

The realization of the multiple-input with bulk-driven MOS device is shown in Figure 3. The multiple-input is constructed by a capacitive summing circuit using capacitors  $C_i$  ( $i = 1, \dots, N$ ) connected to the bulk terminal of a MOS transistor. To provide proper biasing of the bulk terminal for DC operation, the high resistance resistors  $R_{MOS}$  is used. These  $R_{MOS}$  are realized as the anti-parallel connection of two minimum-size transistors  $M_L$ , operating with  $V_{GS} = 0$ . For AC signals, and for frequencies  $f \gg 1/2\pi C_i R_{MOSi}$ ,  $i = 1 \dots N$ , resistors  $R_{MOS}$  are shunted by capacitances  $C_i$ , which create an analog voltage divider/voltage summing circuit, with the gain coefficients determined solely by the ratio of capacitances [15].

In this work, the multiple-input bulk-driven MOS transistor is implemented using a CMOS structure of the  $G_m$  to build a multiple-input voltage-mode analog filter. As a result, the number of used active devices is reduced while offering more filtering responses compared to conventional  $G_m$ -based filters.

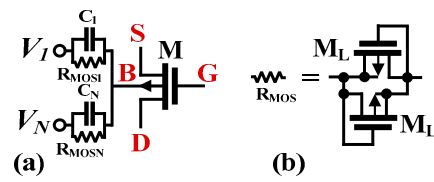


Figure 3. MI-BD MOS transistor (a), and realization of  $R_{MOS}$  (b).

## 2. Methods

In this section, the design of the multiple-input  $G_m$  and the universal filter based on it will be described.

### 2.1. The Multiple-Input $G_m$

The symbol and CMOS structure of the MI- $G_m$  stage are shown in Figure 4a,b, respectively. In an ideal case, the transfer characteristic of the MI- $G_m$  stage of Figure 4a can be expressed by:

$$I_{out} = G_m(V_{+1} + V_{+2} - V_{-1} - V_{-2}), \quad (1)$$

where  $G_m$  is the transconductance gain,  $V_{+1}$  and  $V_{+2}$  are signals at the non-inverting inputs,  $V_{-1}$ ,  $V_{-2}$  are signals at the inverting inputs, and  $I_{out}$  is the output current.

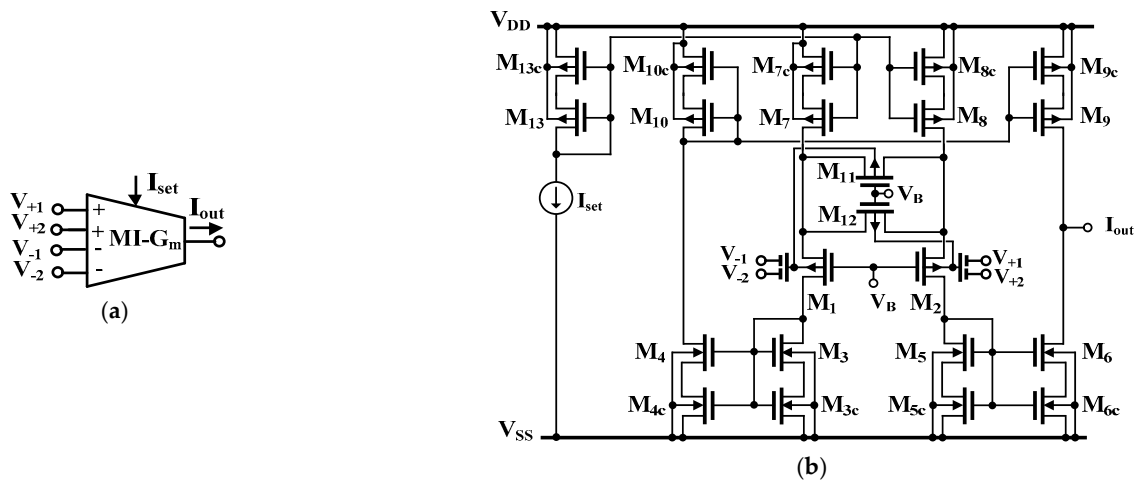


Figure 4. The symbol of the multiple-input  $G_m$  stage (a) and its CMOS structure (b).

The particular realization of the MI- $G_m$  stage discussed here was first presented and experimentally verified in [15]. The circuit employs the MI-bulk-driven differential pair  $M_1$ ,  $M_2$ , with the source-degenerative bulk-driven transistors  $M_{11}$ ,  $M_{12}$ , which operate in the triode region and improve the circuit linearity. Note, that  $V_{GS}$  as well as  $V_{BS}$  voltages for  $M_{11}$ ,  $M_{12}$  and  $M_1$ ,  $M_2$  are identical for any common-mode input voltage and biasing current. The single-input gate-driven counterpart of the input stage was first proposed in [16], and its weak-inversion version was discussed in [17]. Here, due to the use of bulk-driven transistors, and an additional capacitive voltage divider, both, the input linear range, as well as the input common-mode range are significantly increased, as compared with the conventional gate-driven (GD) version operating in a weak-inversion region. Moreover, the application of MI transistors allows realizing MI- $G_m$ s without multiplying the input differential pair, as in classical solutions, which saves power and simplifies the overall structure of such circuits.

Regarding the rest of the structure, the circuit can be seen as a classical current-mirror OTA, where all current mirrors are realized with the use of self-cascode transistors. This improves their output resistances, and consequently, also the DC voltage gain of the proposed OTA, with negligible limitation of the output voltage swing. Note, that the current gain of all current mirrors in this design was assumed to be equal to unity.

Assuming that a p-MOS transistor is operating in a weak-inversion region, the drain current can be described by the following equation, [18]:

$$I_D = I_T \left( \frac{W}{L} \right) \exp \left( \frac{V_{SG} + V_{TH}}{n_p U_T} \right) \left[ 1 - \exp \left( - \frac{V_{SD}}{U_T} \right) \right] \quad (2)$$

where  $I_T$  is the technology current,  $W$  and  $L$  are the transistor channel width and length, respectively,  $n_p$  is the subthreshold slope factor,  $U_T$  is the thermal potential and  $V_{TH}$  is the threshold voltage, which can be linearly approximated as:

$$V_{TH} = V_{TO} - (n_p - 1) V_{BS} \quad (3)$$

where  $V_{TO}$  is the threshold voltage for  $V_{BS} = 0$ .

Assuming that the circuit is controlled with  $i$ -th differential input, with other inputs grounded for AC signals, the low-frequency large-signal transfer characteristic of the  $G_m$  can be expressed as:

$$I_{out} = 2I_{set} \tanh \left( \beta_i \eta \frac{V_{+i} - V_{-i}}{2n_p U_T} - \tanh^{-1} \left[ \frac{1}{4m + 1} \tanh \left( \beta_i \eta \frac{V_{+i} - V_{-i}}{2n_p U_T} \right) \right] \right) \quad (4)$$

where  $\eta = (n_p - 1) = g_{mb1,2} / g_{m1,2}$  at the operating point,  $m = (W_{11} / L_{12})(W_1 / L_1)$  is the relative aspect ratio of the two matched transistor pairs  $M_{11}$ - $M_{12}$  and  $M_1$ - $M_2$ .  $\beta_i$  is the voltage gain of the input capacitive divider from one input, which neglects the second order effects and for  $f \gg 1 / C_i R_{MOSi}$  can be approximated as:

$$\beta_i \cong \frac{C_i}{\sum_{i=1}^n C_i} \quad (5)$$

where  $n$  is the total number of differential inputs (in the discussed design  $n = 2$ ).

For optimum linearity, the coefficient  $m$  should be equal to 0.5, as for the GD counterpart, of the discussed circuit. This value does not depend on the biasing voltage  $I_{set}$  [17].

As it can be concluded from (4), as compared to its single-input GD counterpart, the linear range of the proposed circuit is extended by a factor of  $1/\beta_i \eta$ , which for the discussed case ( $\beta_i = 0.5$ ,  $\eta = 0.34$ ) means that the linear range is extended around 6 times.

The small-signal transconductance of the  $G_m$  can be calculated from (4) as:

$$G_m = \beta_i \eta \cdot \frac{4m}{4m + 1} \cdot \frac{I_{set}}{n_p U_T} \quad (6)$$

thus, the small-signal transconductance is equal to the gate transconductance of the input transistors  $M_1$  and  $M_2$ , multiplied by a factor of  $[4m/(4m + 1)] \beta_i \eta$ , which for the proposed design in the optimal case ( $m = 0.5$ ) is equal to around 1/9.

The low-frequency voltage gain of the  $G_m$  can be approximated as:

$$A_{VO} \cong G_m [(g_{m9} r_{dsD9} r_{ds9c}) || (g_{m6} r_{ds6} r_{ds6c})] \quad (7)$$

Its value is negatively affected by the low transconductance of the MI- $G_m$ . On the other hand, however, self-cascode connections allow for enlarging the output resistance of the MI- $G_m$ , thus improving its voltage gain and at least partially compensating the losses caused by the input capacitive divider and the small bulk transconductance of MOS transistors.

Assuming that the noise current of an  $i$ -th MOS transistor in a weak inversion region can be expressed as:

$$\overline{I_{ni}^2} = 2q I_{Di} + \frac{1}{f C_{OX}} \left( \frac{K g_{mi}^2}{W_i L_i} \right) \quad (8)$$

where  $q$  is the electron charge,  $C_{OX}$  is the oxide capacitance per unit area and  $K$  is the flicker noise constant, the input-referred noise of the MI- $G_m$ , referred to as one of the differential inputs, is given by:

$$\overline{v_n^2} = \frac{1}{G_m^2} \left[ 2\overline{I_{n1,2}^2} \left( \frac{2G}{g_{m1,2} + 2G} \right)^2 + 2\overline{I_{n7,8SC}^2} \left( \frac{g_{m1,2}}{g_{m1,2} + 2G} \right)^2 + \overline{I_{nG}^2} \left( 2\frac{g_{m1,2}}{g_{m1,2} + 2G} \right)^2 + 4\overline{I_{n3-6SC}^2} + 2\overline{I_{n9,10SC}^2} \right] \quad (9)$$

where  $G = 1/(r_{ds11} || r_{ds12})$  at the operating point.

As it can be concluded from (9), the input-referred noise of the MI- $G_m$  is increased, as compared to its single-input GD counterpart, due to the lower transconductance  $G_m$ . However, the input noise is increased in the same proportion as the input linear range, therefore, the dynamic range will not be affected and remains the same in both realizations.

## 2.2. Universal Filter Design

The voltage-mode analog filter is a commonly used analog signal processing block, that is well-known for a long time. This is due to the versatility of operational amplifiers that are commonly used in the synthesis of analog electronic circuits [19]. Over the last decades, some other active elements such as operational transconductance amplifiers (OTAs), second-generation current conveyors (CCII), and current feedback operational amplifiers (CFOAs) have received considerable attention for designing voltage- and current-mode analog filters [20–28]. To design voltage-mode filters, multiple-input type filters can reduce the number of active devices compared with single-input type filters, because variant filtering responses can be obtained by appropriately applying the input signal, depending on the conditions of the required filtering responses. To avoid loading effects, the input terminals of the voltage-mode filter must have high impedance. To avoid additional circuits such as inverting amplifiers, the minus-type input signal of voltage-mode filters must be available.

For the purpose of illustration, Figure 5a shows a universal filter design using five standard  $G_m$  blocks, and two grounded capacitors and it offers five standard filtering functions [26]. In this work, a multiple-input voltage-mode analog filter using multiple-input transconductors MI- $G_m$  is proposed as shown in Figure 5b. The structure will show that the multiple-input  $G_m$ -based filter can reduce the number of used active devices and can offer more filtering responses compared with conventional  $G_m$ -based filters. The filter employs three multiple-input  $G_m$  stages and two grounded capacitors, which is desirable in integrated solutions. Thanks to the MI- $G_m$  elements that offer noninverting/inverting multiple-input terminals, noninverting/inverting transfer functions of five types of filtering responses, namely, low-pass, high-pass, band-pass, band-stop, and all-pass can be easily obtained. Moreover, the input signals are connected to the high-impedance inputs of MI- $G_m$ , hence the additional buffer circuits to avoid the loading effects are not required. It is worth noting that although both filters in Figure 5a,b offer the five standard filtering functions, the count of active elements is reduced from 5 to 3 thanks to the MI- $G_m$ . This results in power consumption reduction and filter topology simplification, and in offering more transfer functions (including both non-inverting and inverting versions of five standard filtering functions).

Using (1) and nodal analysis, the output voltages of Figure 5b are given by

$$V_{o1} = \frac{(sC_2G_{m1} + G_{m1}G_{m2})(V_{in1} - V_{in2}) + G_{m1}G_{m2}(V_{in4} - V_{in3} + V_{in5} - V_{in6})}{s^2C_1C_2 + sC_1G_{m2} + G_{m1}G_{m2}} \quad (10)$$

$$V_{o2} = \frac{G_{m1}G_{m2}(V_{in1} - V_{in2}) + C_1G_{m2}(V_{in3} - V_{in4} + V_{in6} - V_{in5})}{s^2C_1C_2 + sC_1G_{m2} + G_{m1}G_{m2}} \quad (11)$$

$$V_{o3} = \frac{G_{m1}G_{m2}(V_{in1} - V_{in2}) + C_1G_{m2}(V_{in3} - V_{in4}) + (s^2C_2C_2 + G_{m1}G_{m2})(V_{in5} - V_{in6})}{s^2C_1C_2 + sC_1G_{m2} + G_{m1}G_{m2}} \quad (12)$$

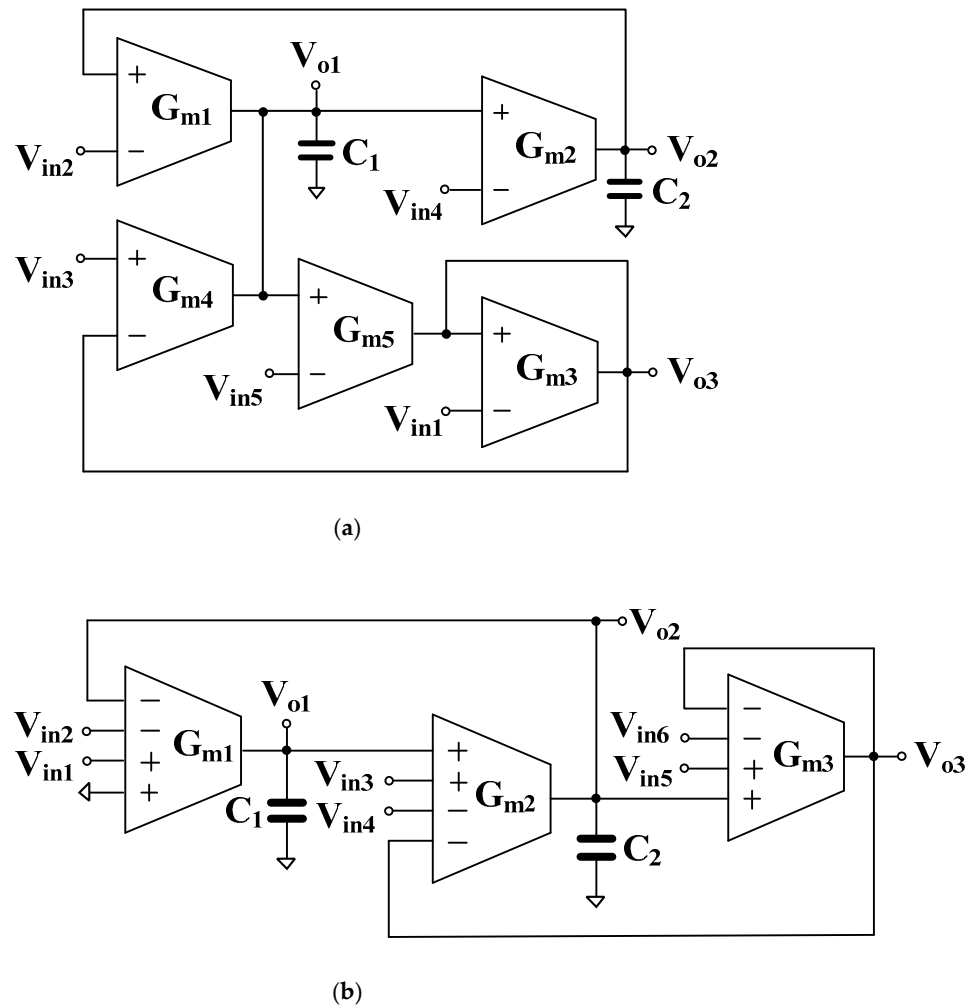


Figure 5. Proposed universal filter using standard  $G_m$  [26] (a), and MI- $G_m$  (b).

The conditions for obtaining variant filtering responses by the appropriate connection of input signals are shown in Table 1.

Table 1. Variant filtering functions of the universal filter.

	Filtering Function	Input	Output
LP	Non-inverting	$V_{in4} V_{in5} V_{in1} V_{in1}$	$V_{o1} V_{o1} V_{o2} V_{o3}$
	Inverting	$V_{in3} V_{in6} V_{in1} V_{in2}$	$V_{o1} V_{o1} V_{o2} V_{o3}$
BP	Non-inverting	$V_{in1}$ and $V_{in6}$	$V_{o1} V_{o2} V_{o2} V_{o3}$
	Inverting	$V_{in3} V_{in6} V_{in3}$ $V_{in2}$ and $V_{in5}$ $V_{in4} V_{in5} V_{in4}$	$V_{o1} V_{o2} V_{o2} V_{o3}$
HP	Non-inverting	$V_{in5}$ and $V_{in2}$	$V_{o3}$
	Inverting	$V_{in6}$ and $V_{in1}$	$V_{o2}$
BS	Non-inverting	$V_{in5}$	$V_{o3}$
	Inverting	$V_{in6}$	$V_{o3}$
AP	Non-inverting	$V_{in5}$ and $V_{in4}$	$V_{o3}$
	Inverting	$V_{in5}$ and $V_{in3}$	$V_{o3}$

Note: the unused inputs should be grounded.

The natural frequency ( $\omega_o$ ) and the quality factor ( $Q$ ) are given by:

$$\omega_o = \sqrt{\frac{G_{m1} G_{m2}}{C_1 C_2}} \tag{13}$$

$$Q = \sqrt{\frac{C_2 G_{m1}}{C_1 G_{m2}}} \tag{14}$$

It is apparent that the parameter  $\omega_o$  can be controlled electronically by  $G_{m1} = G_{m2}$  while the parameter  $Q$  is controllable orthogonally by the ratio of  $C_2/C_1$ .

Taking into account the non-idealities of MI- $G_m$ , there are three major non-idealities that should be considered [29]: (i) the frequency-dependent transconductance, (ii) the input parasitic resistances and capacitances, (iii) the output parasitic resistances and capacitances.

Figure 6 shows the non-ideal model with parasitic elements of the MI- $G_m$ , where  $R_+$ ,  $R_-$ ,  $C_+$ ,  $C_-$  are the input parasitic resistances and capacitances, and  $R_o$ ,  $C_o$  is the output parasitic resistance and capacitance, respectively. Considering Figure 5b the parasitic resistances at nodes  $V_{o1}$  and  $V_{o2}$  are, respectively,  $R_{o1}/R_{+1}$  and  $R_{o2}/R_{+3}$ , thus the value of these parallel resistances is very high and can be neglected. Consider the parasitic capacitances at nodes  $V_{o1}$  and  $V_{o2}$ , they can be expressed respectively as  $C'_1 = C_1 + C_{o1} + C_{+2}$  and  $C'_2 = C_2 + C_{o2} + C_{-1} + C_{+3}$ .

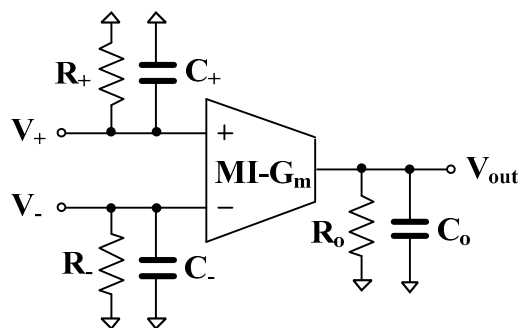


Figure 6. Non-ideal MI- $G_m$  model with parasitic elements.

Considering the non-ideality of transconductance, the output current can be rewritten as

$$I_{out} = G_{mnj}(V_{+1} + V_{+2} - V_{-1} - V_{-2}), \tag{15}$$

where  $G_{mnj}$  is the non-ideal transconductance gain of the  $j$ -th MI- $G_m$  that is frequency-dependent, and can be approximately given by [29,30]:

$$G_{mnj}(s) \cong G_{mj}(1 - T_j s) \tag{16}$$

From Figure 5 and (16), denominators of (10)–(12) can be expressed by:

$$s^2 C'_1 C'_2 \left( 1 - \frac{C_1 G_{m2} T_2 - G_{m1} G_{m2} T_1 T_2}{C_1 C_2} \right) + s C'_1 G_{m2} \left( 1 - \frac{G_{m1} G_{m2} T_1 + G_{m1} G_{m2} T_2}{C'_1 G_{m2}} \right) + G_{m1} G_{m2} \tag{17}$$

The non-idealities of the transconductance  $G_{mnj}$  can be neglected, if the following condition is satisfied:

$$\frac{C'_1 G_{m2} T_2 - G_{m1} G_{m2} T_1 T_2}{C'_1 C'_2} \ll 1 \tag{18}$$

$$\frac{G_{m1} G_{m2} T_1 + G_{m1} G_{m2} T_2}{C'_1 G_{m2}} \ll 1 \tag{19}$$

In such a case, the parameters  $\omega_o$  and  $Q$  become as follows:

$$\omega_o = \sqrt{\frac{G_{m1} G_{m2}}{C'_1 C'_2}} \tag{20}$$

$$Q = \sqrt{\frac{C'_2 G_{m1}}{C'_1 G_{m2}}} \tag{21}$$



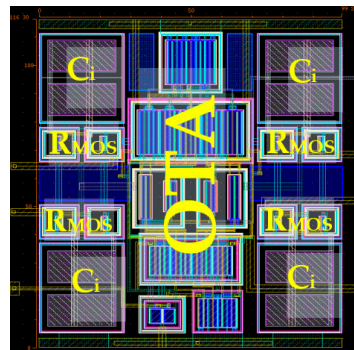
The parasitic capacitances will decrease the value of  $\omega_0$  as compared to the ideal case.

### 3. Results and Discussion

The filter circuit was designed in a Cadence environment using 180 nm TSMC CMOS technology. The voltage supply was 0.5 V, and the power consumption of the filter was 37 nW. The MI- $G_m$  stage first presented in [15] was used. The transistor aspect ratios  $W/L$  are presented in Table 2. The input metal-insulator-metal (MIM) capacitor  $C_i$  with a capacitance value of 0.5 pF was used. The layout of the MI- $G_m$  is shown in Figure 7, with a silicon area of  $116.3 \mu\text{m} \times 99.2 \mu\text{m}$ .

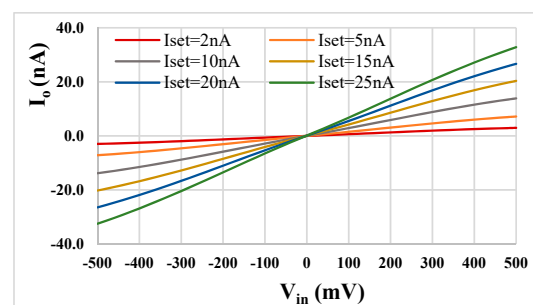
**Table 2.** Transistor Aspect Ratio of the  $G_m$ .

Device Name	W/L ( $\mu\text{m}/\mu\text{m}$ )
$M_1, M_2, M_7-M_{10}, M_{13}$	$2 \times 15/1$
$M_3-M_6$	$2 \times 10/1$
$M_{3c}-M_{6c}$	10/1
$M_{7c}-M_{10c}, M_{13c}, M_{11}, M_{12}$	15/1
$M_L$	5/4



**Figure 7.** The layout of the MI- $G_m$ .

The DC transfer characteristics of the used MI- $G_m$  for  $I_{set} = [2, 5, 10, 15, 20, 25]$  nA are shown in Figure 8. The enhanced linearity in the  $V_{in}$  range of  $\pm 500$  mV is clearly observable.



**Figure 8.** DC transfer characteristic of the MI- $G_m$ .

For the filter application, the simulated frequency responses of the proposed filter are shown in Figure 9. The values of  $C_1 = C_2 = 15$  pF and the setting current  $I_{set} = 5$  nA. The simulated cut-off frequency value of 153 Hz is very close to the calculated value of 154.9 Hz. The power consumption of the filter was 37 nW.



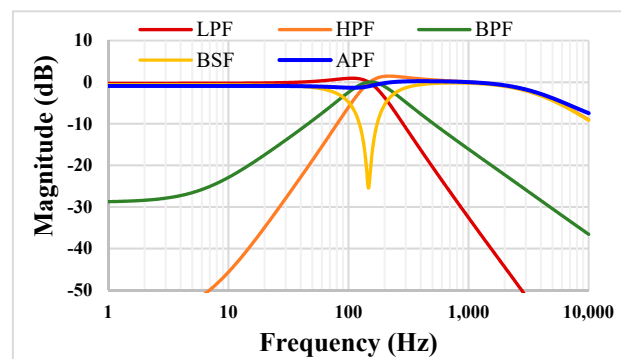


Figure 9. The simulated frequency responses of the proposed filter.

Figure 10 shows the tuning capability of the LPF (a), HPF (b), BPF (c), and BSF (d) with  $C_1 = C_2 = 15$  pF. The setting current was  $I_{set} = 2$  nA, 5 nA, 10 nA, and 20 nA and the cut-off frequency values were 62.3 Hz, 153 Hz, 301.9 Hz, and 595.6 Hz, respectively. Results shown in Figure 10 confirm the wide tuning capability of the proposed filter for low-frequency biomedical applications.

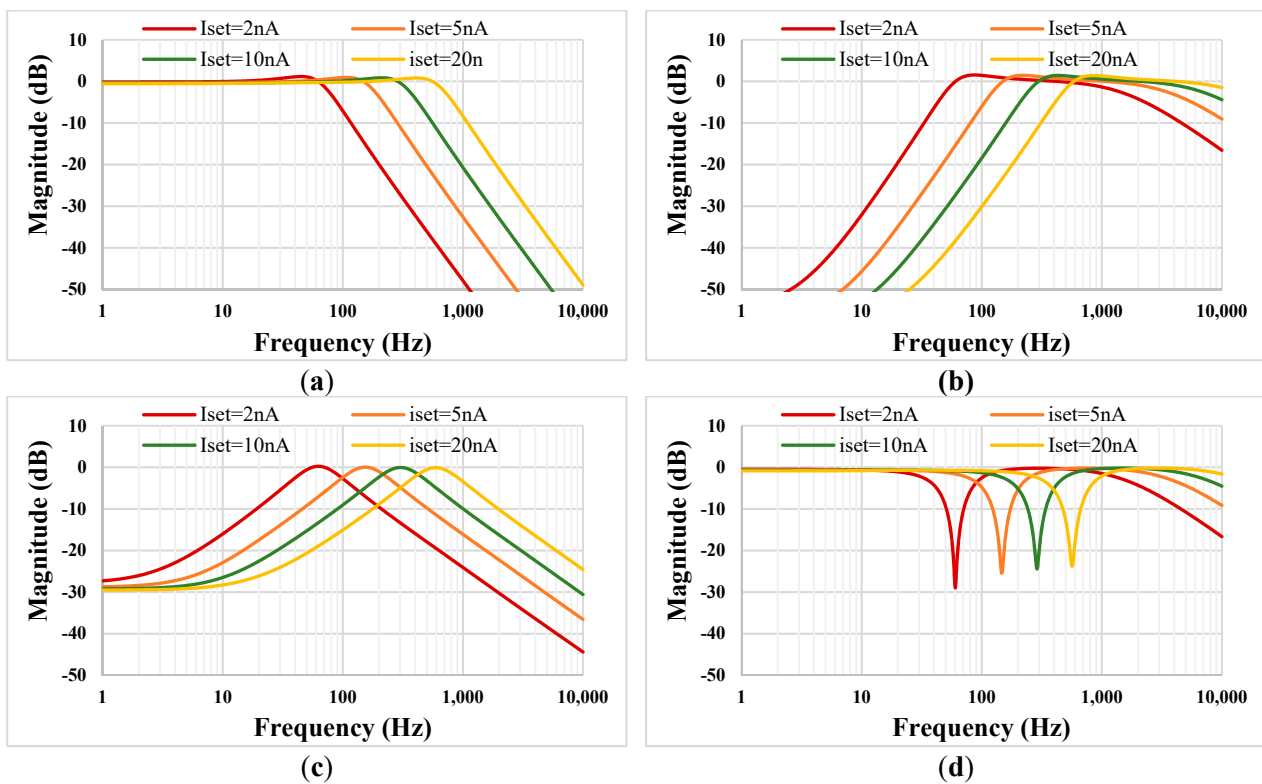


Figure 10. The simulated tuning capability of the proposed LPF (a), HPF (b), BPF (c) and BSF (d).

The Monte Carlo process and mismatch analysis was performed with 200 runs. Figure 11 shows the simulated results for the LPF and BPF. The low-frequency gain at 1 Hz of the LPF was in the range from  $-1.39$  dB to  $0.47$  dB, and the gain of the BPF at a frequency of 153 Hz was in the range from  $-0.438$  dB to  $0.168$  dB.

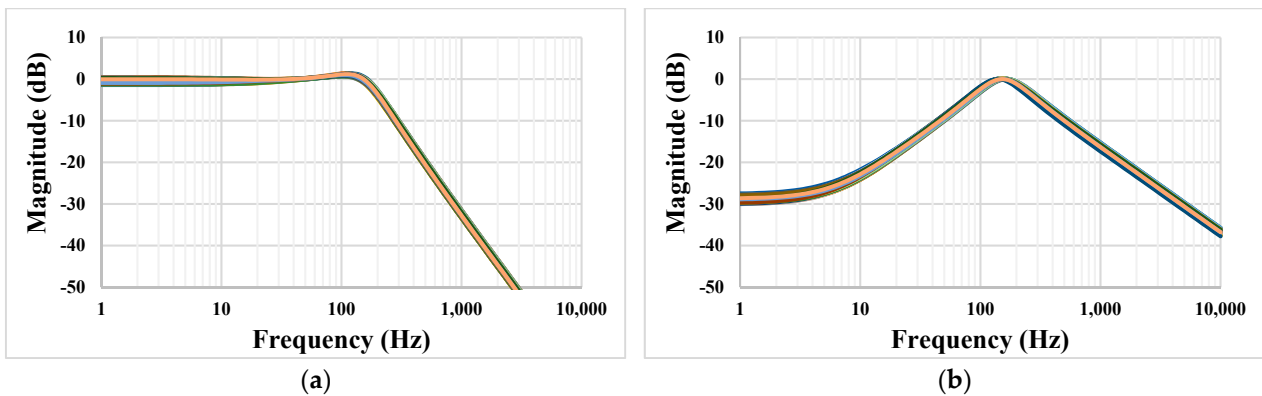


Figure 11. The Monte Carlo simulation of the LPF (a) and BPF (b).

Figure 12 shows the simulation results of the LPF and BPF with the process, voltage, and temperature variations. The process corners were fast-fast, fast-slow, slow-fast, and slow-slow, the voltage supply corners were in the range of  $V_{DD} \pm 10\%$ , and the temperature corners were  $0^\circ\text{C}$  and  $70^\circ\text{C}$ .

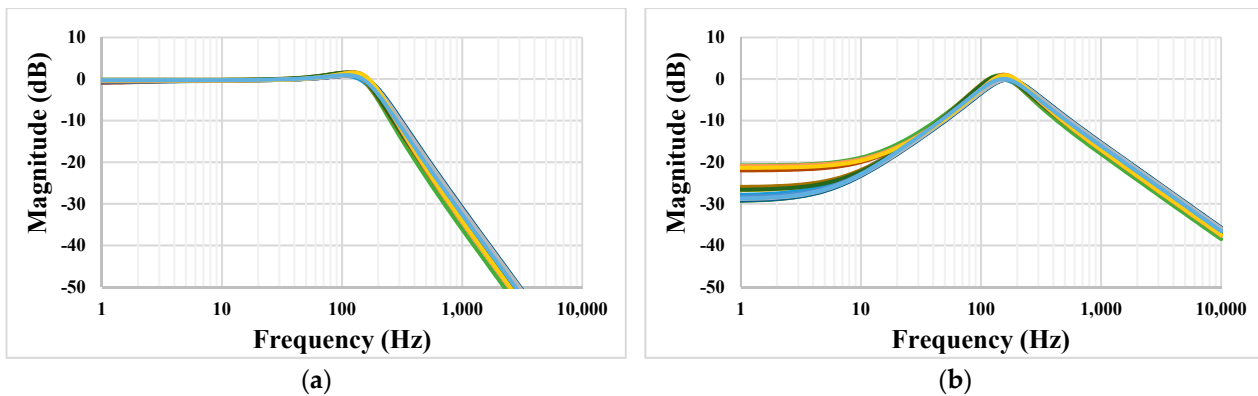


Figure 12. The PVT simulation of the LPF (a) and BPF (b).

Figure 13 shows the transient response of the LPF with an applied input signal of  $100\text{mV}_{pp}$  @  $50\text{Hz}$  and its output spectrum. The total harmonic distortion (THD) of 0.33% was achieved, which was kept still below 1% for the input signal of  $200\text{mV}_{pp}$  @  $50\text{Hz}$ . The output integrated noise of the LPF was  $220\ \mu\text{V}_{rms}$  which resulted in a 50 dB dynamic range ( $DR = 20 \times \log(V_{rms-max}/V_{rms-noise})$ ) of the filter with 1% THD.

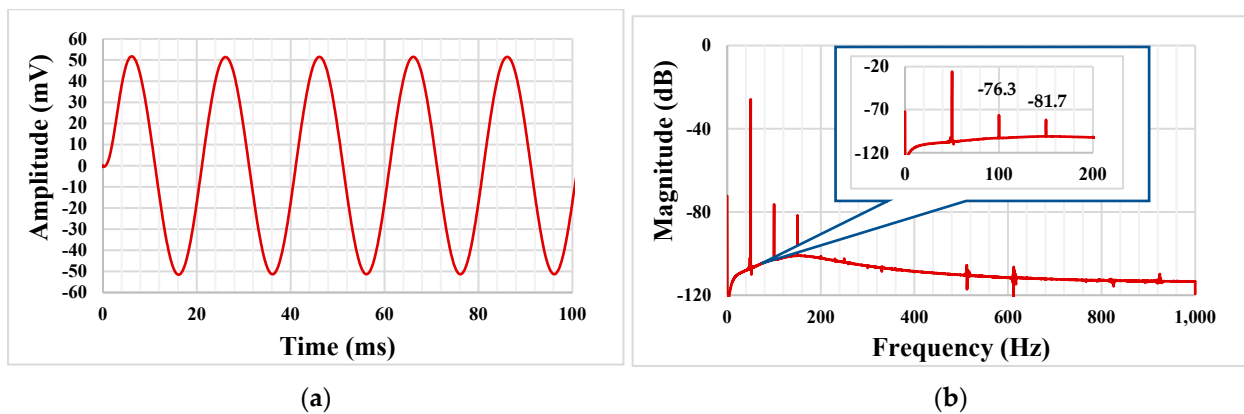


Figure 13. The transient response of the LPF (a) and its spectrum (b).

Table 3 shows a comparison of the proposed filter with the others [26–28]. It is evident that the proposed filter offers the largest amount of filtering functions with a minimum count of active elements, and the lowest voltage supply, and is the only one with nanowatt consumption. All these facts confirm the usability of the multiple-input  $G_m$  stage in filter applications mainly by means of reducing the count of active blocks and power consumption. The figure of merit (FoM) is also presented, where a lower FoM implies the better performance of the filter.

**Table 3.** Comparison with other filters.

	This Work	[26]	[27]	[28]
Technology (nm)	180	commercial IC	180	180
$V_{DD}$ (V)	0.5	$\pm 15$	1.2	$\pm 0.3$
Power consumption (nW)	37	$860 \times 10^6$	$0.96 \times 10^6$	5770
DR (dB)	50			53.2
Fter function	22 (VM)	13 (VM)	22 (VM)	20 (MM)
Offer inverting and non-inverting of five standard responses	Yes	No	Yes	No
Natural frequency (kHz)	0.153	217	1	5
Number of active and passive element	3-OTA, 2-C	5-OTA, 2-C	4-OTA, 2-C	8-OTA, 2-C
Total harmonic distortion (%)	0.33@100 mV <sub>pp</sub>	1.93@200 mV <sub>pp</sub>	1.67@600 mV <sub>pp</sub>	<2@200 mV <sub>pp</sub>
$FOM = \frac{P_{diss}}{f_o \times N \times DR}$	$2.41 \times 10^{-12}$	-	78.6	$1.26 \times 10^{-12}$

where  $P_{diss}$  is the power dissipation,  $f_o$  is the center frequency,  $N$  is the order of filter, and  $DR$  is the dynamic range.

#### 4. Conclusions

This paper demonstrates the advantages of the MI- $G_m$  in filter application, in terms of topology simplification, increasing filter functions, and minimizing the count of the needed active blocks and their power consumption. Therefore, the developed circuit is a good candidate for extremely low-power low-voltage applications like biosignals processing. The filter application offers the largest amount of filtering functions with a minimum count of active elements. The post-layout simulations prove the presented advantages of MI- $G_m$ .

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