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RESEARCH ARTICLE

31.3 nW, 0.5 V Bulk-Driven OTA for Biosignal Processing

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ABSTRACT This paper presents a new extremely low-voltage low-power bulk-driven (BD) operational transconductance amplifier (OTA) realized for low frequency biosignal processing. The CMOS structure of the OTA utilizes bulk-driven and self-cascode techniques in the subthreshold region, supporting the operation with the supply voltage (V_{DD}) as the threshold voltage (V_{TH}) of a single MOS transistor, i.e., $V_{DD} = V_{TH} = 0.5$ V, while offering nano power consumption (31.3 nW for 15 nA nominal setting current). Using the extremely low-voltage and low-power OTA in biosignal processing enables extending the lifetime of applications that are powered by battery or energy harvesting sources. The OTA has a 54.7 dB low frequency gain, 6.18 kHz gain bandwidth and 75° phase margin at 15 pF load capacitance. The proposed OTA has been used to realize a bandpass filter (BPF) with adjustable gain for electrocardiogram (ECG) signal processing. The higher cutoff frequency of the BPF is adjustable electronically by a setting current and the BPF's gain can be adjusted by capacitors value. The total harmonic distortion (THD) of the BPF is −53.56 dB, the input integrated input-referred voltage noise is 17.9 μV_{rms}, the common mode rejection ratio (CMRR) is 75 dB and the power supply rejection ratio (PSRR) is 87.7 dB. The BPF was designed in the Cadence program using 0.18 μm CMOS technology from TSMC. The simulation results agree with the presented theory.

INDEX TERMS Operational transconductance amplifier (OTA), bulk-driven, band-pass filter, low-voltage, low-power CMOS.

I. INTRODUCTION

Nowadays, systems such as portable, battery-operated, and self-powered electronics require extremely low-voltage operation capability and low-power consumption. In biomedical systems, such as data acquisition systems for electrocardiographic (ECG) signal processing, low-voltage and low-power analog circuits are required at the front-end of the systems. Analog circuits, such as amplifiers and filters, are usually used to realize the front-end. Some examples include the operational amplifier (op-amp), transconductance amplifier (OTA), and the differential difference amplifier (DDA), which is based on complementary metal-oxide-semiconductor (CMOS) technologies. In the analog portion, reducing the voltage supply degrades the analog circuit performances, such as the dynamic range (DR), bandwidth and linearity. To maintain the required DR when the voltage supply is reduced, the input voltage swing should be increased. It is well-known that circuits capable of rail-to-rail input voltage swing are the best solution for maintaining the required DR when the circuits are operated with low-voltage supply. The original technique for implementing the rail-to-rail input voltage swing of circuits is the use of differential pairs that are composed of both PMOS and NMOS transistors [1]. However, this technique is complex due to the additional differential pair, current branches and the circuitry used to maintain constant transconductance over the whole input voltage range. Moreover, this technique is not the most

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suitable for circuits that operate with a low-power supply and low-power consumption. Therefore, non-conventional techniques, such as bulk-driven (BD) [2], floating-gate (FG) [3], quasi-floating gate (QFG) [4], or dynamic threshold voltage (DT) [5], which are suitable for circuits operating with low-supply voltages, have been reported. Using these techniques, the input voltage swing of circuits can be extended due to the threshold voltage that can be reduced or removed from the signal path.

Some low-voltage and low-power analog devices using non-conventional techniques are reported in literature, including the op-amp [6], [7], [8], [9], OTA [10], [11], [12], [13], [14], DDA [15], [16], [17], [18], [20], [39], [40], and second-generation current conveyor (CCII) [19], [20], [21], [22]. Low-voltage and low-power analog circuits can be applied to biosignal processing; analog filters are an example of this application [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38]. In [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], and [38], BPFs suitable for applications in biomedical systems have been proposed. However, some of these BPFs suffer from high-power consumption [28], [29], [30], [31], [32], [35], [36], [37], [38], cannot control voltage gain [30], [31], [32], [33], [34], [35], [37], [38], or cannot control the higher and lower cutoff frequencies [29], [30], [31], [32], [33], [34], [35], [36], [37], [38].

In this work, the bulk-driven technique has been used to realize a new extremely low-voltage low-power OTA (BD-OTA) for low frequency biosignal processing. The OTA can work with a supply voltage of 0.5 V and a power of 31.3 nW for 15 nA nominal setting current. The proposed OTA has been used to realize a bandpass filter (BPF) with adjustable gain for ECG signal processing. The voltage gain and higher cutoff frequency can be controlled.

II. PROPOSED CIRCUIT

A. PROPOSED 0.5 V OTA

The CMOS schematic of the 0.5-V OTA used to realize the BPF proposed in this work is shown in Fig. 1 (a). The structure was first proposed in [41] and verified experimentally in [42]. In both cases, it served as the input stage of a two-stage operational amplifier. Here, the structure is used as a single-stage amplifier, with all transistors replaced by self-composite devices, as shown in Figs 1 (b) and 1 (c).

The OTA shown in Fig. 1 (a) is in fact a single-stage non-tailed differential amplifier. For simplicity, let us first consider the version with transistors M_7 and M_8 removed [43]. In such a case, transistors M_{1A} with M_{2A} and M_{1B} with M_{2B} form two current mirrors. The mirrors are biased with constant current sources based on transistors M_3 and M_4. Note that the input differential signals V_+ and V_- are applied to the bulk terminals of the input transistors. With $V_+ = V_-$, the threshold voltages of M_{1A} and M_{2A} (M_{1B} and M_{2B}) are equal for every level of the input voltage. Therefore, neglecting the impact of drain-source conductances g_{ds}, the current gains of the above-mentioned current mirrors do not depend on the input common-mode signals. Note that in such a case, the drain currents of M_{1A} and M_{1B} are not only equal, but also remain constant and equal to the biasing currents $I_{D3,4}$. This is a significant difference in comparison with pseudo-differential amplifiers, where currents of a differential stage highly depend on the common-mode level. The drain currents of M_{1B} and M_{1A} (I_{D1B} and I_{D1A}) are subtracted thanks to the unity-gain current mirror M_5-M_6; thus, the output current is equal to zero. Note that, neglecting second order effects, variations of V_{DD} do not affect the drain currents of M_{1A} and M_{1B}. Thus, neglecting the impact of second order effects, the output signal of the OTA is insensitive to both the input common-mode level as well as variations of V_{DD}. This results in relatively large values of the common-mode and power supply rejection ratios (CMRR and PSRR, respectively).

When V_+ and V_- are not equal, then the threshold voltages of M_1 and M_2 are different, thus producing a current difference between M_1 and M_2 and consequently a non-zero output current of the whole stage. Note that the value of this current is not limited by a tail current source and can approach significant values, much larger than the biasing currents $I_{D3,4}$. This improves the slew-rate (SR) of the OTA.

By removing the tail current source, which is used for biasing the differential amplifiers in conventional solutions, the minimum V_{DD} can be decreased while still offering good CMRR and PSRR performances. This also increases the output swing of the OTA, which is nearly rail-to-rail. In addition, the input common-mode range of the amplifier is also rail-to-rail, due to the use of bulk-driven input transistors.

By applying a single-stage OTA, a power-effective solution can be achieved as it eliminates the need for a second gain stage that usually consumes more power. However, sufficient voltage gain is problematic. In order to increase the voltage gain, two additional techniques have been applied.

First, the voltage gain is increased by applying partial positive feedback (PPF), introduced by the cross-coupled transistors M_7 and M_8. The transistors generate negative conductances at the drain/gate nodes of M_{2A} and M_{2B}, thus increasing the resulting resistance at these nodes, and consequently increasing the voltage gain from the input terminals to these nodes. Since transistors M_{1A} and M_{1B} are controlled with larger signals at their gates, the overall transconductance and the voltage gain of the OTA is increased. Referring to Fig. 1 (a), the DC voltage gain of the OTA can be expressed as [41]:

$$A_{vo} = \frac{g_m}{g_{ds1} + g_{ds6}} \tag{1}$$

where g_m is the transconductance of the OTA, which in turn can be expressed as:

$$g_m = 2g_{mb1}\frac{1 + p/2}{1 - m + p} \tag{2}$$

where $m = g_{m7,8}/g_{m2}$, $p = (g_{ds2} + g_{ds7,8} + g_{ds3,4})/g_{m2}$, and g_{mb1} is the bulk transconductance of M_1. Note that in a weak inversion region, the ratio of transconductances is equal to

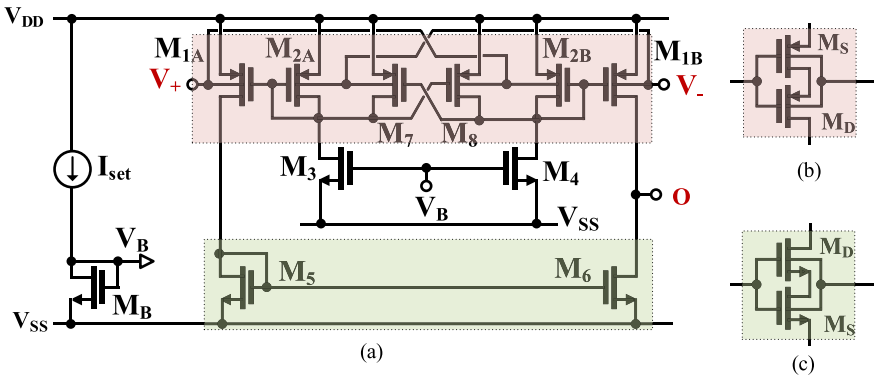

FIGURE 1. (a) 0.5 V bulk-driven OTA, (b) self-cascode PMOS, (c) self-cascode NMOS.

the ratio of biasing currents, which is again equal to the W/L ratios of the corresponding MOS transistors.

As we can conclude from (1) and (2), the voltage gain of the OTA depends on the coefficient m, which is equal to the ratio of transconductances $g_{m7,8}/g_{m2}$ that expresses the amount of positive feedback. The closer the coefficient m is to unity, the higher the voltage gain. The maximum value of this coefficient is limited by g_m, the sensitivity to transistor mismatch. For instance, the g_m sensitivity to parameter m can be expressed as [20]:

$$S_m^{gm} = \frac{m}{1-m+p} - \frac{m}{1+m+g_{m1}/g_{m2}} \approx \frac{m}{1-m+p} \quad (3)$$

Thus, the g_m sensitivity increases as m tends to unity, i.e., with increasing voltage gain.

The maximum value of m is also limited by the frequency properties of the OTA, since increasing the value of m increases the resistance seen at the gate/drain nodes of M_2. This decreases the frequency of the parasitic pole associated with this node and can be expressed as [20]:

$$\omega_p = \frac{1-m+p}{1+m+g_{m1}/g_{m2}} \cdot \frac{g_{m2}}{C_{gs2}} \quad (4)$$

Thus, the frequency of the pole is approximately inversely proportional to the voltage gain A_{vo}. The partial positive feedback also improves the CMRR and PSRR parameters of the OTA, which can be expressed as [41]:

$$\mathrm{CMRR} = 2\frac{1+p/2}{p} \cdot \frac{(1+m+p)}{(1-m+p)} \quad (5)$$

$$PSRR \approx 2\frac{1+p/2}{p\,(1-m+p)\,(1+g_{m2}/g_{mb2})} \quad (6)$$

This is because PPF increases the differential voltage gain, without affecting the common-mode gain and the parasitic gain from V_{DD}. The input-referred noise of the OTA can be described by the following equation [41]:

$$\bar{v_{ni}^2} = N\left[\frac{8kT}{3g_{mb1}^2}\left(g_{m1}+g_{m5,6}\right) + \frac{1}{g_{mb1}^2 f C_{OX}}\left(\frac{K_p g_{m1}^2}{W_1 L_1} + \frac{K_n g_{m5,6}^2}{W_{5,6} L_{5,6}}\right)\right] \quad (7)$$

where:

$$N = \frac{1}{4}\frac{g_{m1}/g_{m2}}{(1+p/2)^2}\left[1+m+\frac{(1-m+p)^2}{g_{m1}/g_{m2}}\right] \quad (8)$$

where k is the Boltzmann constant, C_{OX} is the gate oxide capacitance per unit area, K_p and K_n are the flicker noise constants for the p- and n-channel transistors respectively, and the other symbols have their usual meaning or were defined earlier.

It can be concluded from (7) and (8) that the input referred noise of the OTA is approximately equal to the noise of a conventional bulk-driven differential pair, biased with the same total current and the same sum of transistor channel areas [41], [42].

In order to further increase the DC voltage gain of the OTA in the proposed solution, each transistor (except for the biasing M_3, M_4 and M_B) was replaced with a so-called self-cascode composite transistor, as shown in Fig.2 (b) and (c). Such a solution increases the voltage gain without sacrificing the voltage swing at the output of the OTA.

In a weak inversion region, with the $|V_{DS}|$ of the "bottom" triode operated transistor M_S tending to zero, the small signal transconductance of the self-composite transistor is approximately equal to the transconductance of the upper transistor M_D. Thus, it is equal to the transconductance of a single MOS transistor biased by the same current. However, the output resistance of a composite device is larger than that of a single MOS transistor and can be calculated as $r_{ds} \cong r_{dsD}(1 + g_{mD}r_{dsS})$. Thus, the intrinsic voltage gain of a self-cascode transistor is larger than that of a single MOS transistor, which further improves the DC voltage gain of the OTA.

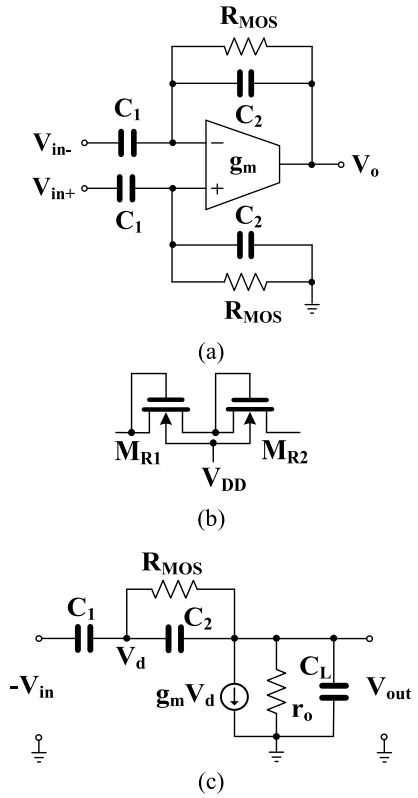

FIGURE 2. BPF using OTA, (a) schematic, (b) realization of R_{MOS}, (c) equivalent schematic.

The circuit was designed as follows. First, the coefficient m was chosen to be equal to 0.7, in order to increase the voltage gain by around 10 dB with acceptable sensitivity to transistor mismatch. The channel lengths for the M_D and M_S transistors were chosen to be 2 μm and 1 μm, respectively. Note that relatively large values of L were chosen to increase the r_{ds} resistances of the transistors. The nominal biasing current I_{set} was chosen to be 15 nA. This enables the circuit to obtain the required transconductance value as well as an acceptable value of the input referred thermal noise. The particular values of W for transistors were calculated to obtain dc voltages at an operating point equal to about half-supply for all diode-connected self-cascode transistors. Such a solution increased the available tuning range and provided sufficient headroom for variations of the potentials associated with process, voltage, and temperature (PVT). The relationship between W/L of the M_S and M_D transistors was chosen to obtain $|V_{DS}|$ voltages for the M_S transistors equal to around 10mV. This provided a good tradeoff between voltage gain and signal swing. Finally, the design was verified by simulations, including noise and Monte Carlo analyses.

B. PROPOSED BANDPASS FILTER

A conventional BPF is shown in Fig. 2 (a) [44]. The BPF is realized using a single-ended OTA, four capacitors, and two resistors. The capacitor C_1 eliminates the dc offset voltage from input electrodes. To avoid signal attenuation, the impedance of C_1 should be much smaller than the impedance of the signal electrode [45]. Utilizing capacitors in the feedback network eliminates the need for resistors with very large values and good linearity, which would be difficult to implement on a chip. The large resistors R_{MOS} in Fig. 2 (a) are used to properly bias the inputs of the OTA for DC. They are realized using two MOS transistors M_R with bulks connected to V_{DD}, as shown in Fig. 2 (b). Because of their very large values, they are bypassed by capacitors for AC.

The equivalent schematic of the bandpass filter, used to determine its transfer function, is shown in Fig. 2 (c), where C_L represents the load capacitance. The voltage gain of the BPF is described by bandpass characteristics. The voltage gain (G) in the middle of its bandwidth can be expressed as:

$$G = \frac{\frac{C_1}{C_2}}{1 + \left(1 + \frac{C_1}{C_2}\right)\frac{1}{A_v}} \tag{9}$$

where A_v is the open-loop voltage gain of OTA, given by (1). Note that for A_v tending to infinity, the ideal mid-band voltage gain of the BPF is given by:

$$G = \frac{C_1}{C_2} \tag{10}$$

Thus, G is established by the ratio of capacitances only, since in this frequency range their impedances are much lower than R_{MOS}. The lower cutoff frequency of the BPF can be expressed as:

$$f_L = \frac{1}{2\pi C_2 R_{MOS}} \tag{11}$$

Thus, f_L depends on the time constant being the product of R_{MOS} and C_2.

Due to the very large value of R_{MOS}, a very low cutoff frequency can be obtained (<1Hz), even for low values of C_2, which is desirable in order to limit the value of C_1 for large voltage gains.

The higher cutoff frequency of the BPF can be expressed as:

$$f_H = \frac{g_m\left(1 + \frac{C_1/C_2}{A_v}\right)}{2\pi\left(\frac{C_1}{C_2}\right)(C_2 + C_L)} \cong \frac{g_m}{2\pi\left(\frac{C_1}{C_2}\right)(C_2 + C_L)} \tag{12}$$

Except for the above poles, the circuit transmittance shows one right half-plane zero located at:

$$f_{RHP} = \frac{g_m}{2\pi C_2} \tag{13}$$

The value of f_{RHP} is typically much larger than f_H, and most often its impact can be neglected.

The input-referred noise of the BPF can be expressed by:

$$\overline{V_{ni,amp}^2} = \left(\frac{C_1 + C_2}{C_1}\right)^2 \cdot \overline{V_n^2} \tag{14}$$

where $\overline{V_n^2}$ and $\overline{V_{ni,amp}^2}$ are the input-referred noise of the OTA and BPF, respectively. Thus, for large voltage gains

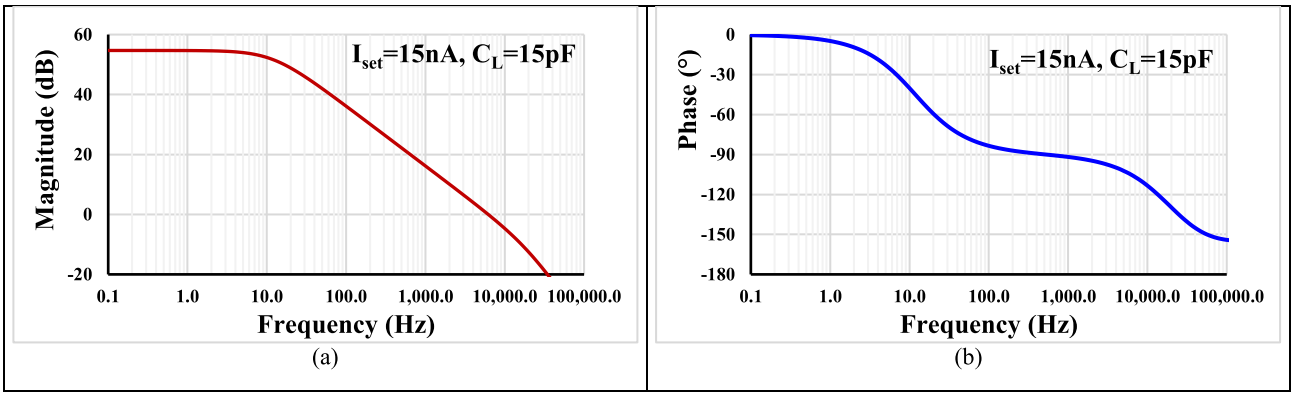

FIGURE 3. The frequency characteristic of the OTA (a) magnitude (b) phase.

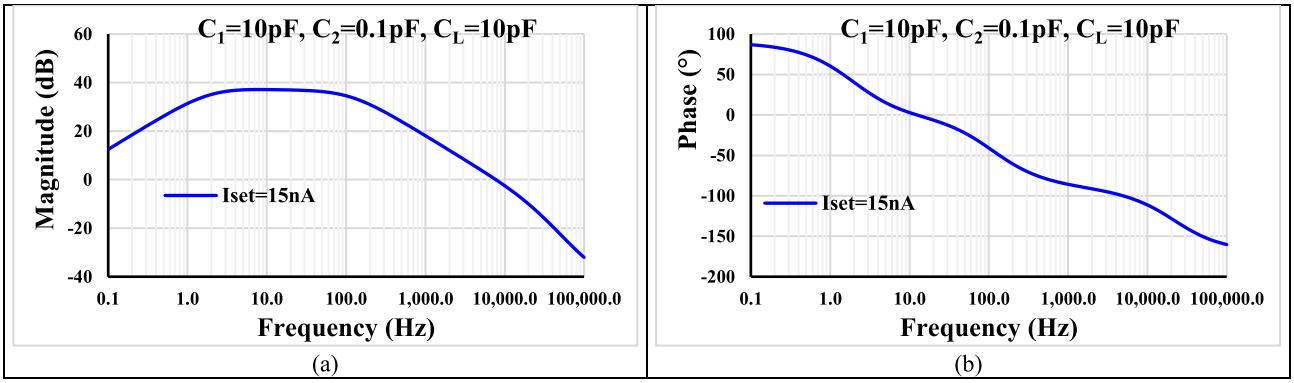

FIGURE 4. The magnitude (a) and phase characteristic (b) of the BPF.

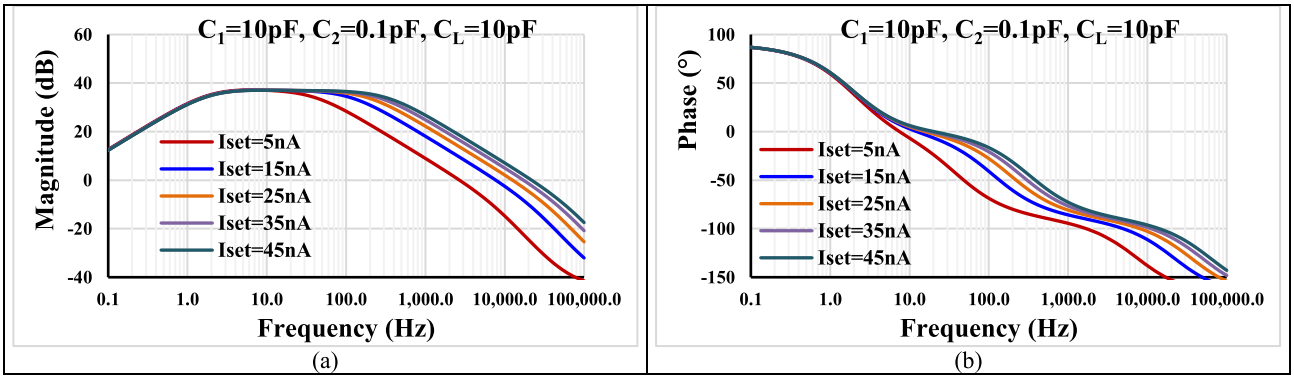

FIGURE 5. The magnitude (a) and phase characteristic (b) of the BPF for different I_{set}.

(large C_1/C_2 ratios), the input referred noise of the BPF is approximately equal to the input noise of the OTA itself.

From the above formulas, one can conclude that the mid-band gain of the BPF can be controlled by the value of C_1 with a constant C_2. Further, the lower cutoff frequency can be set by resistor R_{MOS} and the higher cutoff frequency can be adjusted by g_m.

III. SIMULATION RESULTS

The proposed structure was designed in the Cadence platform and simulated with the Spectre simulator of the Analog Design Environment, using a 0.18 μm CMOS process from TSMC where the threshold voltage of the MOS transistor is around 0.5 V. The voltage supply was 0.5 V ($\pm$0.25V) and the power consumption was 31.3 nW for 15 nA nominal setting current. The component values of the OTA are given in Table 1.

The frequency and phase characteristics of the OTA with a 15 pF load capacitance are shown in Fig. 3 (a) and (b), respectively. The low frequency gain was 54.7 dB, the gain bandwidth was 6.18 kHz and the phase margin was 75°. The input and output impedance of the OTA at low frequency were 74.7 GΩ and 890 MΩ, respectively.

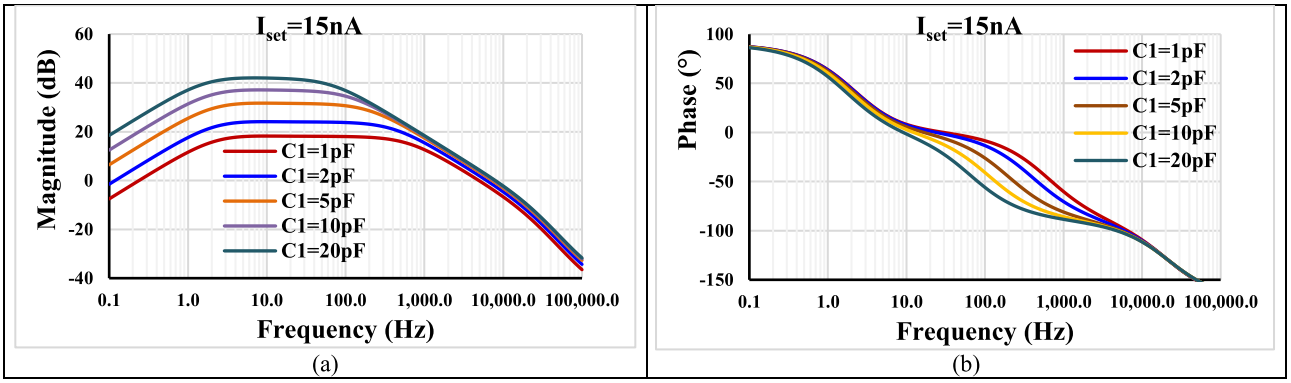

FIGURE 6. The magnitude (a) and phase characteristics of the BPF (b) for different C_1.

TABLE 1. Transistor aspect ratio of the OTA.

OTA	W/L (µm/µm)
S: M_{1A}, M_{2A},M_{1B}, M_{2B}	20/1
D: M_{1A}, M_{2A},M_{1B}, M_{2B}	20/2
S: M_7, M_8	14/1
D: M_7, M_8	14/2
S: M_5, M_6	20/1
D: M_7, M_8	20/2
M_3, M_4, M_B	10/1

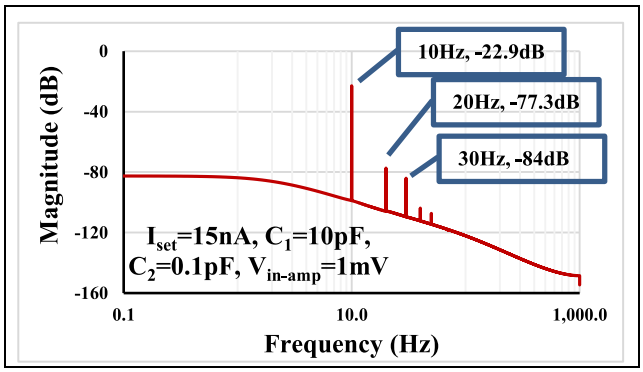

FIGURE 7. The FFT of the output signal.

The magnitude and phase characteristic of the BPF with $M_R = 4\mu m/15\ \mu m$, $I_{set} = 15$ nA, $C_1 = 10$ pF, $C_2 = 0.1$ pF and $C_L = 10$ pF are shown in Fig. 4. The mid-band gain was 37.1 dB, the lower and higher cut-off frequency was 1.5 Hz and 112 Hz, respectively. Note that the mid-band gain was slightly lower than the ratio of capacitances C_1 and C_2, due to the limited voltage gain of the OTA (see (9)). The power consumption of the BPF was 31.3 nW.

Fig. 5 shows the tuning capability of the higher cutoff frequency of the BPF by means of $I_{set} = (5, 15, 25, 35, 45)$ nA. The f_L was around 1.5 Hz while $f_H = 41.2$ Hz, 112 Hz, 186 Hz, 251 Hz and 317 Hz, respectively. Fig. 6 (a) and (b) shows, respectively, the magnitude and phase characteristics of the BPF with $I_{set} = 15$ nA, $C_2 = 0.1$ pF and various $C_1 = (1, 2, 5, 10, 20)$ pF, with $C_L = 10$ pF. This was done in order to increase the mid-band gain, which was 18.2 dB, 24.1 dB, 31.7 dB, 37.11 Hz and 41.98 dB, respectively. Based on the transient analysis, Fig. 7 shows the spectrum of the output signal using Fast Fourier Transform (FFT) when the input of the BPF is supplied by a sine wave signal with amplitude $V_{in-amp} = 1$ mV@ 10 Hz and $I_{set} = 15$ nA. The total harmonic distortion (THD) is obtained based on the FFT that indicates −53.56 dB (0.2%). The THD of the BPF for $V_{in-amp} = 1$ mV@ 10 Hz versus different $I_{set} = (5, 15, 25, 35, 45)$ nA and different $C_1 = (1, 2, 5, 10, 20)$ pF is shown in Fig. 8 (a) and (b), respectively. For all I_{set}, the THD is below 0.43% and for all C_1, the THD is below 1.2%. Thus, the BPF offers low THD.

The 200 runs Monte-Carlo (MC) process and mismatch analysis for the magnitude and phase characteristics of the BPF are shown in Fig. 9, indicating acceptable deviation. The histograms of the gain of the BPF @10Hz and the power consumption with $I_{set} = 15$ nA are shown in Fig. 10 (a) and (b), respectively. The mean value of the gain is 37.1 dB and the standard deviation is 43.6 mdB. The mean value of the power consumption is 31.3 nW with a standard deviation of 492 pW. This confirms the robustness of the design.

The process, voltage, and temperature (PVT) corner analysis for the magnitude and phase characteristics of the BPF are shown in Fig 11. The process corners (fast-fast, slow-fast, fast-slow, slow-slow), voltage corners ($V_{DD}\pm10\%$) and temperatures corners (−20°C, 70°C) were used. As it is evident, the curves overlap, thus confirming the robustness of the design against PVT corners. The input-referred voltage noise spectrum of the BPF is shown in Fig. 12. The thermal noise level is 0.8 $\mu V\sqrt{Hz}$. The integration of the noise from 1.5 Hz to 112 Hz yields a noise 17.9 μV_{rms}.

Fig. 13 (a) shows the ECG noisy signal that was applied to the input of the BPF containing low frequency 0.1mV @ 0.1Hz and high frequency 0.1mV @ 2kHz noises. The

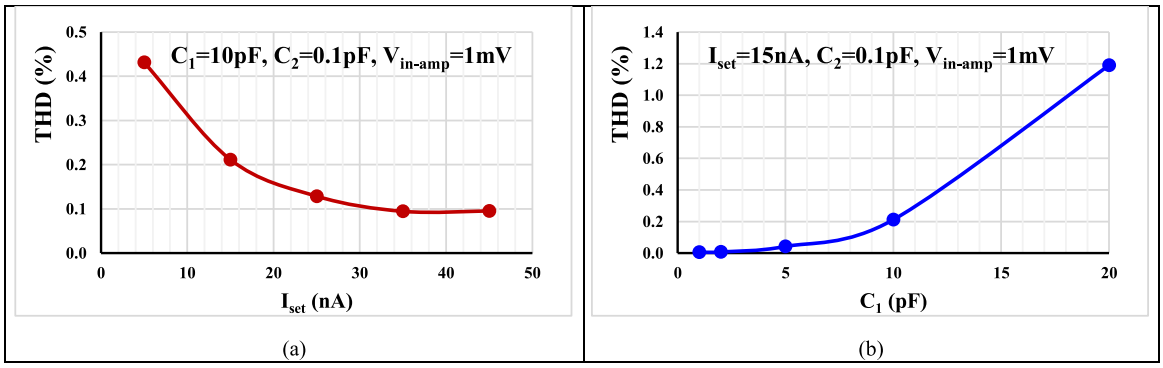

FIGURE 8. The total harmonic distortion of the output signal with different I_{set} (a) and different C_1 (b).

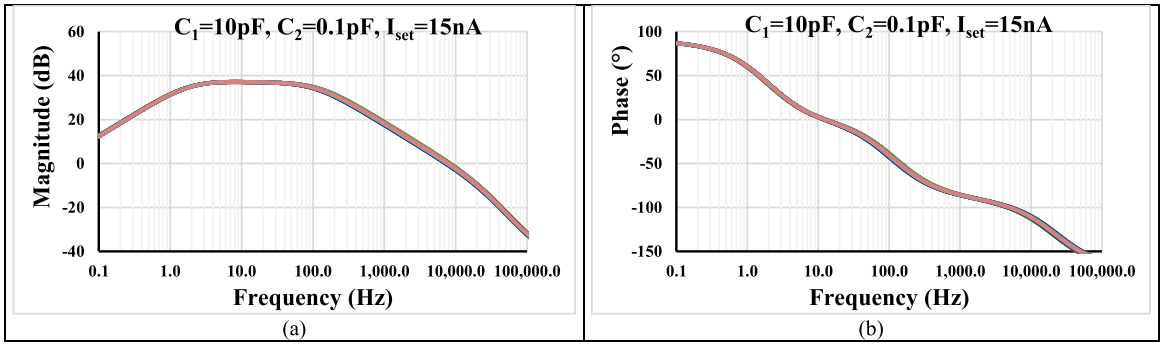

FIGURE 9. The magnitude (a) and phase characteristics of the BPF (b) with 200 runs MC.

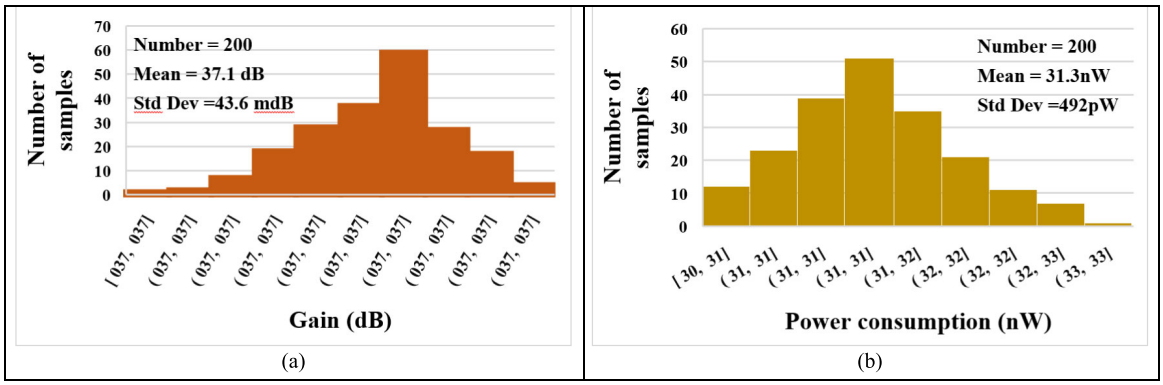

FIGURE 10. The histogram of the gain of the BPF @10Hz (a) and power consumption of the BPF (b) with 200 runs MC.

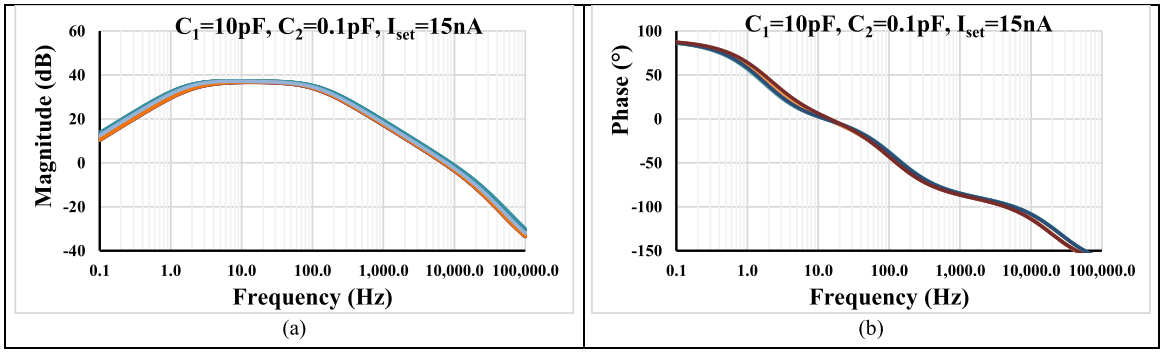

FIGURE 11. The magnitude (a) and phase characteristics (b) with PVT corners.

filtered and the amplified output signal is shown in Fig. 13 (b).

Table 2 shows the performance comparison of the proposed BPF with some previous works [24], [28], [29], [30], [31],

TABLE 2. Comparison of the proposed bpf and some previous works.

	This work	2022 [24]	2020 [28]	2022 [29]	2003 [30]	2023 [31]	2010 [35]	2007 [37]	2013 [38]
Technology (nm)	180	180	180	180	1500	180	180	350	180
OTA structure	BD-OTA	BD-OTA	BD-QFG-OTA	BD-DDA	GD-OTA	BD-OTA	GD-MOST	GD-OTA	DT-VDTA
Supply voltage (V)	0.5	0.5	1	0.5	2.8	0.6	1	1	0.4
Power consumption (μW)	0.0313	0.06	1.1	0.626	0.23	1.65	0.0144	0.068	0.0127
Order	2	3	2	2	4	2	4	6	2
Gain (dB)	37.1	~-6	39.9	39.6	~0	~0	~-5	-	~-8
Bandwidth (Hz)	1.5-112	250 (f_c/BW)	0.266-2.8k	0.1-150	200	17.48-20.72k	523-1.024k	670	19.5 (f_c/BW)
THD (dB)	-53.56	-44.73	-	-49.37	-	-40	-40	-	-33.97
Input referred noise (μVrms)	17.9	240	3.15	59	323	190.5	50	50	22.9
Dynamic range (dB)	55.5	60.4	-	-	65	47.4	55	49	63.7
CMRR (dB)	75	-	-	-	-	-	-	-	-
PSRR (dB)	87.7	-	-	-	-	-	-	-	-
FoM	12.5×10^{-13}	6.62×10^{-13}	-	-	119×10^{-13}	5.04×10^{-13}	0.64×10^{-13}	3.4×10^{-13}	20.4×10^{-13}
Area (mm2)	0.0167*	0.0435	-	-	-	-	0.132	0.234	-
Obtained results	Sim.	Sim.	Sim.	Sim.	Exp.	Sim.	Exp.	Exp.	Sim.

* estimated, VDTA = voltage differencing transconductance amplifier, f_c = center frequency, GD-MOST = gate-driven MOS transistor, BW = bandwidth

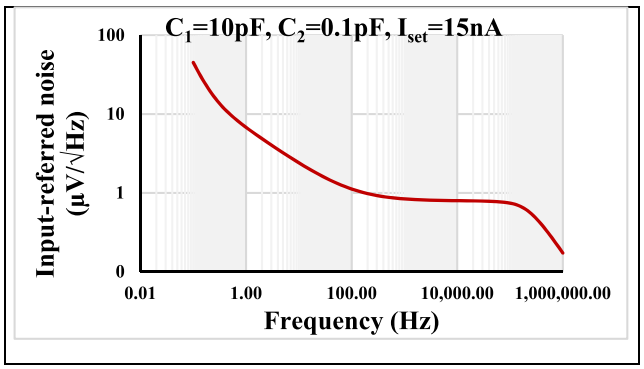

FIGURE 12. The input-referred voltage noise spectrum.

[35], [37], [38]. Compared with BPFs that can control gain and bandwidth in [28] and [29], the proposed circuit clearly has lower power consumption. Compared with BPFs in [24] and [35], the proposed circuit can control gain and has lower power consumption than [24]. Compared with [31] and [38], the proposed BPF can control gain and bandwidth. Although the input referred noise is higher when compared with [28], due to the bulk-driven technique, the proposed circuit has much lower power consumption and voltage supply (31.3 nW, 0.5 V versus 1.1 μW, 1 V). Therefore, the circuit is a trade-off between the voltage supply and power consumption on one hand and the input referred noise on the other. The THD for the proposed BPF is the lowest compared to other designs. The estimated chip area of the BPF including a 10 pF load capacitance is 0.0167 mm^2. Finally, the figure of merit

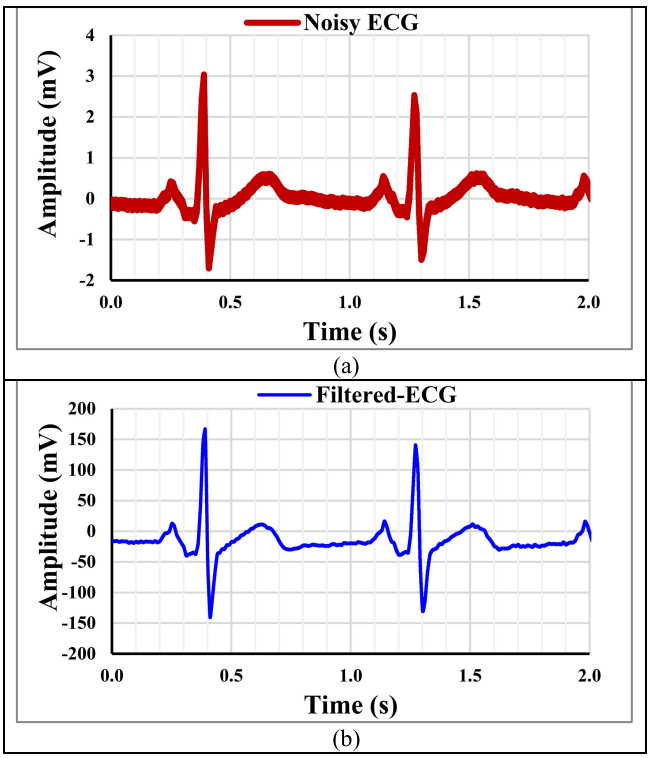

FIGURE 13. The noisy input ECG signal (a) and the filtered output signal (b).

(FoM), defined in [37], has been used

$$FoM = \frac{P \times V_{DD}}{N \times f_o \times DR} \tag{15}$$

where p is the power consumption, VDD is the supply voltage, N is the order, f_o is the center frequency, DR is the dynamic range.

IV. CONCLUSION

This paper presents a new BPF using low-voltage and low-power OTA. The OTA is realized using BD MOST operating in the subthreshold region; thus, it can work with 0.5 V of voltage supply and 31.3 nW of power. The structure was designed in the Cadence program using 0.18 μm CMOS technology from TSMC. The simulated results agree with the theoretical analysis. The proposed BPF can be applied to biomedical signals, such as local field potential, electroencephalogram, and electrocorticography.

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