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RESEARCH ARTICLE

0.3-V, 357.4-nW Voltage-Mode First-Order Analog Filter Using a Multiple-Input VDDDA

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ABSTRACT In this paper, a new versatile first-order voltage-mode analog filter using a single multiple-input voltage differencing differential difference amplifier for extremely low-voltage supply and low-frequency applications is presented. Using multiple-input MOS transistor technique, the filter can realize the first-order transfer functions of non-inverting and inverting low-pass, high-pass, and all-pass filters in a single topology with high input and low output impedance. This is particularly useful for voltage-mode circuits. The filter's pole frequency can be controlled electronically. The filter was used to implement a new quadrature oscillator to confirm its advantages. The multiple-input was applied to bulk-driven differential pairs operating in weak inversion; therefore, the proposed circuit operated from a supply voltage of 0.3 V and consumed 357.4 nW. The circuit was designed in the Cadence program using 0.13 μm UMC CMOS technology. The performance and robustness of the design was validated by intensive simulations, including Monte Carlo and Process, Voltage and Temperature corner analyses.

INDEX TERMS Voltage differencing differential difference amplifiers, analog filters, first-order filters, ultra-low power circuits.

I. INTRODUCTION

The active building block called a voltage differencing differential difference amplifier (VDDDA) was first introduced in [1]. This device has the advantages of an operational transconductance amplifier, such as the possibility of electronic tuning, and of a differential difference current conveyor (DDCC), such as the possibility of arithmetic operations in voltage mode. Unlike the differential difference transconductance amplifier (DDTA), which has high input and output impedance, the VDDDA is more suitable for voltage-mode operation and filter cascading due to its high input and low output impedance [1], [2], [3], [4], [5], [6], [7], [8]. VDDDA has been successfully used in various applications reported in the literature [1], [2], [3], [4], [5], [6], [7], [8]. The utility of VDDDA with conventional CMOS structure was demonstrated in [1] on a novel first-order resistorless voltage-mode all-pass filter and in the design of a voltage-mode quadrature oscillator with a supply voltage of ±0.9 V and a power consumption of 0.99 mW. In [2], the VDDDA was used to implement a universal voltage-mode filter using commercially available integrated circuits (LT1228 from Linear Technology Inc. and AD830 from Analog Device Inc.) with a supply voltage of ±5 V. In [3], a VDDDA-based voltage-mode shadow filter with a conventional CMOS structure and a supply voltage of ±0.9 V was presented. Reference [4] presents an electronically tunable quadrature sinusoidal oscillator based on VDDDA with commercially available integrated circuits and a supply voltage of ±5V. In [5], the implementation of a grounded inductance simulator using

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a single VDDDA with a conventional CMOS structure and a supply voltage of ±0.9 V and a power consumption of 127 μW was presented. In [6], a capacitive multiplier implementation using a VDDDA with commercially available ICs and a voltage of ±5 V was used. In [7], a universal filter based on a compact multiple-input gate-driven CMOS VDDDA structure with a supply voltage of ±0.9 V and a power consumption of 0.99 mW was presented. In [8], an analog current mode VDDDA filter using 32 nm CNTFET technology, conventional CMOS topology with ±0.9 V supply and 166 μW power consumption was used. As mentioned above, the VDDDA CMOS structures in [1], [3], and [5] are standard and not innovative. All VDDDAs [1], [2], [3], [4], [5], [6], [7], [8] are incompatible with extremely low supply voltage and low power consumption, which makes them impossible to use in extremely low voltage applications powered by batteries or power harvesting sources.

Low-voltage, low-power CMOS analog circuits are an important design consideration in modern portable and battery-powered electronics, sensors, and in biomedical and energy harvesting applications where energy efficiency is critical to maximize uptime. Ultra-low voltage circuits typically operate with a supply voltage (V_{DD}) around or even below the threshold voltage (V_{TH}) of a single MOS transistor, i.e. $V_{DD} \leq V_{TH}$. They use specialized and unconventional design techniques to operate reliably at such extremely low supply voltages while maintaining acceptable performance specifications such as input common mode range, gain, bandwidth, and noise. Techniques such as the following are widely used in literature to achieve low-voltage operation: weak inversion MOS transistors, bulk-driven (BD), multiple-input floating-gate (MIFG), quasi-floating-gate (QFG), multiple-input MOS transistors (MI-MOST), self-cascode MOS transistors, which are widely used in the literature [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]. Low power consumption can be achieved through the minimization of the number of active components and reduction of their operating voltages and currents.

For first-order filters, three filter functions can be implemented, namely a low-pass (LP) filter, a high-pass (HP) filter, and an all-pass (AP) filter. These first-order filters can be used in signal processing, for example, as high-order filters, sinusoidal oscillators, frequency-selective filters with a quality factor, group delay filters, or phase equalizers [27], [28], [29], [30]. There are many versatile first-order filters in the literature that can implement LP, HP, and AP filters from a single topology. This paper focuses on first-order voltage-mode universal filters. These filters should provide high input and low output impedance, which is valuable for voltage-mode circuits. First-order voltage-mode and mixed-mode filters have been published in the open literature [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50]. The filters in [31], [32], [35], [37], [38], [39], [41], and [50] use capacitors and/or resistors into the input signal path, which is not ideal for cascading voltage-mode circuits. In [33], [34], and [36], some filter functions do not provide low output impedance. The filters in [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [31], [32], [32], [33], [33], [34], [34], [35], [35], [36], [36], [37], [37], [38], [39], [39], [40], [40], [41], [42], [43], [44], [45], and [46] offer only three transfer functions of LP, HP, AP filters. The filters in [38] and [41] offer voltage-gain of transfer functions; however, they offer only four transfer functions of LP, HP, AP filters (non-inverting and inverting AP). Although the filter in [47] can provide all first-order noninverting and inverting universal responses, the circuit uses two differential voltage-current conveyors (DVCCs). Filters including voltage mode (VM), trans-admittance mode (TAM), current mode (CM), and trans-impedance mode (TIM) are described in [48], [49], and [50], but the VM of these filters only provides three transfer functions of LP, HP, AP filters. It should be noted that the universal filters in [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], and [50] are implemented using high-power supply (i.e., >1 V) and high-power consumption devices, which are not suitable for low-power signal processing applications.

This paper introduces the multiple-input VDDDA (MI-VDDDA). It incorporates several design techniques such as a bulk-driven MOS transistor operating in weak inversion to minimize the voltage supply and achieve the ability to operate at V_{DD} lower than V_{TH}. In addition, the MI-MOST technique is used to minimize the number of active components by maintaining a single differential pair, thus reducing power consumption. As a result, the circuit can operate at 0.3 V, 357.4 nW while providing a rail-to-rail input voltage range. The MI-VDDDA was used to implement the first-order transfer functions of non-inverting and inverting low-pass, high-pass and all-pass filters in a single topology with high input and low output impedance. Thus, it is ideally suited for voltage-mode circuits. The rest of this paper is organized as follows: in Section II, the CMOS structure of the MI-VDDDA and the proposed first-order universal voltage filter are presented, and their theoretical description is given. In Section III, an example application of the quadrature oscillator is presented. Intensive simulation results of the filter and oscillator are presented in Section IV, while Section V concludes this paper.

II. PROPOSED CIRCUIT

A. THE MI-VDDDA

Fig. 1 (a) shows the symbol of the conventional voltage differencing differential difference amplifier (VDDDA) that was introduced in [1]. This device is composed of a transconductance amplifier (TA) as a first stage, followed by a differential difference current conveyor (DDCC) as a second stage. The port characteristic of the conventional VDDDA in Fig. 1 (a) can be expressed by:

$$\left.\begin{aligned} I_z &= g_m (V_+ - V_-) \\ V_w &= V_z - V_n + V_p \end{aligned}\right\} \quad (1)$$

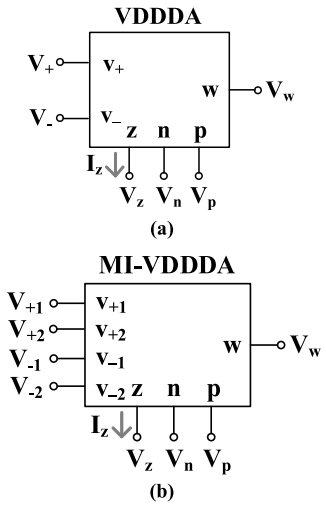

FIGURE 1. Symbol of (a) a conventional VDDDA, (b) the proposed MI-VDDDA.

This device has a high-impedance differential voltage input V_+ and V_-, a high-impedance current output z, high-impedance voltage inputs V_n and V_p, and a low-impedance voltage output w. The differential voltage V_+–V_- is transferred to the current output I_z with the transconductance g_m.

Fig. 1 (b) shows the electrical symbol of the multiple-input VDDDA proposed in this work. Its port characteristics are like those of the conventional VDDDA [1], except for a differential voltage input. The proposed MI-VDDDA has multiple differential voltage inputs; thus, its operation can be expressed as:

$$\left.\begin{aligned} I_z &= g_m\left(V_{+1} - V_{-1} + \ldots + V_{+(n)} - V_{-(n)}\right) \\ V_w &= V_z - V_n + V_p \end{aligned}\right\} \quad (2)$$

Fig. 2. shows the CMOS implementation of the proposed MI-VDDDA. The multiple-input MOS transistor (MOST) technique [24], [26], as shown in Fig. 3 (a)-(c), is used to realize this multiple input device; hence, the MI-VDDDA is realized without increasing the number of active components by maintaining one differential pair and preserving the same power consumption. Unlike the low-voltage DDTA (DDCC followed by TA) presented in [25], the proposed MI-VDDDA is a multiple-input TA (MI-TA) followed by DDCC. This provides a high-input, low-output impedance active block suitable for voltage-mode applications. Thanks to the MI-MOST technique that used for both, the differential pair of the TA and DDCC, the input terminals and the versatility of the MI-VDDDA is increased.

The adapted transconductance amplifier is based on the non-tailed differential pair $M_{1A,B}$ and $M_{2A,B}$, biased by the current sinks M_3 and M_4 and the linearization resistance R. The transistors M_5 and M_6 operate as active load and provide single-ended output for the TA. The non-tailed architecture allows the device to operate from a very low supply voltage. The basic form of the amplifier, i.e., without MI transistors at the input, was first proposed and validated experimentally using 0.13 μm technology in [11]. Here, the input transistors M_{1A} and M_{1B} were replaced by MI devices, thus realizing a mathematical summing of the input voltages V_1 and V_2, as described by the first equation of (2).

Assuming equal capacitances C_B in the input transistors (see Fig.3.b) for frequencies where the voltage gain of the input capacitive divider is determined by the capacitances C_B only (i.e., $1/\omega C_B \ll R_{MOS}$), the circuit transconductance is given by:

$$g_m = \beta_1 g_{mo} \quad (3)$$

where $\beta_1 = 1/2$ is the attenuation factor for the input capacitive divider and g_{mo} is the transconductance of the TA determined from the bulk terminals of M_{1A} and M_{1B} [11]:

$$g_{mo} = 2g_{mb1,2}\frac{R + \frac{1}{g_{m1,2}}}{R + \frac{2}{g_{m1,2}}} \quad (4)$$

where $g_{m1,2}$ is the transconductance of the input transistors $M_{1A,B}$ and $M_{2A,B}$ (assumed identical) and $g_{mb1,2}$ is their bulk transconductance.

As shown in [11], the circuit linearity depends on the value of the linearization resistance R, and optimum linearity is achieved if the following condition is met:

$$R = \frac{1}{g_{m1,2}} \quad (5)$$

Note that the circuit linearity remains good even for relatively large incompatibilities between R and $1/g_{m1,2}$, allowing transconductance tuning. Moreover, in the proposed circuit, the input capacitive divider further increases the linear range of the TA. For optimal linearity, the circuit transconductance is given by:

$$g_m = \beta_1 \frac{4}{3} \cdot \eta \frac{1}{R} \quad (6)$$

where $\eta = g_{mb1,2}/g_{m1,2}$ is the bulk to gate transconductance ratio for the input transistors at the operating point. Due to the non-cascode structure of the TA, the voltage gain of the circuit is relatively low and can be expressed as:

$$A_{VTA} = g_m\left(r_{ds1,2} || r_{ds5,6}\right) \quad (7)$$

The second block of the proposed MI-VDDDA is the differential-difference current conveyor. The DDCC is a two-stage structure, where the first stage is a differential difference amplifier (M_1-M_6). The two differential input ports were realized using MI devices, eliminating the need for a second pair of transistors, and thus simplifying the overall structure and saving power. The core of the input stage (with conventional transistors at the inputs) was first proposed in [9] and validated experimentally in [10]. It consists of a non-tailed differential pair with partial positive feedback (PPF), introduced by the cross-coupled transistors M_7 and M_8. The PPF circuit was introduced to improve the voltage gain of the first

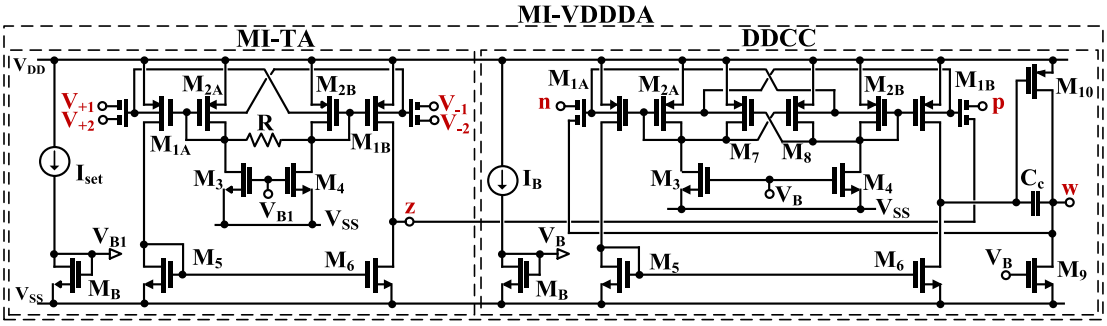

FIGURE 2. CMOS structure of the multiple-input VDDDA.

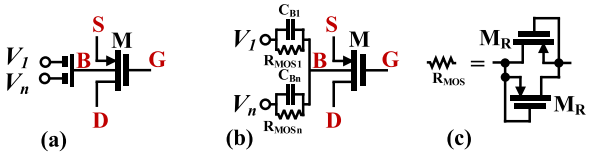

FIGURE 3. MI-BD MOST: (a) symbol, (b) realization, and (c) possible implementation of R_{MOS}.

stage, which, neglecting the input capacitive divider, can be expressed as:

$$A_{v1} = \frac{2g_{mb1,2}}{1-m}\left(r_{ds1}||r_{ds5}\right) \tag{8}$$

where the coefficient m = $g_{m7,8}/g_{m1,2}$.

The second stage of the DDCC is a common-source amplifier based on the transistor M_{10} loaded by the current sink based on M_9, with a voltage gain of:

$$A_{v2} = g_{m10}\left(r_{ds9}||r_{ds10}\right) \tag{9}$$

The overall voltage gain of the DDCC can be expressed as:

$$A_v = \frac{\beta_2 A_{v1} A_{v2}}{1+\beta_2 A_{v1} A_{v2}} \tag{10}$$

where $\beta_2 = 1/2$ is the voltage gain of the input capacitive divider at the bulk terminals of $M_{1,2}$. Due to the relatively high value of the open-loop gain ($\beta_2 A_{v1} A_{v2}$), the voltage gain A_v is very close to unity, as is required in this application.

The circuit stability in closed loop configuration is provided by the capacitance C_C, and the GBW product of the DDCC is given by:

$$GBW = \beta_2 \frac{2g_{mb1,2}}{(1-m)\,C_C} \tag{11}$$

As in other two-stage amplifiers, the GBW product in practice is limited by the frequency of the output pole (g_{m10}/C_{Lw}), which depends on the load capacitance of the w terminal (C_{Lw}) and should not exceed around a half of this frequency.

The output resistance of the DDCC (MI-VDDDA), seen from the w terminal, can be approximated as:

$$r_{outW} \cong \frac{1}{\beta_2 A_{v1} g_{m10}} \tag{12}$$

Thus, it is equal to the reciprocal value of g_{m10} multiplied by the voltage gain of the first stage, which makes it possible to obtain a relatively low value of this resistance.

It should be noted here that although the presented VDDDA in Fig. 2 appears to be somewhat more complex compared to the conventional VDDDA design, it can operate with extremely low supply voltages, even much lower than the threshold voltage of a single MOS transistor (i.e., $V_{DD} = 0.3 < V_{TH} = 0.5V$). The proposed block offers suitable parameters for low-frequency applications, such as rail-to-rail input voltage range, high linearity, and low power consumption. Furthermore, using MI-MOST simply increases the number of VDDDA inputs without the need for additional input differential pairs that result in additional power consumption and CMOS structure complexity. Ultimately, an MI-VDDDA based application is less complex with a minimum number of active blocks compared to an application using a conventional VDDDA structure. It is worth noting here that the circuit is intended for low frequency applications, such as biosignal processing. The spectrum of these biosignals ranges from sub-hertz to 10 kHz.

B. PROPOSED VOLTAGE-MODE FIRST-ORDER UNIVERSAL ANALOG FILTER

Fig. 4 shows the proposed voltage-mode first-order universal filter using MI-VDDDA. The proposed first-order filter with four-inputs and one-output employs one MI-VDDDA and one grounded capacitor. The input signals V_1, V_2, V_3, and V_4 supply through the high-impedance terminals V_{+1}, V_{-2}, p, and n of the MI-VDDDA. The output signal V_{out} is connected to the low-impedance terminal w of the MI-VDDDA. Therefore, the proposed filter provides high-input impedance and low-output impedance which is optimal for voltage-mode circuits.

Using (2) and nodal analysis, the output voltage of Fig. 4 can be expressed by:

$$V_{out} = \frac{sC_1\left(V_3 - V_4\right) + g_m\left(V_1 - V_2\right)}{sC_1 + g_m} \tag{13}$$

From (13), the first-order LP, HP, and AP filters can be obtained by appropriately applying the input signals. The variant filtering functions of first-order filters are shown in Table 1. It is evident from Table 1 that both non-inverting and

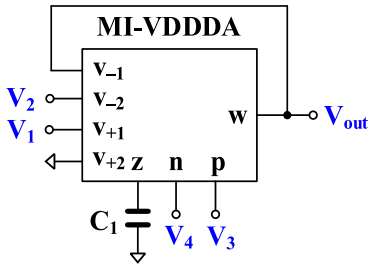

FIGURE 4. Proposed voltage-mode first-order universal analog filter.

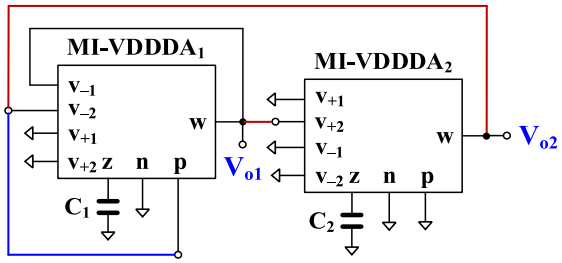

FIGURE 5. Proposed quadrature oscillator circuit using MI-VDDDA-based all-pass filter.

TABLE 1. Obtaining variant filtering functions of the first-order analog filter.

Filtering Function		Input	Transfer Function
LP	Non-inverting	$V_1 = V_{in}$	$H(s) = \frac{g_{m1}}{sC_1 + g_{m1}}$
	Inverting	$V_2 = V_{in}$	$H(s) = -\frac{g_{m1}}{sC_1 + g_{m1}}$
HP	Non-inverting	$V_3 = V_{in}$	$H(s) = \frac{sC_1}{sC_1 + g_{m1}}$
	Inverting	$V_4 = V_{in}$	$H(s) = -\frac{sC_1}{sC_1 + g_{m1}}$
AP	Non-inverting (phase lag)	$V_1 = V_4 = V_{in}$	$H(s) = -\frac{sC_1 - g_{m1}}{sC_1 + g_{m1}}$
	Inverting (phase lead)	$V_2 = V_3 = V_{in}$	$H(s) = \frac{sC_1 - g_{m1}}{sC_1 + g_{m1}}$

inverting transfer functions of LP, HP, and AP filters can be obtained from Fig. 4. The proposed multiple-input universal filter with high-input impedance does not require additional circuits, such as buffer circuits, nor does it require inverting amplifiers to generate inverting input signals.

The pole frequency (ω_o) of all filters can be given by:

$$\omega_o = \frac{g_m}{C_1} \tag{14}$$

Thus, the pole frequency of the filters can be electronically controlled using g_m via the bias current of the MI-VDDDA.

C. NON-IDEALITY ANALYSIS

This section shows the effect of the non-ideality of the MI-VDDDA on the performances of the proposed first-order filter. Because the proposed MI-VDDDA is expected to work within a limited operating frequency, the parasitic parameters at the input and output terminals of the MI-VDDDA, such as impedances and capacitances, are absent from consideration. There are two non-ideal characteristics that are considered: the transconductance gain error (g_{mn}) and voltage gain errors (β). Thus, the terminal relationships in (2) can be rewritten as:

$$\left.\begin{aligned} I_z &= g_{mn}\left(V_{+1} - V_{-1} + \ldots + V_{+(n)} - V_{-(n)}\right) \\ V_w &= \beta_z V_z - \beta_n V_n + \beta_p V_p \end{aligned}\right\} \tag{15}$$

where g_{mn} is the transconductance gain error and β_z, β_n, and β_p are the voltage gain errors from the z-, n-, and p-terminals to the w-terminal. Ideally, these voltage gains are equal to unity. In the frequency range near its cutoff frequency, the transconductance gain error can be expressed by [51]:

$$g_{mn} \cong g_m\left(1 - \mu s\right) \tag{16}$$

where $\mu = 1/\omega_{gm}$, ω_{gm} denotes the first-order pole.

Using (15), (13) can be rewritten as:

$$V_{out} = \frac{sC_1\left(\beta_p V_3 - \beta_n V_4\right) + \beta_z g_{mn}\left(V_1 - V_2\right)}{sC_1 + \beta_z g_{mn}} \tag{17}$$

Thus, the inverting and non-inverting transfer functions of LP, HP, and AP filters can be rewritten respectively as

$$\left.\begin{aligned} H(s) &= \frac{\beta_z g_{mn}}{sC_1 + \beta_z g_{mn}} \\ H(s) &= -\frac{\beta_z g_{mn}}{sC_1 + \beta_z g_{mn}} \end{aligned}\right\} \tag{18}$$

$$\left.\begin{aligned} H(s) &= \frac{\beta_p sC_1}{sC_1 + \beta_z g_{mn}} \\ H(s) &= -\frac{\beta_n sC_1}{sC_1 + \beta_z g_{mn}} \end{aligned}\right\} \tag{19}$$

$$\left.\begin{aligned} H(s) &= -\frac{\beta_n sC_1 - \beta_z g_{mn}}{sC_1 + \beta_z g_{mn}} \\ H(s) &= \frac{\beta_p sC_1 - \beta_z g_{mn}}{sC_1 + \beta_z g_{mn}} \end{aligned}\right\} \tag{20}$$

Using (15), the denominator ($D(s)$) of these transfer functions can be expressed as:

$$D(s) = sC_1\left(1 - \frac{\beta_z \mu g_m}{C_1}\right) + \beta_z g_m \tag{21}$$

It can be made negligible by satisfying the following condition:

$$\frac{\beta_z \mu g_m}{C_1} \ll 1 \tag{22}$$

The pole frequency in (14) becomes:

$$\omega_o = \frac{\beta_z g_m}{C_1} \tag{23}$$

It follows from (18)-(20) and (23) that the non-idealities of the MI-VDDDA slightly affect the circuit characteristics.

If consider the parasitic effect on the VDDDA [7], the parasitic impedances at z-terminal ($R_z//C_z$) and w-terminal (R_w) will be considered. The parasitic capacitance can be minimized by setting the value of $C_1 \gg C_z$ while the parasitic resistance R_z can be minimized by setting the value of

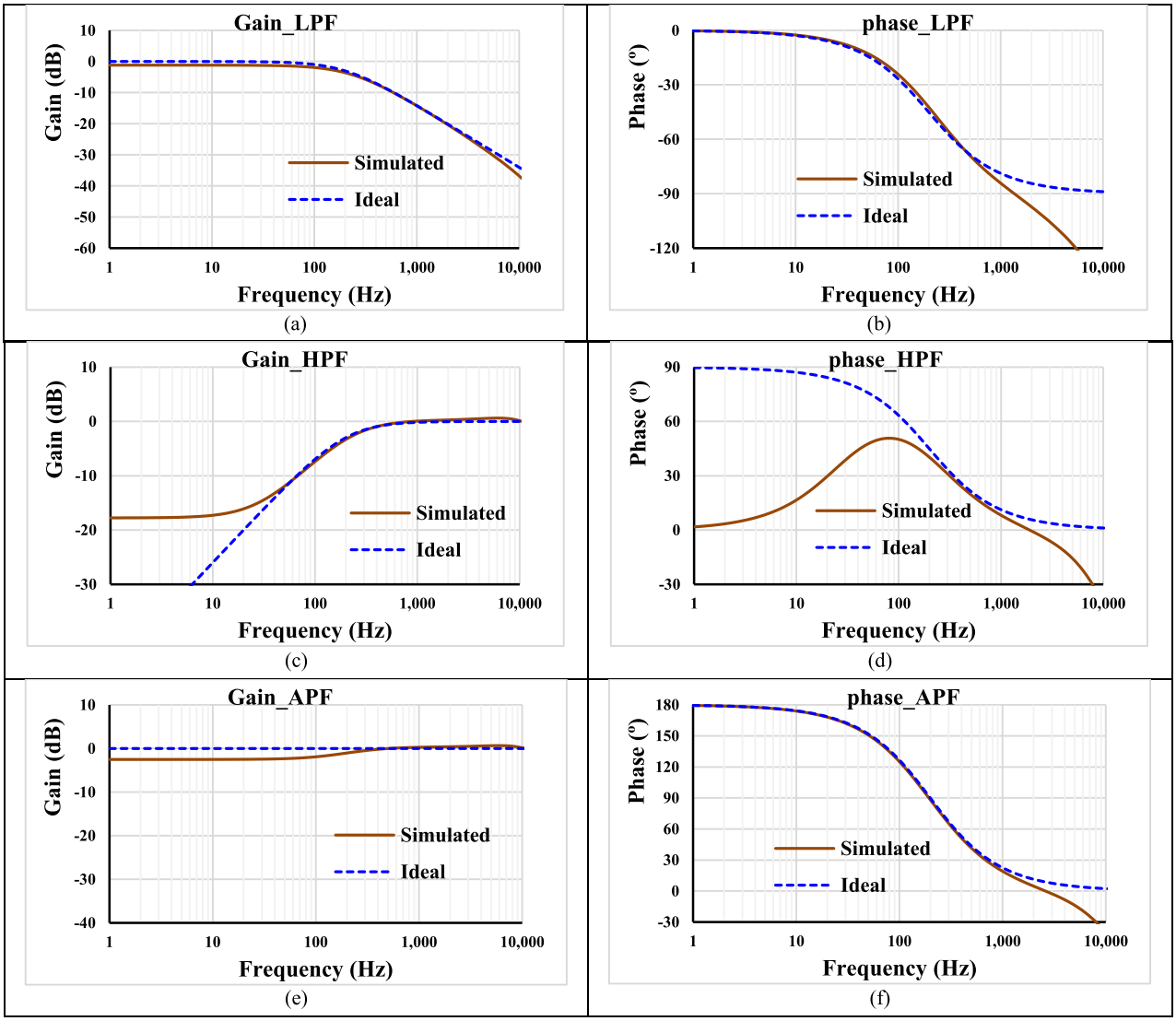

FIGURE 6. Gain and phase characteristics: (a,b) LPF; (c,d) HPF; (e,f) APF.

$1/g_m \gg R_z$, the parasitic resistance R_w can be minimized by using the value of load resistance R_L higher than R_w ($R_L > R_w$). Usually, R_w of VDDDA is low. Note, that the effect of parasitic impedance, which occurs at much higher frequencies than the bio-signals has negligible effect on the performance of the application.

III. APPLICATION EXAMPLE

Fig. 5 shows the proposed quadrature oscillator circuit using the MI-VDDDA-based first-order all-pass filter. The circuit consists of an inverting first-order AP filter (MI-VDDDA$_1$ and C_1) and a lossless integrator (MI-VDDDA$_2$ and C_2).

The nodes V_{o1} and V_{o2} of the circuit possess a low impedance level, hence loads can be directly connected without buffer circuits. Using the transfer function of the inverting AP filter from Table 1 and letting the unity loop (LG) gain (LG=1), we obtain:

$$\left(\frac{sC_1 - g_{m1}}{sC_1 + g_{m1}}\right)\left(\frac{g_{m2}}{sC_2}\right) = 1 \tag{24}$$

The characteristic equation of the oscillator can be given by:

$$s^2C_1C_2 + s\left(C_2g_{m1} - C_1g_{m2}\right) + g_{m1}g_{m2} = 0 \tag{25}$$

Letting $g_{m1} = g_{m2}$, the condition of oscillation can be given as:

$$C_2 = C_1 \tag{26}$$

The frequency of oscillation is:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{27}$$

The condition of oscillation can be given by C_1 and C_2 whereas the frequency of oscillation can be controlled electronically by $g_m (g_m = g_{m1} = g_{m2})$. The proposed oscillator

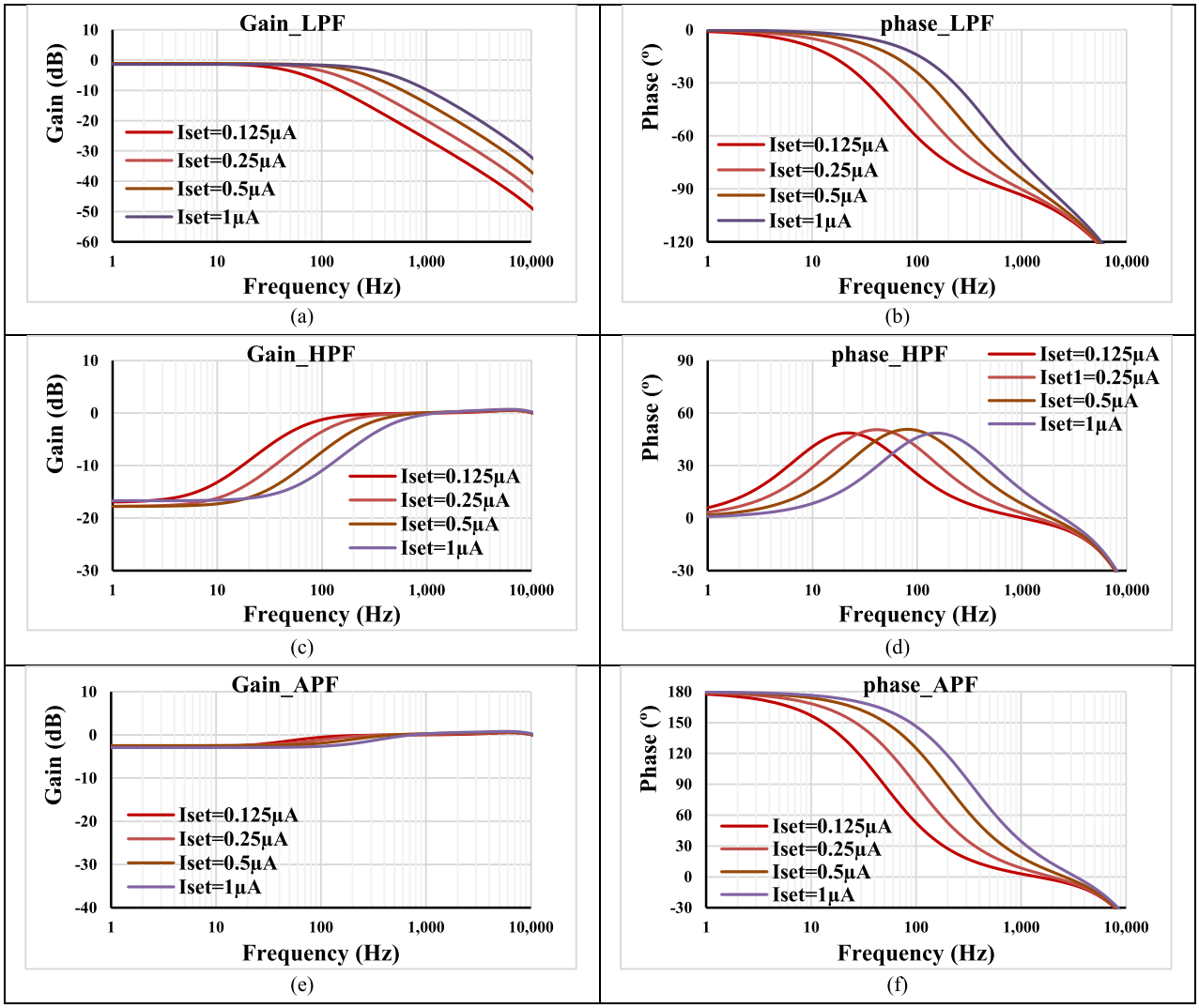

FIGURE 7. Gain and phase characteristics: (a,b) LPF; (c,d) HPF; (e,f) APF with various I_{set}.

also possesses orthogonally controlled condition and frequency of oscillation. Considering the MI-VDDDA$_2$ and C_2 are composed as a lossless integrator, the transfer function between nodes V_{o2} and V_{o1} can be expressed by:

$$\frac{V_{o2}}{V_{o1}} = \frac{g_{m2}}{sC_2} \tag{28}$$

At oscillating frequency (ω_o), the magnitude of the signal is $\left|g_{m2}/C_2\right|$ and the phase difference between V_{o1} and V_{o2} is 90°.

TABLE 2. Transistor aspect ratios and passive components of the MI-VDDDA.

Device	W/L (µm/µm)
M_{1A}, M_{2A}, M_{1B}, M_{2B}	20/3
M_7, M_8	15/3
M_3-M_6, M_B	10/3
M_9	6 × 10/3
M_{10}	6 × 20/3
M_R	5/3
MIM capacitor: C_B = 0.2 pF, C_c = 4 pF	
Poly-resistor R = 90 kΩ	

IV. SIMULATION RESULTS

The Cadence Virtuoso Analog Design Environment, using 130 nm CMOS technology from UMC, was used to design the circuit. Table 2 includes the transistor aspect ratio of the MI-VDDDA and values of passive components. The voltage supply was 0.3 V (±0.15V), the nominal value of the setting current was $I_{set} = 0.5$ μA, the bias current $I_B = 50$ nA, and the nominal power consumption of the MI-VDDDA was 357.4 nW. The MI-TA linear resistor's R was a high-resistance poly-resistor. The input and compensation capacitors were highly linear metal–isolator–metal capacitors (MIM). The open-loop gain of the DDCC (i.e. without the unity gain feedback) was simulated as 73.9 dB and the phase margin was 56.2° for 20 pF load capacitor. The low-frequency gain for V_w/V_p and V_w/V_n is 14 mdB

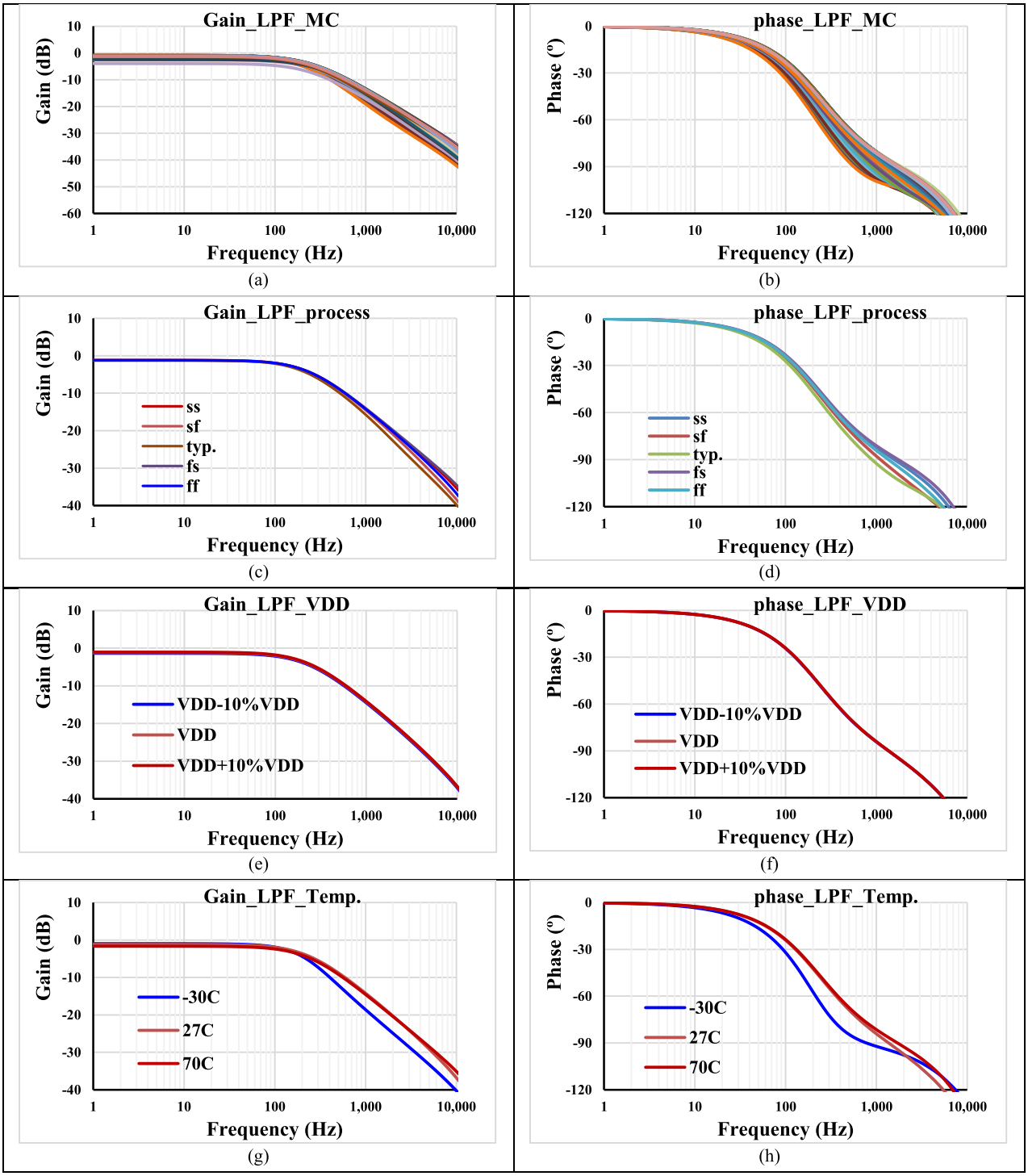

FIGURE 8. Frequency responses of gain and phase for LPF: (a,b) MC; (c,d) process corners; (e,f) voltage supply corners; (g,h) temp. corners.

and 57.29 mdB while the -3dB bandwidth is 22.24 kHz and 22.23 kHz, respectively. The simulated DC transfer characteristics of the DDCC shows rail-to-rail operation capability. The simulated gain and phase characteristics for the TA (without MI) and $I_{set} = 0.5\ \mu$A and 20 pF load capacitance shows that the low DC gain is 23.2 dB and the bandwidth is 19.65 kHz while the phase error is 3.8° [11]. The DC characteristic of the output current and the transconductance of the TA versus fully differential input voltage for $I_{set} = 0.125\ \mu$A, 0.25 μA, 0.5 μA confirms a rail-to-rail operation with high linearity. To the best of the authors' knowledge, this is the first VDDDA with the lowest supply voltage presented

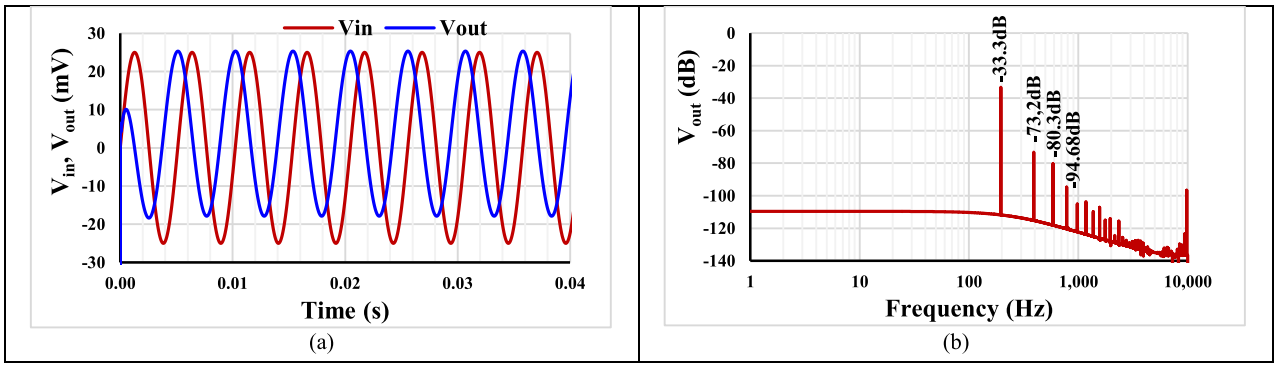

FIGURE 9. The transient response of the APF (a) and the spectrum of the V_{out} using FFT (b).

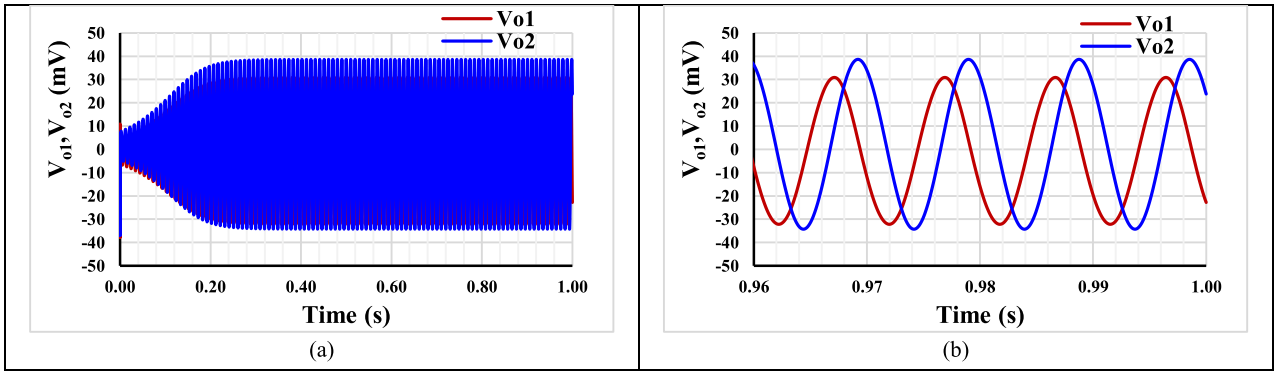

FIGURE 10. The running oscillation (a) and the steady state (b).

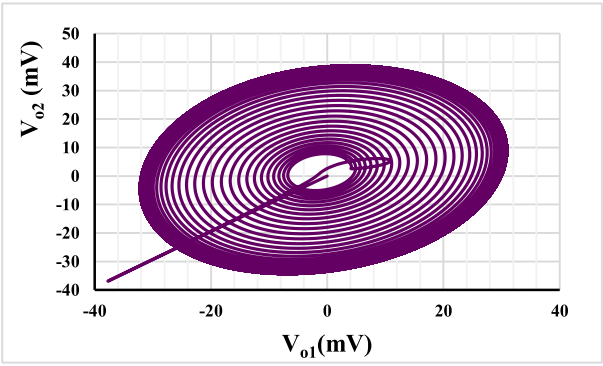

FIGURE 11. The quadrature relationship between V_{o1} and V_{o2}.

in the literature. Despite the extremely low supply voltage, the circuit offers rail-to-rail operation capability and high linearity.

The proposed voltage-mode first-order universal filter from Fig. 4 was simulated with $C_1 = 1$ nF and the setting current $I_{set} = 0.5$ μA ($g_m = 1.25$ μS). Fig. 6 shows the ideal and simulated filter gain and phase characteristics. The designed and simulated cut-off frequencies were very close i.e., 197.4 Hz and 195.6 Hz, respectively.

The electronic turnability of the filter is confirmed in Fig. 7. The gain and phase characteristics were repeated for $C_1 = 1$ nF and various $I_{set} = (0.125, 0.25, 0.5, 1)$ μA. The cut-off frequency was (50, 100, 195.6, 332) Hz, respectively.

The filter performance was evaluated under varying process and mismatch conditions using Monte Carlo (MC) analysis and under the effects of process, voltage, and temperature (PVT) corners. Fig. 8 shows the gain and phase characteristics of the LPF for $C_1 = 1$ nF and $I_{set} = 0.5$ μA, with: (a,b) 200 runs Monte Carlo analysis; (c,d) process slow-slow (ss), slow-fast (sf), fast-slow (fs) and fast-fast (ff); (e,f) voltage supply corners $V_{DD} \pm 10\%V_{DD}$; (g,h) temperature corners -30°C and 70°C. As it is evident, the curves are almost overlapped, ensuring reliable operation under the range of the operating conditions. The slight deviation in the temperature corners analysis is expected due the operation in weak inversion that is sensitive to temperature variation.

The transient response of the APF with $C_1 = 1$ nF and setting current $I_{set} = 0.5\mu$A is shown in Fig. 9 (a). The input of the filter V_{in} was supplied by a sine wave signal with 50 mV_{pp}@ 195 Hz. Fig. 9 (b) shows the spectrum of the output signal V_{out} using Fast Fourier Transform (FFT). The total harmonic distortion of V_{out} was found to be -39.09 dB (1.1%).

To start the oscillation of the oscillator in Fig.5, the following values were selected: capacitors $C_1 = C_2 = 1$ nF, the setting current $I_{set2} = 0.5$ μA, and $I_{set1} = 0.22$ μA. Fig. 10 (a) and (b) shows the running oscillation and steady

TABLE 3. Comparison of the proposed first-order filter and some previous works.

Features	Proposed	[38] 2021	[40] 2022	[44] 2022	[50] 2023	[52] 2023
Active and passive elements	1 VDDDA, 1 C	1 LT1228, 1 C, 2 R	2 CFOA, 1 C, 4 R	2 CFOA, 1 C, 4 R	1 VGA, 1 R, 1 C	2 OTA, 1 C
Realization	CMOS structure (0.13 μm)	Commercial IC (LT1228)	CMOS structure (0.18 μm)	Commercial IC (AD844)	CMOS structure (0.18 μm)	CMOS structure (0.18 μm)
Mode operation	VM	VM	VM	VM	MM	VM
Type of filter	MISO	MISO	SIMO	MISO	MIMO	MISO
Number of filtering functions	6 (LP+, LP-, HP+, HP-, AP+, AP-)	4 (LP+, HP+, AP+, AP-)	3 (LP+, HP+, AP+)	3 (LP-, HP+, AP+)	3 VM (LP+, HP+, AP+)	6 (LP+, LP-, HP+, HP-, AP+, AP-)
High-input & low-output impedances	Yes & Yes	No & Yes	Yes & No	Yes & Yes	No/Yes (VM)	Yes & No
Electronic control of parameter ω_o	Yes	Yes	No	No	Yes	Yes
Using grounded capacitor/resistor	Yes/Yes	No/No	Yes/No	Yes/No	No/Yes	Yes/Yes
Pole frequency (kHz)	0.197	90	1591.5	159	1590	0.220
Total harmonic distortion (%)	1.1@50mV$_{pp}$	1@200mV$_{pp}$	1@200mV$_{pp}$	-	0.15@40mV$_{pp}$ (VM)	0.36@40mV$_{pp}$
Power supply voltages (V)	0.3	±5	±1.25	±12	±0.9	0.5
Power consumption (μW)	0.3574	57600	3910	-	1310	0.0595
Applications	QSO	QSO	QSO	-	QSO	High-Q BPF
Verification of result	Sim.	Exp.	Sim./Exp.	Exp.	Sim/Exp	Post-layout Sim

Note: QSO = quadrature sinusoidal oscillator, High-Q BPF = high-Q bandpass filter, MISO = multiple-input single-output, SIMO = single-input multiple-output, MIMO = multiple-input multiple-output.

state of the oscillator, respectively. The THDs were around 0.8%. The outputs V_{o1} and V_{o2} were in quadrature with a frequency of 103 Hz. Fig. 11 shows the relation between V_{o1} and V_{o2} that confirms the quadrature relationship of the output signals.

Table 3 shows the comparison of the proposed first-order filter with some previous works, namely the recent publications in [38], [40], [44], [50], and [52]. Compared to [38], [40], [44], and [50], the proposed filter can realize more transfer functions and offers both lower supply voltage and lower power consumption. Like [52], the proposed filter offers six transfer functions, but the filter in [52] uses two OTAs and does not provide low-output impedance. The circuits in [38] and [50] excite the input signal via the capacitor, which is not ideal for voltage-mode circuits. Compared to [40] and [44], the proposed filter has an electronic tuning capability. Finally, the proposed circuit operates with the lowest voltage supply of 0.3V.

V. CONCLUSION

This paper presents a universal 0.3 V voltage-mode first-order analog filter using a single multiple-input VDDDA. The CMOS structure of the MI-VDDDA is capable of operating at extremely low supply voltages without degrading circuit performance due to various design aspects. Thanks to the multiple-input technique, the first-order filter provides non-inverting and inverting low-pass, high-pass and all-pass filters in a single topology with high input and low output impedance. The filter circuit has been used to implement a quadrature oscillator. The robustness of the design is supported by intensive simulation results, such as MC and PVT corner analyses.

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