Educational Tool for the Demonstration of DfT Principles Based on Scan Methodologies

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Abstract

In the paper, the principles of Scan Educational Tool are presented. First, the motivation for this activity is briefly mentioned. Then, the structure of software package together with the principles of communicating and controlling the tools belonging to the system are explained. It is shown how the system can be utilized for testability analysis and design for testability demonstrations resulting in applying scan design principles in the design.

1. Introduction

For several years we have dealt with register transfer level (RTL) testability analysis [1, 4–9]. We have developed methodologies the goal of which is to analyze RTL component structure, evaluate the testability of internal components and suggest modifications of the circuit. We have also demonstrated that the problem of testability analysis can be converted into the problem of discrete mathematics [6, 7, 8]. For this purpose the model was defined, which allows to reflect structural and diagnostic properties of an RTL component by means of discrete mathematics concepts. Then, to analyze testability properties of an RTL structure, discrete mathematics algorithms can be used.

In the past, numerous methodologies based on enumerating controllability/observability factors were published. These factors are utilized in different heuristic approaches, the identification of registers through which the test will be applied is the result of implementing these methodologies. During the selection, the requirements of a designer or a test expert (design constraints) must be taken into account and satisfied, if possible. This process can be realized as a strictly heuristic approach in which different modifications are accepted and evaluated successively, and then the solution, which satisfies the requirements most is selected for implementation. We see that these procedures might be quite time consuming in certain situations and for certain RTL circuit structures, e.g. those with numerous feedback loops. Moreover, we feel that controllability/observability factors are not the only factors, which should be included into decision-making process the result of which is the selection of registers into *scan-chains*, i.e., *scan-layout*.

Scan approaches fall into two main groups: *full scan* and *partial scan*. In full-scan, all memory cells (e.g., flip-flops) within the circuit structure are included into scan. In partial scan, memory cells are selected into scan in such a way that the remainder of the circuit has certain desirable testability properties. This requires extra analysis of the circuit, but can lead to full-scan testability results for significantly lower price. Existing approaches for selecting registers for partial scan can be classified as *testability analysis based* [10], *test generation based* [11] and *structural analysis based* [12]. All of these techniques suggest testability modifications after the completion of the design and are incapable of suggesting behavioral modifications by identifying testability bottlenecks in the design behavior during the design process. Some methods exist, which are based on inserting test registers in order to obtain self-testable circuits [13], [14]. The methodologies are implemented in the way, which guarantees minimum hardware overhead [15]. In [16] an interesting method how to further utilize scan chains is demonstrated - they are used for pattern decompression. Several algorithms were developed to select partial scan FFs to break feedback cycles [17][18]. In [19] a methodology is described, which is able to take into account a number of technological constraints and determines the optimal order of FFs into the scan chains.

In our research we have concentrated on developing methodologies the goal of which is the enhancement of testability parameters [2] of given circuit for the lowest possible price. They result in

partial scan methodologies, based either on the structure analysis [20] or on the identification of feedback loops [3], [4]. Also, the identification of so-called testable cores, which satisfy predefined testability properties, was one of topics we have dealt with [1]. The application of such methodologies on RTL structures results in reducing the amount of diagnostic data transported through the circuit.

On our research both staff people and Ph.D. students participate. We felt that it might be reasonable to develop educational tools, which could be utilized by the members of the research team who join the team as beginners and are charged with a particular task from the area of research covered by the team. The *SET* (*Scan Educational Tool*) presented in this paper is a software tool, which allows to study the principles and possibilities of applying scan techniques in RTL digital circuits.

The paper is organized as follows. First the structure of SET is explained. Then, all the tools of SET are explained in detail together with the principles of communicating with the software.

2. The Structure the Tool

The SET software package consists of the following modules: (1) testability analysis module and of (2) an automated design for testability module. Through the Main window (Figure 1, the most left window), a user can select which of the modules will be utilized. The selected module is invoked by pressing the Run button. By checking proper checkboxes in the Main Window, following windows can be displayed on the screen:

- *Scan Layout Selection* (selection of registers into scan chains, i.e. scan-layout selection),
- *Testability Details* of educational circuit (impact of selecting registers into scan can be observed). Diffeq benchmark circuit [21] was selected to be used as the educational circuit (see Figure 1 and Figure 5),
- *Circuit Schema* (schema of educational circuit with depiction of selected scan-layout, diagnostics-data transportation paths of selected circuit elements etc.).

In the following text, the windows are described in more detail.

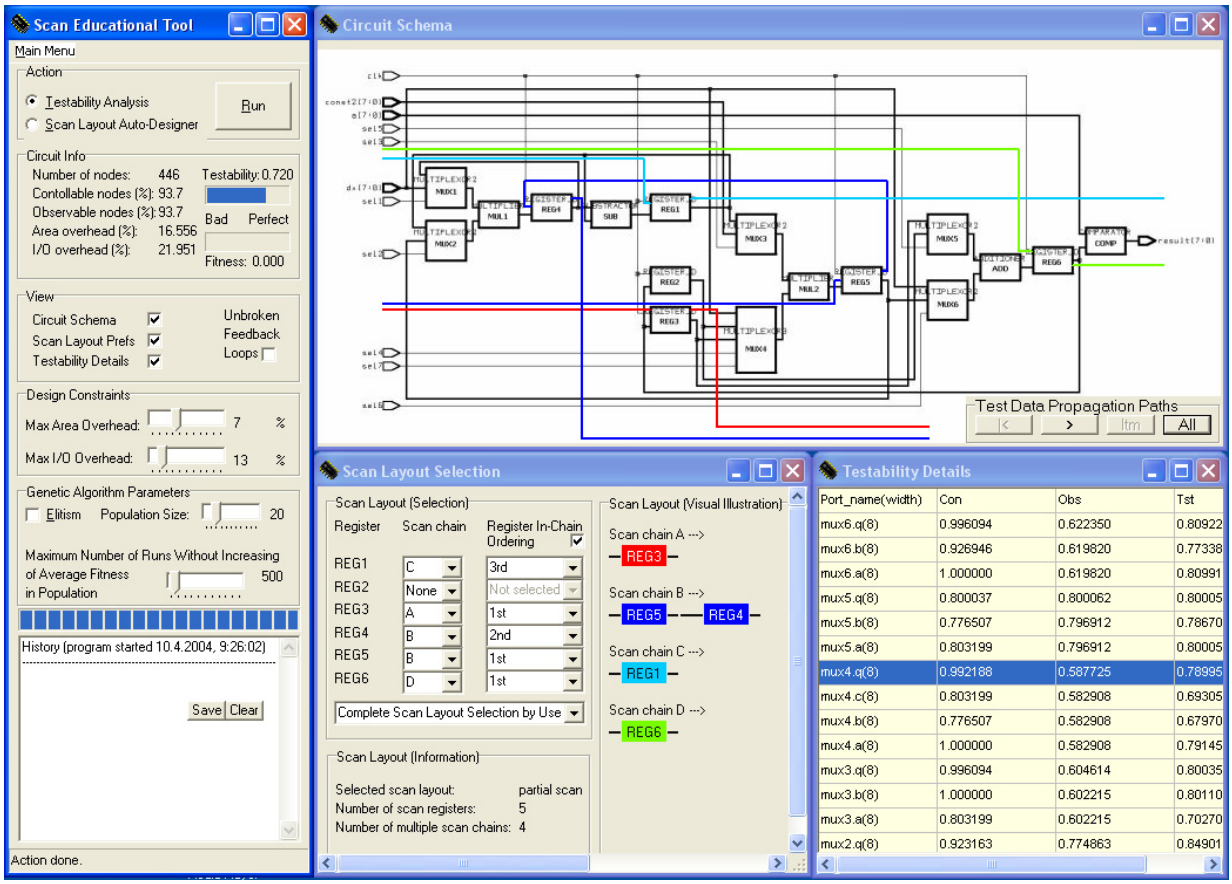


Figure 1. SET application windows

2.1 Scan Layout Selection Window

The purpose of module (1) is to perform, evaluate and display testability results of the educational circuit according to selected scan-layout. In the *Scan Layout Selection* window, user can select any combination of in-circuit registers into scan chains and consequently observe the impact of the selection on circuit testability parameters (checking *Testability Analysis* radio button in the *Main Window* and pressing the *Run* button). More detailed testability results can be seen after checking the *Testability Details* checkbox in the *Main Window*.

In the educational circuit, there are six registers available in total. They can be organized in scan chains in many ways. In Figure 2, snapshots of four various configurations set in the *Scan Layout Selection* window are presented. In the window, it is possible to set-up:

- which registers are to be included in scan chains,
- pre-defined organizations of registers in scan chains, e.g., special full scan variants,
- (random/user-selected) ordering of registers in particular scan chains.

In Figure 2a and Figure 2b it is depicted how it is possible to select the "Scan layout user-selection" mode. In the mode, a user can select his own configurations of registers in scan chains. As an example in Figure 2b, registers are selected to be included in scan chains in the following way (including ordering of registers within scan chains): REG1 is included into scan chain "A", REG4 and REG5 are included into scan chain "B" and REG4 (REG5) is the 1st (2nd) register in scan chain "B". As can be seen in Figure 2b-see Scan Layout (Information)-3 registers are included in two scan chains.

In Figure 2c, the following pre-selected "full scan" organization of registers within scan chains is selected: all six registers from educational circuit are included in scan chains in such a way that each register forms one scan chain. So, there are six registers (REG1-REG6) included in the scan chains and six scan chains ("A"-"F") in total. In Figure 2d, example of randomly generated scan-layout is presented. The layout consists of four scan chains; scan chain "A" consists of REG5, "B" of REG4 and REG2 (in this order), "C" of REG1 and "D" of REG3, so there are five scan registers in total.

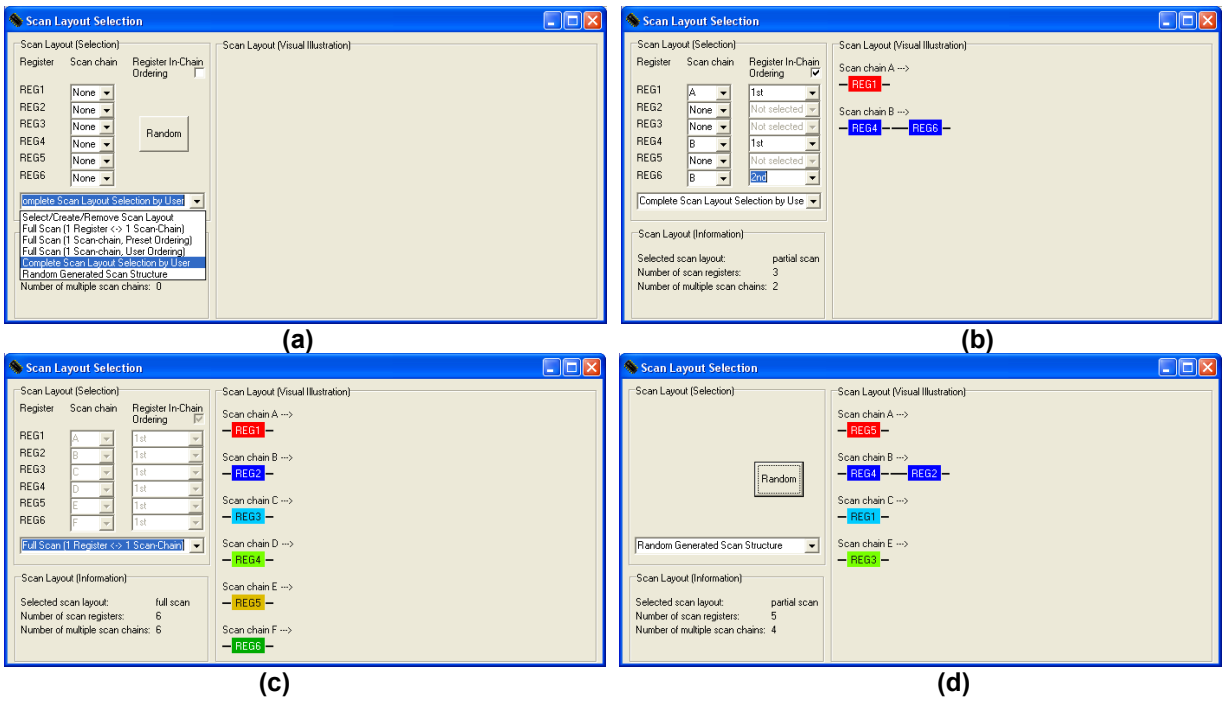
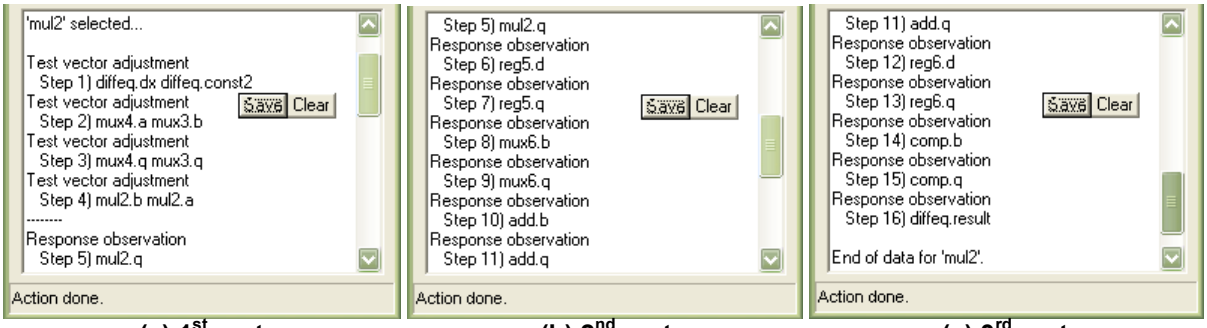


Figure 2. Snapshot of Scan Layout Selection windows

2.2 Testability Details Window

Evaluation of testability properties (results) of the original educational circuit structure and/or of the structure with selected scan-layout implemented can be observed in *Testability Details Window* (in Figure 4, snapshot of the window is depicted). In the window, the information about circuit data-path testability properties is presented. Each data port of in-circuit elements is assigned a triplet of real numbers evaluating its controllability (left number), observability (middle number) and testability (right number). At the end of the window, diagnostic attributes of the whole circuit are presented in two rows. In the top row, information about total number of data ports within the circuit is given (1st column from the left), then the number and ratio of controllable (2nd column from the left), observable (3rd column from the left) and testable (i.e., both controllable and observable, see 4th column from the left) data ports is given. In the bottom row, evaluation of circuit controllability (2nd column from the left), observability (3rd column from the left) and testability (4th column from the left) is presented.



(a) 1st part **(b) 2nd part** **(c) 3rd part**

Figure 3. Diagnostics data propagation paths for MUL2 key-points

2.3 Circuit Schema Window

In the Circuit Schema window, it is possible (after testability analysis is performed) to visualize diagnostics data (i.e., test vectors and responses) transportation paths for selected circuit element(s). Of course, the transportation is influenced by circuit testability, i.e., also by the selected scan layout. With a respect to the educational goal, only one way of transportation of test vectors and responses is selected by SET.

As an example, MUL2 is selected and its diagnostic data transportation paths are depicted in the Figure 5 while REG1 and REG6 are included in two separate scan chains. Together with the graphical visualization of transportation data paths in the Circuit Schema window, key-points of the paths are noted in the History (see Figure 3 for window snapshot) in the Main Window.

2.4 Design For Testability Mode

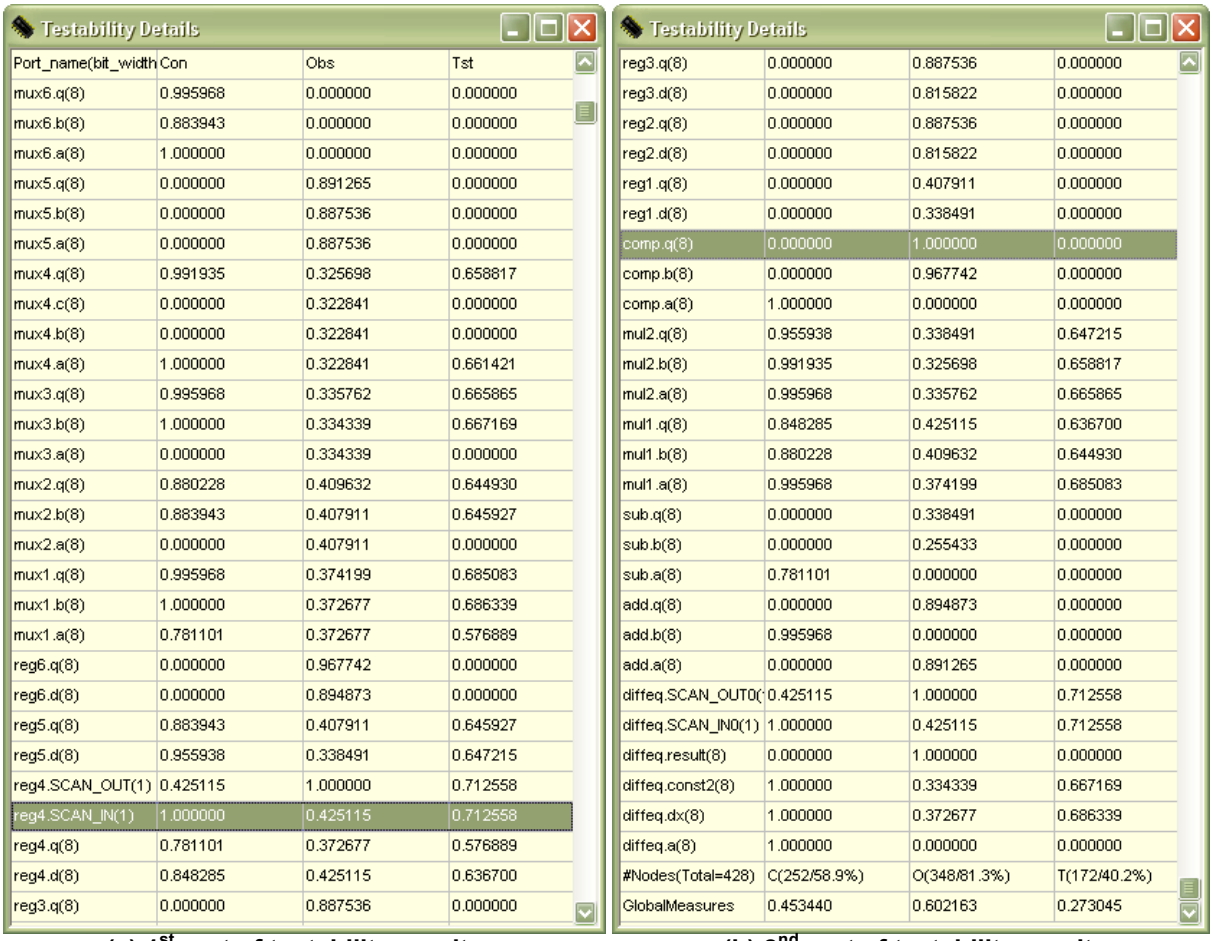
In Main Window, second module (2) can be selected by checking Scan Layout Auto Designer radio button first; then pressing the Run button. The goal of module (2) is to automatically find such a scan layout that meets selected design constraints (given in the Design Constraints section in the Main Window) the most. In the actual version of SET, only two design constraints can be set by the user: maximum area overhead and maximum input/output overhead. To find the scan layout, genetic algorithm is utilized – in the Genetic Algorithm part of the Main Window parameters of the algorithm can be modified to influence the searching process.

In design for testability methodologies different aspects (criteria) can be taken into account, which allow different solutions of the problem to be gained. As a result of such approaches, a subset of registers is identified through which the test will be applied. It is

supposed the registers will be converted to scan registers.

One possibility how to identify the set of registers for the test application process is by means of two steps: 1) enumerating all combinations of registers, which could possibly form the scan chain(s) and 2) evaluating every alternative. These approaches are usually denoted as "rough methods" (although they lead to acceptable solutions, they can be too much time consuming for the problem complexity). These methods are based on exhaustive search: they simply visit all points in the search space in some order and retain the best solution visited. Other methods only visit part of the search space, albeit the number of points visited may grow exponentially (or worse) with the problem size. To avoid this problem, it is possible to use general-purpose heuristics that do not guarantee an optimal solution.

During our research [5-8] it was demonstrated that registers for scan can be selected in the way which enables design constraints to be fulfilled maximally. The problem can be seen as the problem of state space investigation, the complexity grows exponentially with the number of registers in the circuit.



(a) 1st part of testability results **(b) 2nd part of testability results**

Figure 4. Snapshot of Testability Details window

Thus (as mentioned above), in our methodology, the evolutionary approach is represented by genetic algorithm, which performs a multidirectional search by maintaining a population of potential solutions (set of registers for scan). The population of registers for scan undergoes a simulated evolution from one generation to another: at each generation the relatively good solutions reproduce, while the relatively bad solutions die. The goodness or badness

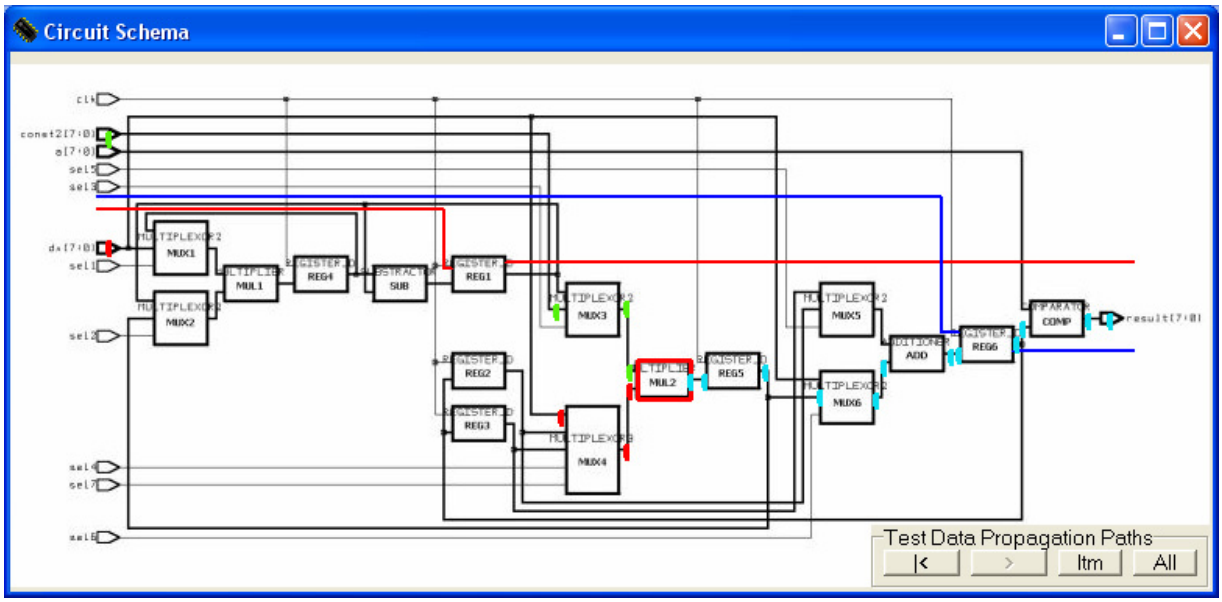


Figure 5. Circuit Schema window with diagnostics data propagation paths depicted for MUL2

of the solutions is defined by a cost function. Each solution is encoded as a chromosome, which is represented as a string of bits from a binary alphabet. To generate new solutions, crossover operation is used. For the crossover, two solutions S1 and S2 of the current generation of registers are selected and the chromosome to the new solution is produced. The new chromosome is the result of mixing a part of the chromosome of S1 with a part of that corresponding to S2. This means that the new solution inherits certain features of its two parent solutions. The mutation operator, on the other side, produces a small, random perturbation to a given solution (chromosome).

To determine the solutions, which are considered as parents for crossover operations, a selection scheme is used. An essential criterion at selection for crossover is the fitness of the solution defined by the cost function. Thus, selection of fit solutions for crossover ensures the propagation of high quality features into the next generation. The selection is based on a probabilistic scheme, which favors candidates having a high fitness. Producing several successive generations, the average fitness of the solutions is increasing. The algorithm is usually stopped after a certain number of iterations or when no further improvements are produced. The best solution that has been produced is that one, which is hopefully close to the optimum. To apply genetic algorithm to a problem, it is necessary to identify: (1) meaningful representation for the candidate solutions; (2) a fitness function to assess different solutions; and (3) a set of useful genetic operators, that can efficiently recombine and mutate candidate solutions.

The goal of the genetic algorithm is to utilize results provided by proposed testability analysis method in the following way: it was required to select registers into scan chains and to chain them in such a way that 1) design constraints posed on the final circuit will be fulfilled and 2) the highest testability of resulting design would be achieved together with the lowest price proportional to size of modifications caused by scan application in the original circuit structure.

In [3, 9], the problem of proper scan-layout selection is discussed together with scan-layout state-space analysis and a formal notation for scan-layout description. Using the notation, scan layout selected in the Scan Layout Selection window is written into History window after testability analysis is performed. Let the notation be summarized in brief by the following points: 1) scan chain is represented by a sequence of registers that are chained within the chain, 2) special character (period, dot) is used to separate particular scan chains, 3) if the ordering of scan registers within the scan chains is not important, registers belonging to the same scan chain are chained in the left-right direction according to increasing values of indexes (registers with higher indexes are placed on the right), 4) scan chains are ordered in a left-to-right way according to increasing index of the first register in a scan chain (scan chains with higher index of the first register are placed on the right), 5) if there is no register selected into scan, notation contains only the special character. As an example of

scan chains described by the notation, let us present $R_1R_2.R_5$ or $R_1R_4R_5.R_2.R_3.R_6$ (ordering of registers in scan chain is not important) and $R_2R_1.R_3$ or $R_1R_5R_4.R_3.R_2.R_6$ (ordering of registers in scan chain is important-registers are chained in the order as it is described in the notation).

The method for selection of registers into scan chains based on results of testability analysis takes as input the information on the circuit structure, the set of design for testability techniques to be used for testability improvement, diagnostic related requirements (e.g., desired fault coverage, test application time, number of testable nodes), design constraints (e.g., maximum area/pin overhead allowed) and selection of optimizing algorithm are used as an output. At the output, a modification of original circuit structure fulfilling desired diagnostic properties and design constraints maximally appears.

2.5 Supported Environments

In the full graphical user interface mode, SET runs as WIN32 application (EduSW.exe, see Figure 1), thus it should run on all WIN32-based operating systems (e.g., Win9x, WinXP). Also, SET can be run as an MS-DOS console application (dcta.exe, see Figure 6) – e.g. in the Command Prompt or MS-DOS emulation system in an UNIX environment. SET results are stored in several file-formats (ASCII, LaTEX, HTML) to be easily presented in most frequently used publishing systems.

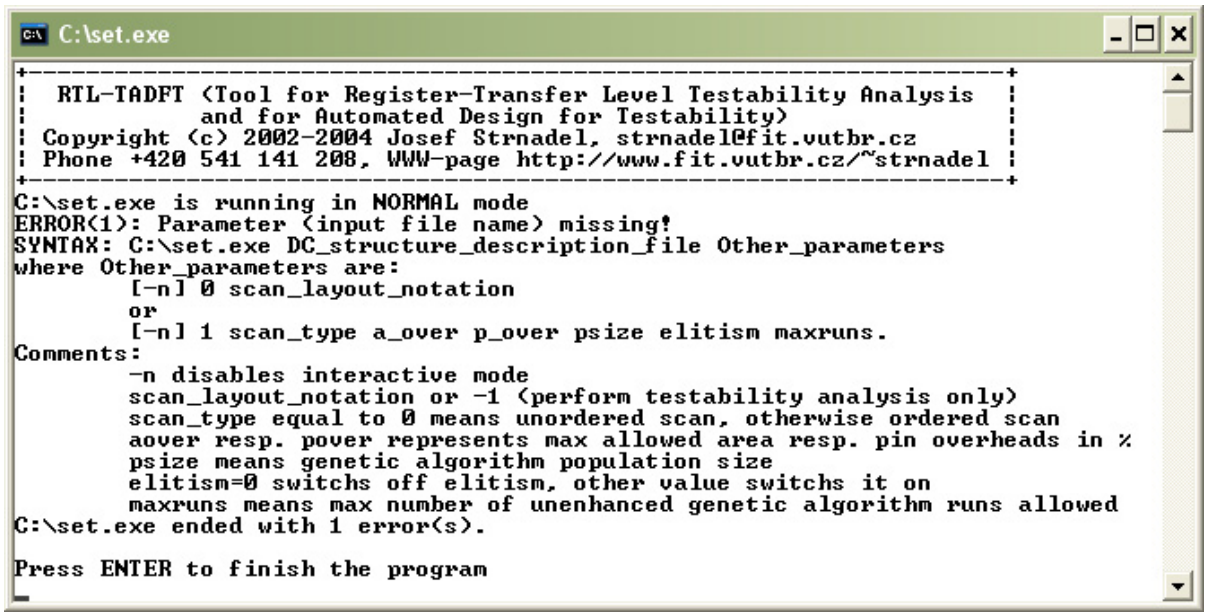


Figure 6. Snapshot of SET as an MS-DOS Console Application

3. Conclusions

The educational tool is utilized both by PhD students and undergraduate students studying at our department. It will be appreciated if it is utilized not only by them but by other researchers as well. The latest SET version, bug fixes, actualized documentation, examples etc. can be downloaded from *www.fit.vutbr.cz/~strnadel/diag/downloads* page. We shall be grateful for comments or the recommendations how to improve the software.

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References

[1]Kotásek, Z., Pečenka, T., Strnadel, J.: Improving Testability Parameters of Pipelined Circuits

Through the Identification of Testable Cores, In: Proc. of the 7th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Bratislava, SK, SAV, 2004, p. 99 - 104

[2]Kotásek, Z., Mika, D., Strnadel, J.: Methodologies of RTL Partial Scan Analysis and Their Comparison, In: Proceedings of IEEE Workshop on Design and Diagnostic of Electronic Circuits and Systems, Poznaň, PL, UNI-DRUK, 2003, pp. 233–238

[3]Strnadel, J.: Algebraic Analysis of Feedback Loop Dependencies in Order of Improving RTL Digital Circuit Testability, In: Proceedings of IEEE Workshop on Design and Diagnostic of Electronic Circuits and Systems, Poznan, PL, UNI-DRUK, 2003, pp. 303–304

[4]Strnadel, J.: Nested Loops Degree Impact on RTL Digital Circuit Testability, In: Programmable Devices and Systems, Oxford, GB, Elsevier, 2003, pp. 202–207

[5] Kotásek, Z., Růžička, R., Strnadel, J.: Formal and Analytical Approaches to the Testability Analysis - the Comparison, In: Proceedings of IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop 2001, Gyor, HU, SU, 2001, p. 123-128

[6]Strnadel, J., Kotásek, Z.: Testability Improvements Based on the Combination of Analytical and Evolutionary Approaches at RT Level, In: Proceedings of Euromicro Symposium on Digital System Design Architectures, Methods and Tools DSD'2002, Los Alamitos, ICSP, 2002, pp. 166–173

[7] Strnadel, J.: Testability Analysis and Improvements of Register-Transfer Level Digital Circuits, PhD thesis, Brno University of Technology, Brno, 2004, p. 150

[8]Strnadel, J.: Scan Layout Encoding by Means of a Binary String, In: Proceedings of 37th International Conference on Modelling and Simulation of Systems, Ostrava, CZ, MARQ, 2003, pp. 115–122

[9]Hlavička, J., Kotásek, Z., Růžička, R., Strnadel, J.: Interactive Tool for Behavioral Level Testability Analysis, In: Proceedings of the IEEE ETW 2001, Stockholm, SE, 2001, pp. 117–119

[10] Agrawal, V. D., Cheng, K., Johnson, D. D., Lin, T.: A Complete Solution to the Partial Scan Problem, Proceedings of the 1987 International Test Conference, September 1–3, 1987, Washington, pp. 44–51

[11]Higami, Y., Kajihara, S., Kinoshita, K.: Partial Scan Design and Test Sequence Generation Based on Reduced Scan Shift Method, Journal of Electronic Testing: Theory and Applications, 7, Kluwer Academic Publishers, 1995, pp. 115—123

[12] Flottes, M. L., Pires, R., Rouzeyre, B., Volpe, L.: A Fast and Effective Technique for Partial Scan Selection at RT Level, Proc. of IEEE ETW 1997, May 28--30, 1997, Cagliary, Italy, pp. 36–42

[13]Abadir, M.S., Breuer, M.A.: A Knowledge-Based System for Designing Testable VLSI Chips, IEEE Design & Test of Computers, Vol. 2, No. 3, 1985, pp. 56–68

[14]Stroele, A. P., Wunderlich, H. J.: Hardware-Optimal Test Register Insertion, IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, vol. 17, No. 6, 1998, pp. 531–539

[15]Stroele, A. P., Wunderlich, H. J.: Test Register Insertion with Minimum Hardware Cost, Proc. ICCAD 95, San Jose, California, USA, pp. 95–101

[16]Dorsch, R., Wunderlich, H. J.: Reusing Scan Chains for Test Pattern Decompression, Proc. ETW 2001, Stockholm, May 2001, pp. 307–315

[17]Chakradhar, S. T., Balakrishnan, A., Agrawal, V.: An Exact Algorithm for Selecting Partial Scan Flip-Flops, Journal of Electronic Testing: Theory and Applications, 7, 1995, pp. 83–93

[18]Orenstein, T., Kohavi, Z., Pomeranz, I.: An Optimal Algorithm for Cycle Breaking in Directed Graphs, Journal of Electronic Testing: Theory and Applications, 7, 1995, pp. 71–81

[19]Barbagallo, S., Bodoni, M. L., Medina, D., Corno, F., Prinetto, P., Reorda, M. S.: Scan Insertion Criteria for Low Design Impact, IEEE VLSI Test Symposiun, Princeton, April 1996, pp. 26–31

[20] Kotásek, Z., Mika, D., Strnadel, J.: The Identification of Registers in RTL Structures, In: Preliminary Proceedings of 1st International Symposium on Leveraging Applications of Formal Methods ISOLA 2004, Nicosia, CY, DCS UC, 2004, pp. 317–320

[21] Paulin, P. G., Knight, J. P., Girzyc, E. F.: HAL: A Multi-Paradigm Approach to Automatic Data-Path Synthesis. In: Proceedings of the Design Automation Conference, 1986, pp. 263–270