Power Conscious RTL Test Scheduling

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Abstract

This presentation is based on our recently published paper [1]. In that paper we combined the testability analysis based on partitioning into testable blocks (TBs) with the optimization for low power consumption and power conscious RTL test scheduling.

Our methodology can be divided into several steps: At first the circuit under analysis (CUA) is mapped onto AMI technological library. Then the CUA is partitioned into TBs. For each TB the test vectors are generated with commercial tool and whenever possible reordered for power consumption reduction. As a power consumption metric we use the number of transition count (NTC) during the test application. Because of large solution space of the reordering problem ($n!$, where n is number of test vectors) we utilize genetic algorithm in the process. The population of genomes consists of bit strings. In each bit string the ordering of test vectors is encoded. The fitness value is obtained as the overall NTC value from the test application simulation over the AMI primitives. Due to the high number of genomes the fitness must be determined as quickly as possible, that is why we prefer the NTC metrics. While most of the methods which aim at power reduction during the test application are based on evaluation of the average Hamming distance of test vectors, our approach is closely combined with the AMI platform that renders more accurate results. Also when dealing with small partitions of original circuit instead of overal flat design the size of solution space can be reduced significantly, which adds another advantage to our approach.

Finally, the TBs are utilized for power constrained test scheduling. The goal is to find the test schedule with the lowest test application time that simultaneously does not exceed the allowed chip power dissipation limit. We formulate the test scheduling problem as an integer linear programming (ILP) model. The ILP model defined in this way can be easily converted into GNU MathProg modeling language and then solved by means of GNU linear programming kit.

References

1. Škarvada J., Kotásek Z., Herrman T.: Power Conscious RTL Test Scheduling, In: Proceedings of 11th Euromicro Conference on Digital Systems Design Architectures, Methods and Tools, Parma, Italy 2008, pp. 721–728, ISBN 978-0-7695-3277-6