Behavior of CMOS Polymorphic Circuits in High Temperature Environment

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***Abstract*—The paper describes a series of experiments performed with the aim to analyze the fundamental impact of high temperatures on behavior of polymorphic digital circuits. These experiments were conducted using a reconfigurable polymorphic chip REPOMO32 which is configured (in addition to the configuration bit stream) using the level of power supply voltage (V_{dd}). Experiments show that polymorphic gates in the chip can be easily involved (in terms of functionality) not only by V_{dd}, but also by temperature. Because experiments also prove that the physical design of the REPOMO32 chip is robust enough to keep the functionality of all circuitry of the REPOMO32 and its dynamic parameters are stable enough under wide range of operating temperature, the chip can also be used for future designs of digital polymorphic circuits controlled by temperature.**

I. Introduction

In order to obtain reconfigurable and thus potentially adaptive circuits for a very low cost and without the need to implement a reconfiguration infrastructure (such as switches, multiplexers, configuration registers etc.) designers proposed *multifunctional gates* controlled by various means. In 2001, researchers at NASA JPL introduced polymorphic electronics where new electronic components – CMOS-based *polymorphic gates*–were able to perform several logic functions as response to various V_{dd} levels or temperature [1], [2], [3]. Recently, Sung and his colleagues at IBM T. J. Watson Research Center introduced a novel graphene reconfigurable logic device based on the control of p-n doping configurations using split gates [4]. By using split gates to change the grapheme properties, multi-function logic gate was obtained and dynamically reconfigured. This kind of devices will offer new ways for implementation of electronic components.

In our previous work, we developed and fabricated a reconfigurable polymorphic chip called REPOMO32 (REconfigurable POlymorhic MOdule) [5]. The aim was to recognize potential advantages and drawbacks of real polymorphic electronics as all previous works in the area of gate-level polymorphic circuits have been performed using simulators only. REPOMO32 consists of 32 two-input Configurable Logic Elements; each of them can be programmed to perform either AND, OR, XOR or polymorphic NAND/NOR logic function. As REPOMO32 contains polymorphic gates its behavior is not defined by the configuration bit stream solely. It also depends on the level of power supply voltage. When V_{dd} = 3.3V the NAND/NOR gates exhibit the NOR function and when V_{dd} = 5V the gates exhibit the NAND function. Remaining gates do not change their logic functions with the changes of V_{dd} (for V_{dd}=3–5 V).

The REPOMO32 chip was embedded to the REPOMOkit which is a board developed for testing of polymorphic circuits. We investigated the effect of reconfiguration by means of V_{dd} on the power consumption, delay, switching properties and other characteristics of polymorphic circuits [6]. One of conclusions was that the maximum operation frequency of the NAND/NOR gate strongly depends on a particular mode of the NAND/NOR gate, i.e. on V_{dd}.

The goal of this paper is to present a detailed analysis of REPOMO32 behavior in high temperatures. No similar work has been reported with fabricated polymorphic circuits so far. The only research which deals with temperature-controlled polymorphic gates was performed using simulators and the Field Programmable Transistor Array FPTA-2 [1]. The experiments will be conducted using REPOMOkit. In particular, we will show the polymorphic circuit response to rising and high temperature exposure. During this experimentation, we will evaluate behavior of polymorphic as well as ordinary gates available inside the chip together with their dynamic parameters under various temperatures. Some of these experiments will also be repeated on several chips to discover the differences caused by the fabrication process.

The paper is structured as follows. Section II briefly summarizes the recent work in the field of polymorphic electronics. Section III describes results of measurements performed on REPOMO32 using REPOMO32kit. Finally, conclusions are given in Section IV.

II. Polymorphic Electronics

A. Polymorphic Gates

Table I surveys the polymorphic gates reported in literature. For each polymorphic gate, the logic functions performed by the gate are given together with the values that represent recommended setting of the control signal variable. The number of transistors characterizes the size of polymorphic gates only partially as the transistors occupy different areas and the gates were fabricated using different fabrication technology. Only two of the polymorphic gates have been fabricated so far; remaining polymorphic gates were either simulated or

tested in a field programmable transistor array (FPTA-2). For instance, the 6-transistor NAND/NOR gate controlled by V_{dd} was fabricated in a 0.5-micron HP technology [3]. Another NAND/NOR gate controlled by V_{dd} and introduced in [7] was utilized in the REPOMO32 chip [5].

TABLE I
EXISTING CMOS POLYMORPHIC GATES

Gate	control values	control	transistors	ref.
AND/OR	27/125°C	temperature	6	[1]
AND/OR/XOR	3.3/0.0/1.5V	ext. voltage	10	[1]
AND/OR	3.3/0.0V	ext. voltage	6	[1]
AND/OR	1.2/3.3V	V_{dd}	8	[2]
NAND/NOR	3.3/1.8V	V_{dd}	6	[3]
NAND/NOR/NXOR/AND	0/0.9/1.1/1.8V	etx. voltage	11	[8]
NAND/NOR	5/3.3V	V_{dd}	8	[7]

Other polymorphic gates were developed whose logic function can be controlled by an external logic signal. For example, Ruzicka [9] proposed NAND/XOR gate which performs the NAND function when the external signal is connected to logic Low level, and the XOR function when the external signal is connected to logic High level. Since the external signal is the third logic input of the gate, we can consider these polymorphic gates as special instances of three-input gates. The main advantage of these gates is that they can be implemented as standard complementary CMOS structures. As these implementations are optimized for area, they contain fewer transistors than the structures based on multiplexing ordinary gates.

The problem of polymorphic circuit synthesis (at the gate level) can be considered as a more complicated version of the conventional digital circuit synthesis problem. The problem was initially formulated by Sekanina [10] and then further developed in [11], [12]. Other theoretical foundations of polymorphic electronics such as the completeness theory were presented in [13], [14].

B. Polymorphic Circuits and Their Applications

Polymorphic circuits are multifunctional circuits. The change of their behavior comes from modifications in the characteristic of components (e.g. in a transistors operation point) involved in the circuit in response to controls such as temperature, power supply voltage, light, a special signal etc. The change of circuit function can be recognized as a kind of reconfiguration.

In the field of polymorphic circuits, the reconfiguration lies in changing of the function of elementary building block rather than changing of the structure. In fact, the structure of such circuit (how elements of the circuit are connected together) always remains unchanged. This is the main difference between polymorphic electronics and classic reconfiguration. When the polymorphic circuit is designed carefully, the reconfiguration process is instantaneous (no configuration bitstream upload is necessary)! In addition, polymorphic electronics produces compact and space-efficient solution (polymorphic gates are type of compact design themselves). On the other hand, compactness and space-effectiveness is often achieved at the expense of slightly higher power consumption. But on the other hand, polymorphic electronics can be understood as a new reconfigurable technology which is capable to integrate sensing with logic to a single compact structure and enables the design of novel smart adaptive systems on silicon.

Research papers indicate many areas in which polymorphic gates could be utilized. The following list provides some examples:

- Implementation of low-cost reconfigurable/adaptive systems that are able to adjust their behavior inherently in response to certain control variables (e.g., the change of FIR filter behavior when a power supply is not sufficient [15] or multifunctional counters [8], [9]).
- Implementation of novel concepts for testing and diagnosing of electronic circuits (e.g., self-checking adders [7] and reduction of test vector volume [11], [18]).
- Implementation of a hidden function, invisible to the user, which can be activated in a specific environment (proposed in [1], [2]).
- Intelligent sensors for biometrics, robotics and industrial measurement (proposed in [1], [2]).
- Reverse engineering protection (proposed in [1], [2]).

C. REPOMO32

REPOMO32 is primarily intended for implementation of polymorphic four-input/four-output combinational circuits [5]. As Figure 1 shows the chip consists of 32 two-input Configurable Logic Elements (CLEs) organized in an array of 4 rows and 8 columns. A CLE can be programmed to perform one of the following functions: AND, OR, XOR and polymorphic NAND/NOR (controlled by V_{dd}). REPOMO32's logic behavior is defined by its configuration bits and the level of V_{dd}. The configuration bits control a set of multiplexers which are responsible for interconnecting the CLEs and selecting their logic functions. In total, 8 bits define the configuration of a single CLE. The configuration of the chip is stored in 32 8-bit latch registers. The configuration of a single CLE is performed by supplying CLE's address (*addr*) and configuration data (*data*) followed by activating the WE signal. The chip can be completely reconfigured in 32 configuration steps. The primary outputs $Z0 \ldots Z3$ are connected directly to CLEs of the last column. There are no synchronization registers in REPOMO32. The chip has 28 pins and occupies the area of 2900 x 1970 μm. It was fabricated using AMIS CMOS 0.7 μm technology.

D. REPOMOKit

A REPOMO32/kit is a dedicated experimental board which has been designed with the aim to conveniently facilitate test, evaluation and measurement procedures of all the features available inside the REPOMO32 chip [6]. This evaluation platform contains a DIL-28 socket for an integrated circuit with polymorphic gates (REPOMO32 chip), which may be configured by means of external switches or signals. A set of fast buffers is deployed in order to separate available input ports from the surrounding environment. The REPOMOKit

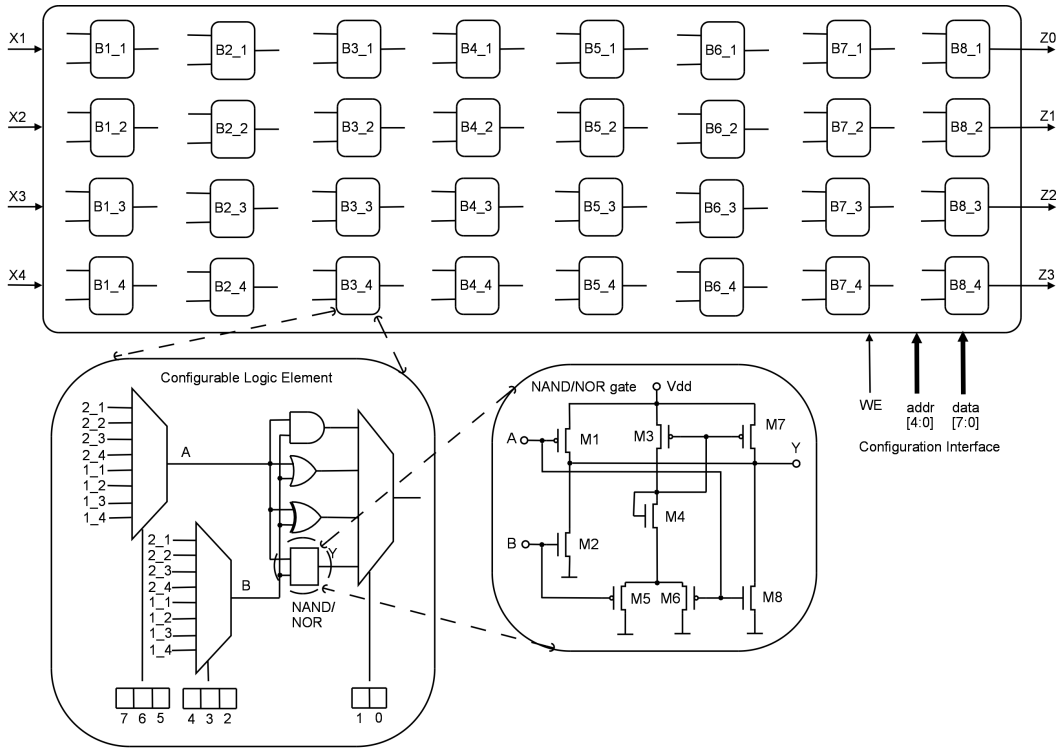

Fig. 1. The REPOMO32 chip shown together with the implementation details of the CLE block and NAND/NOR gate

also contains a Xilinx XC9572XL CPLD which may be used as a configuration controller for REPOMO32 or to customize an additional application-specific logic.

A special attention has been paid to the power generation and distribution across the board. Flexible power system is virtually divided into several independent branches, which deliver power supply within a range of 3.3V - 5V to the individual components onboard. It consists of dedicated rails for on-board auxiliary logic and a set of programmable power sources for the REPOMO32 chip itself. For example, the user may choose between stabilized 3.3/5 V voltage in either manual way or by means of using a signal from external controller or logic. Another feasible alternative how to obtain V_{dd} is based on using programmable power supply, which makes it possible to generate an eligible level of the output voltage within the range of 3.3–5 V. A digital potentiometer and integrated microcontroller are employed for this task.

The experimental platform REPOMO32 kit is equipped with a number of technical elements that can be harnessed throughout the procedure of REPOMO32 polymorphic chip thermal analysis. One of them, which has the major importance for this purpose, is undoubtedly dedicated heated chamber. This specific installation helps to create unique kind of working environment, where the temperature may reach up to 150 °C. The whole conception is based around metal box with dimensions of 76mm x 48mm x 19mm (length x width x height). Spiral heating wire is placed inside this tightly enclosed space where it is responsible for heat generation task. Necessary energy for the process of thermal management is delivered by an external source (12 V with maximum current of 1.5 A). An adequate shielding of this heated chamber ensures that the eventual temperature effects on functionality of other components on REPOMO32 kit are minimized to high degree. The parameters of a concrete thermal analysis test are fully configurable (e.g. duration of heating phase, specific temperature, regulation hysteresis). The whole procedure is subsequently managed by an 8-bit MCU, in particular MC9S08QE8 manufactured by Freescale. Its tasks include processing of test parameters, temperature measurement with sensor ADT7301 and heating regulation by means of switching power to the spiral heating wire. Temperature measurement can be carried out with a resolution of 0.03125 °C, which is more than sufficient for the character of REPOMO32 chip thermal analysis.

III. Experiments and Results

The ultimate goal of experiments, described in this paper, was to examine in detail the behavior of REPOMO32 chip (in particular, polymorphic gates built inside the chip) when exposed to wide range of diverse temperatures. Because the chip design procedure adhered to strict guidelines, we do not expect any serious malfunction to take place. However, the attention will be focused on eventual alterations to the propagation delay (maximal frequency) and perhaps to the polymorphic gates function switching. Dedicated heated chamber of REPOMO32 kit allows to put the polymorphic chip into operative environment where the temperature may reach up 150°C.

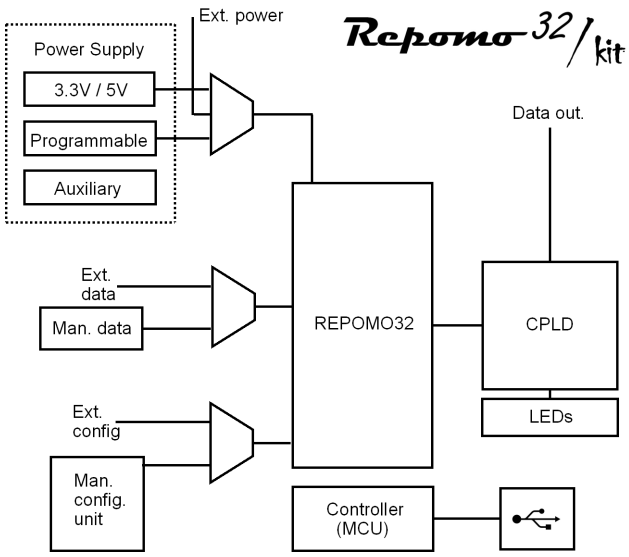

Fig. 2. REPOMO32 Evaluation Kit

A. The Impact of Temperature on Function of Polymorphic Gates

The first experiment involved slow, continuous heating phase from 25 °C up to 140 °C. The REPOMO32 chip was programmed in such way that it performed simple NAND/NOR function (CLE B1_1 performs polymorphic function while all others are configured as ANDs, i.e. work as pass-through). If polymorphic gate inside the REPOMO32 chip adopts the NAND mode (V_{dd} is greater than approximately 4 volts), its function is not affected by temperature. Polymorphic gate certainly performs the NAND function throughout the whole range of temperatures specified above. Nevertheless, another situation occurs when the function of polymorphic gate is selected as NOR mode (V_{dd} is below 4 volts). In this mode, the gate changes its function when chip temperature exceeds certain level. When the temperature of the chip ascends, the gate changes its function from NOR to the NOT B function. But few degrees up, the function changes again from NOT B to NAND. Note that the behavior of the gate exposed to rising temperature is similar to the behavior of the gate when the V_{dd} is rising [7] (with exception of the NOT B mid-function stage). After the chip cools down, the function switches back to the NOT B and NOR. There exist some hysteresis when the function changes from NOR to NAND and back. The hysteresis is mainly caused by thermal capacity of the chip and package and probably also partially by the embedded hysteresis of the gate itself [7].

In Figure 3 a transition from NOR to NOT B function of the polymorphic gate during the rise of temperature is shown. It can be seen that instead of 1s expected output Y when input is 00 (which is typical for the NOR function), another 1 occurs between them for 10 at input — see gray circle in Figure 3. This peak is not yet stable and does not last through the whole period when inputs are assigned stable binary value 10.

In Figure 4, another kind of polymorphic gate function

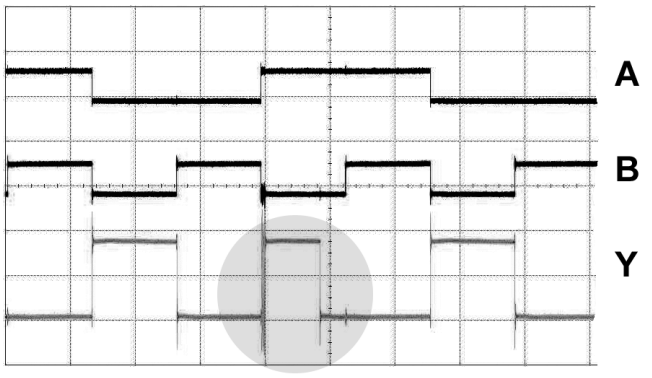

Fig. 3. Function transition of the polymorphic gate from NOR to NOT B function at about 125°C

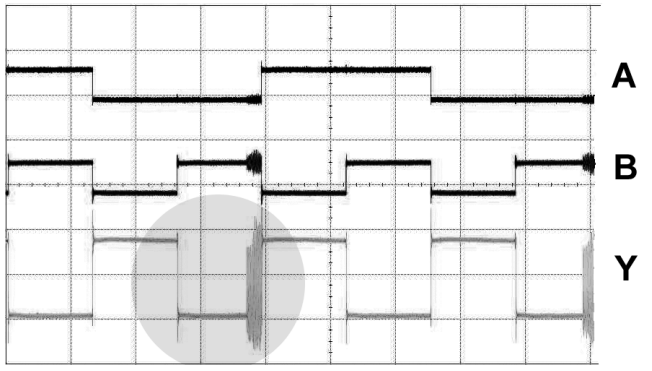

Fig. 4. Function transition of the polymorphic gate from NOT B to NAND function at about 135°C

transition is provided. This time, the temperature is rising a bit higher than in previous case. The resulting effect brings another change, from NOT B to NAND function. In the gray circle, it can be observed that another occurrence of binary 1 is shown up at the output. Besides 1s on the output Y for combination of 00 and 10 at the logic inputs AB, another logic 1 will appear soon within the area highlighted by grey circle. When this change finally takes place, the gate will exhibit NAND logic function.

The thermal point, when the gate reverts the actual function, has also close relation to V_{dd}. As the V_{dd} is approaching the function toggle point under normal temperature (slightly below 4 volts), the change of function happens to show up at lower values of temperature. Table II and Figure 5 demonstrate the effect of thermal point variation with V_{dd} level. It can be clearly observed that thermal sensitivity of gates in the REPOMO32 chip may be adjusted by means of V_{dd}.

Note that values in Table II are typical values of temperature in which the polymorphic gates in the chip changes their function. Five particular pieces of the REPOMO32 were examined during this experiment and thermal points, when gates inside change their function, vary for about $+/-2$°C.

The behavior depicted in Figure 5 means that the REPOMO32 chip can be used also as a polymorphic chip sensitive to temperature. Such purpose assumes the following

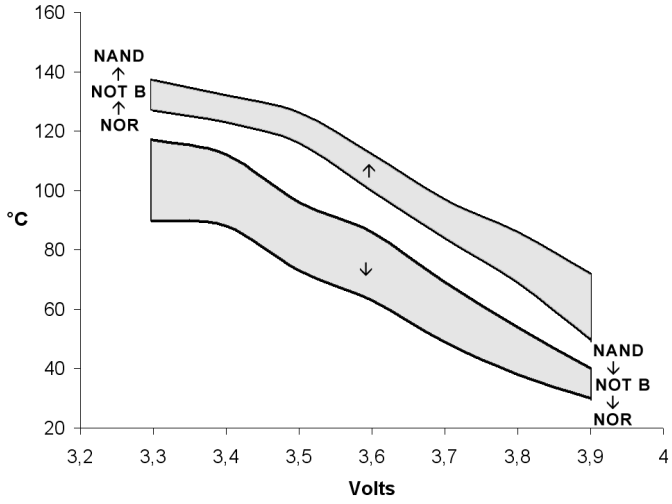

Fig. 5. Function switching temperature vs. Vdd

aspect to hold: function of other gates and circuitry of the chip, except polymorphic gates, must not be affected when the chip enters the environment with higher temperature. Experiments have provided doubtless evidence that the REPOMO32 chip fulfils this requirement.

TABLE II
FUNCTION SWITCHING TEMPERATURE VS. V_{dd}

Vdd	NOR to NOT B	NOT B to NAND	NAND to NOT B	NOT B to NOR
3.3	127°C	137°C	117°C	90°C
3.4	123°C	132°C	112°C	88°C
3.5	116°C	126°C	96°C	73°C
3.6	100°C	112°C	86°C	63°C
3.7	84°C	97°C	69°C	49°C
3.8	69°C	86°C	54°C	38°C
3.9	50°C	72°C	40°C	30°C

B. The Impact of Temperature on Dynamic Characteristics

The second experiment was performed to examine how dynamic characteristics of the REPOMO32 chip depend on temperature. Dynamic characteristics of the chip under normal temperature were already investigated and published in [6]. Previous experiments with polymorphic gates show that the transportation delay t_{pd} of a polymorphic gate is V_{dd} dependent. Table III shows length of one particular critical path in the REPOMO32 chip from input X1 to the output of the B4_1 CLE, where B1_1 is configured as polymorphic and B2_1 – B4_1 are ordinary ANDs (see Figure 1 and [5]). The experiment was performed on four particular REPOMO32 chips. Results show that the length of critical path t_{pd} (a delay of the signal between an input and output) is almost constant to more than 100 °C (for some pieces to more than 120 °C). After this limit, t_{pd} rises significantly. It means that the chip goes slower for high temperatures. This behavior is clearly depicted in Figure 6. Any dependency between polymorphic gate function change (affected by temperature)

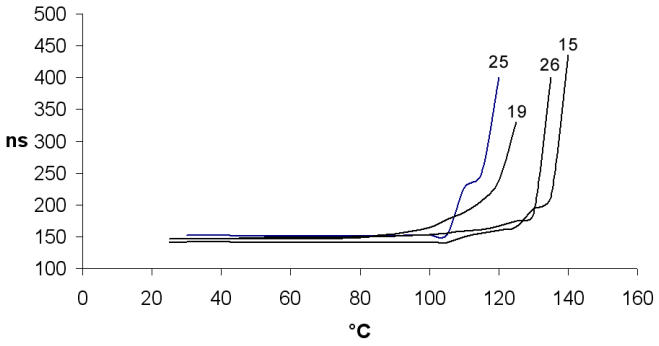

Fig. 6. Critical path length vs. temperature

and rapid deterioration of t_{pd} was not found. Note that the experiment was performed for V_{dd} = 3.3V on several randomly selected particular chips (S/N 15, 19, 25 and 26 – see Table III for details). The results of experiments show that there are no significant differences among chips under 100 °C. Beyond this point, some chips remain working relatively fast up to 120 °C or even more, but some particular pieces becomes quite slow.

TABLE III
CRITICAL PATH LENGTH VS. TEMPERATURE

S/N:	25	26	15	19
T[°C]	t_{pd}[ns]	t_{pd}[ns]	t_{pd}[ns]	t_{pd}[ns]
25			141	146
30	151.9		141.5	146
35	151.7		141.5	146
40	151.6		141.4	146
45	151.5	148	141.3	146
50	151.5	148.1	141.2	146
55	151.4	148.2	141.2	146
60	151.3	148.3	141.1	146
65	151.2	148.4	141	146
70	151.2	148.6	140.9	147
75	151.2	148.9	140.8	148
80	151.2	149.3	140.7	149
85	151.3	149.9	140.6	152
90	151.5	150.7	140.6	154
95	151.9	151.9	140.5	159
100	152.6	153.3	140.5	165
105	153.6	155.6	140.6	177
110	227	158.6	150.2	188
115	250	161.3	156	206
120	400	167.4	159.8	238
125		175	165.7	330
130		184.6	193.6	
135		400	210.8	
140			435.6	

IV. CONCLUSIONS

In the paper, a number of new experiments with previously fabricated REPOMO32 reconfigurable polymorphic chip are presented. These experiments were focused on behavior of the chip under wide range of operating temperatures. For these purposes, special equipment (REPOMO32 kit with regulated heating chamber) was designed. During the course of experiments, some interesting and promising facts were investigated in detail. First, the hypothesis that the simple (composed of

8 transistors only) polymorphic gate, sensitive to V_{dd}, can be easily involved (in terms of functionality) not only by V_{dd}, but also by temperature, was confirmed. In addition, the point of instantaneous function changing caused by temperature change can be adjusted very easily. It enables a lot of new potential applications of such kind of polymorphic gates e.g. in the area of dependable systems (see [7], [16]).

In some specific situations (e.g. under critical circumstances, in emergency), it may be useful to reduce level of service (rather than experiencing a complete failure). This requires some kind of reconfiguration. Thus, properties of polymorphic electronics may be useful. The reason, for which a service reduction (and reconfiguration evoked by this) must be performed, could be e.g. when temperature rises up (cooling system is not able to keep the device cool, e.g. outer temperature is high at the moment). But there is still an expectation of improvement in the future (outer temperature falls down). So the device may be able to reduce its functionality under bad circumstances and restore it back when the environment goes better as smart as possible and the cost of such adaptability or fault-tolerance must be low. It also expects environment sensing. In such situations, polymorphic electronics may be a good choice.

Secondly, experiments have proved that the physical design of the REPOMO32 chip is robust enough to keep the functionality of all support circuitry and glue logic as well as the set of ordinary gates in CLEs under wide range of operating temperature (all circuitry besides polymorphic gates remains functional for the whole temperature range).

Third, the experiments clearly shown that dynamic parameters are stable enough (see Figure 6) to design polymorphic digital circuits controlled by temperature, that exploit relatively high operating frequency (from this perspective, the term high means the frequency typical for this kind of experimental chips).

Future plans are concentrated around the idea to design an experimental digital polymorphic circuit that demonstrates utilisation of temperature-sensitive polymorphic gates for some kind of practical application.

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