

# Reduction of Test Vectors Number based on Parasitic Capacity Extraction of Scan Chain Wires

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**Abstract.** In this paper, method for scan chain optimisation performed after physical layout is presented. It is shown how the method can be used to decrease the number of test vectors. The principles of the method are based on parasitic capacity extraction, eliminating some bridging faults in the physical layout and subsequent reduction of the number of test vectors needed to test the circuit. The method was verified on circuits from benchmark set, experimental results are provided and discussed. It is expected that the method can be used in mass production of electronic components.

**Keywords:** scan chain, reorganization, reordering, test, vector, bridge

## 1 Introduction

Even today's advanced manufacturing technologies do not guarantee that each produced circuit is fault-free because the manufacturing processes are not absolutely precise. There is almost always a small part of faulty ones in a set of manufactured circuits. So each circuit has to be tested and possibly taken out immediately after the production because it is significantly cheaper than to sell a faulty circuit to a customer and suffer a consequences in future.

If a circuit is simple enough, it can be tested through its primary inputs and outputs, but for complex circuits containing high number of internal components this approach can not be used because it is impossible to control and observe these internal components. In this case the circuit design has to be modified according to DfT (Design for Testability) rules and an additional logic called scan chain is included.

When scan chain is included into circuit<sup>1</sup>, each flip-flop existing in the circuit supposed to form scan chain is replaced by its scan version<sup>2</sup>. Then, these scan flip-flops can be connected into serial shift register in test mode, this serial shift register is denoted to as *scan chain* through which test vectors and responses to them are transported.

The order of the flip-flops in scan chain after synthesis is done on the level of logical structure and can be changed in different ways because the reordering does not change the function of the circuit and has no impact on testability parameters as well.

Various scan chain reordering methods exist, e.g. methods to reduce power dissipation during test application [5], [8], methods to improve coverage of delay faults [6] and most often used methods to simplify the process of routing [7]. It is evident that various objectives can be defined to reorganize the scan chain.

In our research, we deal with the idea of reducing the number of test vectors needed to verify proper function of a circuit. We try to improve *routing of scan chain wires* so that the number of faults which must be tested decreases and then the number of test vectors to recognize them decreases as well.

The structure of the paper is as follows. First, procedures of test vectors set generation are described. Then the dependence of potential bridging faults number on wire length is presented. In the 4th section, principles of the method are explained and the experimental results and conclusion are provided at the end of the paper.

## 2 Test Vectors Generating

There may appear various types of faults in a circuit. The most frequently fault model is the stuck-at fault when a wire in the circuit is unintentionally stucked at one logic value. Test vectors must be then generated to test these faults, ATPG (Automatic Test Pattern Generation) tool is used for this purpose. The number of generated test vectors is usually lower when compared to test generated to test bridging faults, In this paper we do not focus on stuck-at faults.

A bridge (defect causing a bridging fault) can be defined as unintended connection between two or more otherwise unconnected nets. Although a large number of bridges can be detected by Stuck-at fault patterns, in general stuck-at fault model does not adequately represent all possible bridges in an electronic component. To be able to detect bridge defects more efficiently, a bridging fault model must to be used.

When we talk about bridging fault model then it is important to realize that a connection between two nets in a device is modelled, the connection causes the faulty behaviour. In each net pair four faults can be recognized, for these four faults a test must be developed to avoid a bridge defect (00, 10, 01 or 11

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<sup>1</sup> usually immediately after synthesis

<sup>2</sup> each flip-flop cell in core library has non-scan and scan version. The scan version includes a multiplexer which allows switching between functional input D and scan input SDI based on "scan enable" signal.

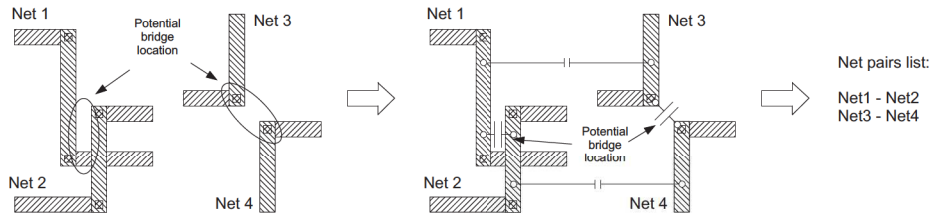


Fig. 1. Possible bridge defect locations.

faults). In addition to the fault model, the potential nets pair list that could be potentially bridged together need to be provided to the ATPG tool. However, the bridging fault list is about the square of the number of all nets inside the design so it is not suitable to test them all and some method selecting only the net pairs with the highest probability to have bridge defects is needed.

The net pairs that have the highest probability to have bridge defects are those nets which are physically near to others nets, the nets pair list is generated by analysing the physical design layout.

One of the possible ways to extract the potential list of nets that are likely to bridge is to extract the list of the bigger intra-layer cross-capacitance. The following figure 1 illustrates the bridge locations and the capacitances.

The bridging ATPG algorithm generates patterns that bring the two nets to the same and to the opposite values in order to detect the short created by the bridge defect (see figure 2).

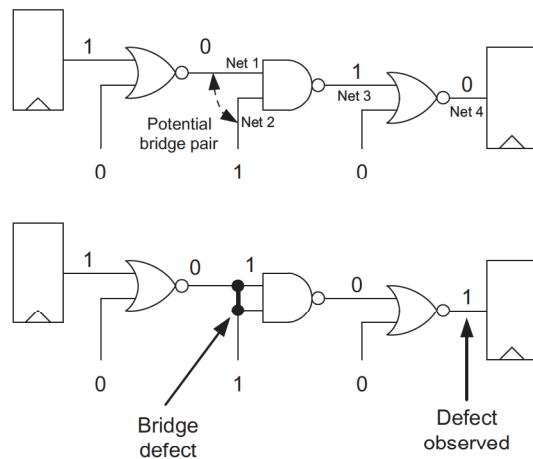


Fig. 2. A bridge defect detection example.

Due to a more logic combination needed, the number of test vectors to test bridging faults is much bigger than to test stuck-at faults.

When test vectors are generated by ATPG tool, the test vectors for bridging faults are generated first. Then a simulation of these vectors is performed to achieve a stuck-at faults coverage of these vector. In most cases these bridging fault test vectors cover also most of stuck-at faults and only a few test vectors for remaining stuck-at faults are generated.

So reducing the number of potential bridge defects can reduce the number of test vectors significantly, therefore it is reasonable to focus on this defect type.

### 3 Dependence of Potential Bridges Number on Wire Length

As shown above, the number of how many times is the net included in potential bridge defects list increases with the increasing number of net crossings and with the increasing number of nets placed close each other. It can be hypothesised that if a wire is long and/or incorrectly routed, the danger of bridge defect is bigger. It was shown in our previous work [4] that this hypothesis is correct.

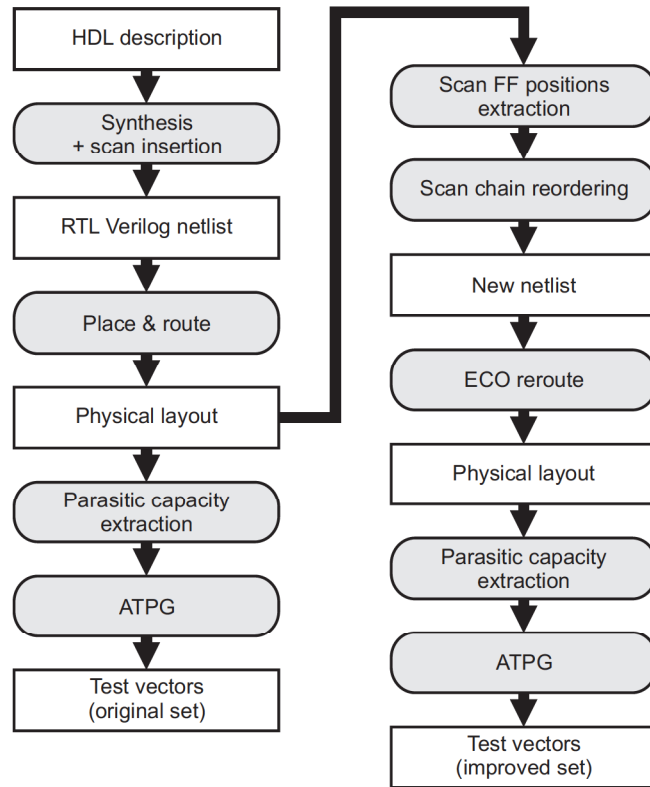
To summarize, to reduce the number of potential bridge defects and as a consequence to reduce the number of test vectors, it is necessary to shorten wires as much as possible and eventually improve routing. But it is hardly to do it with functional logic, because its routing is highly dependent on timing constraints. Anyway, it does not matter how the scan chain is reordered. Thus, it can be stated that an alternative to reduce the number of potential bridge defects through scan reorganization exists. The usual share of scan chain nets in all nets of a circuit is about 5–15% so it is a relatively significant number of nets which can be modified to achieve the above mentioned goals.

It is rather difficult to improve the routing of a net and avoid mutual approaching with other nets due to more difficult routing in this situation and chip size. But the scan chain wires can be shortened so that the scan chain flip-flops are connected to each other as close as possible. When a wire becomes shorter, the number of crossings or approachings to other nets becomes smaller and as a consequence the number of net pairs appearing in the potential bridge defects list becomes smaller.

### 4 Description of the Method

The scan chain reordering cannot be done immediately after synthesis, i. e. in the situation when scan chain is included into design. The reason for this statement is such that the scan chain is included in a logical design phase and the physical locations of flip-flops is not known yet. This can be done after placing process. So the whole design process flow has to be changed as follows (see figure 3).

The scan chain reordering process in our method is based on formalizing the scan chain into a mathematical graph, where the scan chain flip-flops are



**Fig. 3.** Modified complete design process flow.

represented by graph nodes and the interconnecting wires by edges. The scan chain is represented by a path in the graph.

When transforming flip-flop positions into graph nodes, edges from each flip-flop to all the flip-flops are generated. Each edge is weighted by a Manhattan distance between relevant flip-flops.

The reordering process can be transformed to traveling salesman problem (TSP), which is NP-hard problem [3], but it is well known that many heuristic solvers have been developed. We chose the Concorde solver [2] which is regarded as the fastest TSP solver for large instances.

After the scan chain reordering process is finished, the original netlist is altered and then a routing process is performed. At the end of the design process the parasitic capacitances extraction process is performed and the test vectors are generated by an ATPG tool.

## 5 Experimental Results

In our previous work [4] we experimentally proved that the decrease in the number of scan chain wires lengths reduces the number of test vectors, but we experimented with only four real circuits and we admit that they did not differ significantly from each other. We have been asked to do more experiments with circuits of significantly different sizes to prove that the method is applicable generally.

In this paper we presents the results of additional experiments when the method was applied to the benchmark set of circuits ITC'99 [1] containing circuits of different sizes acquired from industrial companies. According this, the method can compared to any of similar methods.

From the ITC'99 benchmark set of circuits, we chose several circuits of different sizes from very small one (49 gates) to large one (231 320 gates). The method was applied to these chosen circuits in order to prove that the method works with different sizes of circuits. The results of the method application compared to design process results without the method application are available in the following table 1.

**Table 1.** Results of the Experiment

<b>Circuit</b>	<b>b01</b>	<b>b05</b>	<b>b07</b>	<b>b12</b>	<b>b15</b>	<b>b17</b>	<b>b19</b>
<b>GATES</b>	49	998	441	1 076	8 922	32 326	231 320
<b>FF</b>	5	34	49	121	449	1 415	6 642
<b>SC</b>	1	1	1	1	1	2	6
Results without the method applied:							
<b>BD</b>	746	10 116	7 456	37 900	235 296	735 218	5 724 460
<b>TV</b>	40	204	174	436	1 612	2 086	7 528
Results with the method applied:							
<b>BD</b>	742	10 094	7 218	30 654	213 722	696 962	5 234 474
<b>TV</b>	37	201	164	406	1 522	1 913	6 299
<b>Rate</b>	<b>92.5 %</b>	<b>98.5 %</b>	<b>94.3 %</b>	<b>93.1 %</b>	<b>94.4 %</b>	<b>91.7 %</b>	<b>83.7 %</b>

GATES – Number of gates in the circuit.

FF – Number of flip-flops in the circuit.

SC – Number of scan chains.

BD – Number of potential bridge defects found.

TV – Number of test vectors (sum of bridging faults and stuck-at faults vectors).

Ratio – Ratio of the test vectors number without the method applied and the test vectors number with the method applied.

The results prove that the method reduces the number of test vectors in all test cases. Results for very small circuits may not be relevant because of too few options to change the order of flip-flops in the scan chain.



The method is more efficient for large circuits because of better routing and larger reduction of wires' length after application of the method.

## 6 Conclusion

In this paper, the method which can reduce costs of testing by reducing the number of faults for which the circuit must be tested, is presented. This method is based on scan chain reordering to reduce length of connections between flip-flops. To reorder scan chain we used the methodology known as traveling salesman problem and for solving this problem we used the Concorde software package.

The described method was previously tested on several real circuits [4] and this paper deals with testing the method on circuits from ITC'99 set [1]. The experimental results confirmed that the method really reduces the number of bridging faults and the number of test vectors as well.

The method achieves better results for large circuits with more scan chains. This is important for potential industrial deployment, because just these circuits are usually manufactured.

Test vectors number reduction of 5 – 15 % we reached is very significant in mass production because it reduces testing cost and time needed to apply the test. It can increase yield significantly as well.

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