MORE COMPLEX POLYMORPHIC CIRCUITS AND THEIR PHYSICAL IMPLEMENTATION

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ABSTRACT:

This paper is dealing with more complex polymorphic circuits and their physical implementation. The actual experimental setup was based around reconfigurable polymorphic chip REPOMO32 as a target environment, which is primarily designed to be configured (besides the configuration bit stream itself) by means of using the level of power supply voltage (Vdd). A part of polymorphic FIR filter was mapped onto available resources inside REPOMO32 chip. Obtained results indicate feasibility of full-scale implementation with several REPOMO32 chips.

Keywords: FIR Filter, Polymorphic Circuit, REPOMO32, Reconfiguration

1 INTRODUCTION

Nowadays, there undoubtedly exist diverse application areas, where a circuit, which is able to perform different functions in different situations, may be useful. Most simple approach is to design as many different circuits, as the number of functions is actually needed. Then, outputs of these circuits are switched according to currently required function. This approach is perfectly functional, but quite ineffective in terms of overall size. Another way to follow is reconfiguration. This brings more area-efficient design and great flexibility – also circuits that were not prepared during design phase could be implemented (evolvable hardware), but may be less effective in terms of time. Recent outcomes in the field of digital design techniques and components of digital circuits provide yet another conception – so called polymorphic electronics. Polymorphic electronics as a research field was opened by Stoica et al. [1].

Typical polymorphic circuit is designed as a compact structure based on multifunctional components, where its structure remains unchanged for all operation modes and only the function of components changes. This ensures that polymorphic circuits are very area efficient in comparison to conventional multi-function circuits. Polymorphic circuits typically change their function in accordance with the state of an environment. The environment in this particular case is represented by a physical quantity that involves some parameters regularly used in connection with electronic structures – power supply voltage level, voltage level of a signal, temperature etc. [2] In certain applications it may be helpful to introduce new (better than existing) solutions [1][3][4]. Change of the circuit function comes immediately (with no delay) and sensitivity to the environment is embedded to the circuit. Today's applications are

based on unipolar semiconductor transistors but the nature of polymorphic electronics is more general. It is very important for future that the concept of polymorphic electronics is divided into technologically dependent (components, gates) and independent (synthesis techniques, applications) areas, because it could be usable also with future semiconductor technologies (e.g. carbon-based nanotechnology) [5][6]. But also with today's semiconductor technology (CMOS devices) the concept is ready to be applied and may offer some vital benefits to the area of multifunctional digital circuits [7].

Several polymorphic gates have been designed but only two have been actually fabricated so far; remaining polymorphic gates were either simulated or tested in a field programmable transistor array (FPTA-2). For real experiments, the first reconfigurable polymorphic chip in the world was designed and manufactured. The chip is called REPOMO32 (REconfigurable POlymorphic MOdule with 32 configurable elements) [8]. The chip was tested extensively after manufacturing and its special capabilities were also used to demonstrate unique method of chip identification [9].

The paper presents almost first physical implementation of a more complex polymorphic circuit. Due to lack of physical implementations of polymorphic gates, only some simple polymorphic circuits were demonstrated so far [4][7]. Nowadays the existence of a REPOMO32 chips enables us to actually implement and validate some previously proposed applications. In [10] a finite impulse response filters (FIR) was proposed, which are able to reduce their power consumption by reduction of active stages (coefficients). Remaining stages of a filter are "reconfigured" (particularly, coefficients are changed) to achieve as much similar response (to the original filter), as is possible. Of course, the response of the reduced filter is not exactly the same; parameters of the reduced may show slightly worse behavior, but significant reduction of power consumption helps to overcome these imperfections. Main goal of this paper is to clearly demonstrate feasibility of the approach where REPOMO32 modules could be used in order to implement the FIR filter functionality.

2 REPOMO32

2.1 NAND/NOR Polymorphic Gate

Polymorphic gate is an element which performs an elementary logic (Boolean) function, whereas the function may (for the same element) vary in accordance with the particular state of the environment. It is possible to say that the function of the gate is virtually controlled by environment. Mutual collaboration between research teams at Brno University of Technology (The Microelectronics Department at The Faculty of Electrical Engineering and Communication represented by Mr. Roman Prokop and The Faculty of Information Technology) has enabled the creation of polymorphic gate with two inputs, whose function is controlled by supply voltage [4]. The gate will accomplish two primary functions f_1 a f_2. Whereas f_1 needs supply voltage of at least 5 V in order to be executed correctly, function f_2 demands lower supply voltage of 3,3 V which is still, however, quite typical for digital logic circuits. Particular logic functions to be performed were assigned in a following way: f_1 = NAND a f_2 = NOR.

The gate is composed of eight MOS transistors (3 n-MOS a 5 p-MOS). Structure of the gate is shown in Figure 1 (bottom-right). Common NAND or NOR gate built with CMOS technology contains exactly four transistors. The resulting size of the created polymorphic gate seems to be acceptable in this perspective – it has the same "price" as a pair of ordinary CMOS gates. Such finding can be also interpreted as if the polymorphic was replacing two usual gates in some class of applications. But if a pair of two standard gates (consisting of NAND and NOR gate) should replace the aforementioned polymorphic gate in functionally

identical way, it would be necessary to append also detector of supply voltage level and some type of switch. The purpose of this switch would be then to select one of the two standard gates for the output according to the detected supply voltage level. Thus, it's easy to observe the overhead associated with conventional approach.

2.2 Structure of REPOMO32

REPOMO32 is primarily intended for implementation of polymorphic four-input/four-output combinational circuits. As Figure 1 shows, the chip consists of 32 two-input Configurable Logic Elements (CLEs) laid out in an array of 4 rows and 8 columns. A CLE can be programmed to perform one of the following functions: AND, OR, XOR and polymorphic NAND/NOR (described in previous section). When V_{dd} = 3.0–3.8 V, the NAND/NOR gate exhibits the NOR function and when V_{dd} = 3.9–5 V the gate exhibits the NAND function. If the CLE is set to exhibit one of ordinary logic functions, it do not change its logic functions with the changes of V_{dd} within the range of 3–5 V.

REPOMO32's logic behavior is defined by its configuration bits and the level of V_{dd}. The configuration bits control a set of multiplexers which are responsible for interconnecting the CLEs and selecting their logic functions. In total, 8 bits define the configuration of a single CLE. The configuration of the chip is stored in 32 8-bit latch registers. The configuration of a single CLE is performed by supplying CLE's address (addr) and configuration data (data) followed by activating the WE signal. The chip can be completely reconfigured in 32 configuration steps. The primary outputs Z0–Z3 are connected directly to CLEs of the last column. There are no synchronization registers in REPOMO32. The chip has 28 pins and occupies the area of 2900 x 1970 μm. It was fabricated using AMIS CMOS 0.7 μm technology.

The REPOMO32 chip is considered as a small module which may be embedded into a larger system.

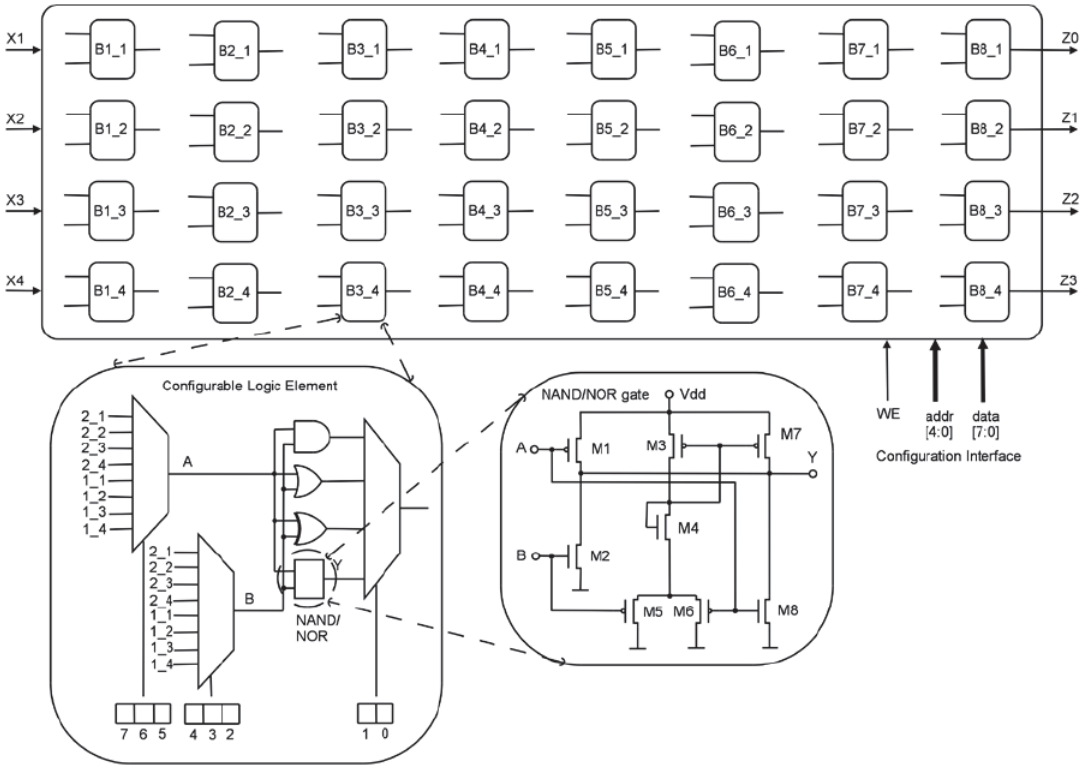

Fig. 1: The REPOMO32 chip, iplementation details of the CLE block and NAND/NOR gate

3 POLYMORPHIC FIR FILTER

Figure 2 shows a polymorphic FIR filter, proposed in [10]. The filter consists of $N - 1$ delay registers, N multiplication units and an N-operand adder which is divided into two subadders whose outputs are summed in the third adder. The filter can operate either in the standard mode or backup mode. The standard mode is used during normal operational conditions of the filter. In that case, the filter is operated as any conventionally created N-tap filter with coefficients b_0–b_{N-1}. In the backup mode, the filter approximates the standard mode using restricted resources. In this mode the filter utilizes only M, where $M < N$ coefficients (b^*_0 –b^*_{M-1}) and $M - 1$ delay registers. Therefore, in the backup mode, original coefficient values b_0–b_{M-1} are reconfigured and unused parts of the filter are disconnected. To reconfigure coefficients, a polymorphic constant multipliers could be used. The mode can be controlled by using either a logic signal (c in Figure 2) or V_{dd} level. If the polymorphic gates are controlled using V_{dd} and unused taps can be disconnected simply by changing V_{dd}, the control signal c is not required and the filter mode can be distinguished by the level of V_{dd}.

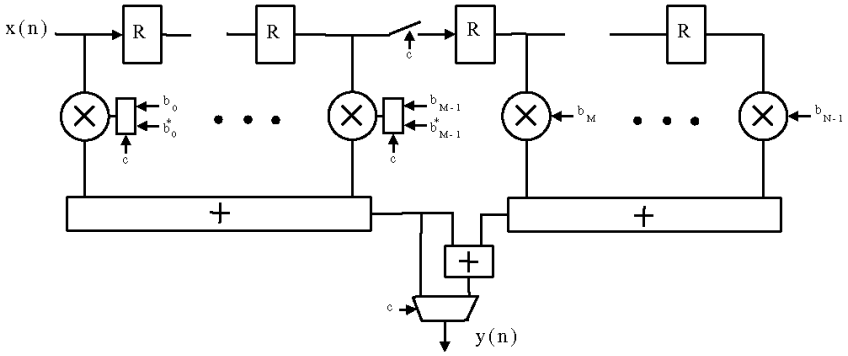

Fig. 2: Circuit Structure of Polymorphic FIR Filter

3.1 Constant Multipliers

Circuits calculating b_i x x in the standard mode and b^*_i x x in the backup mode are implemented using polymorphic and ordinary gates. In addition to ordinary gates, it contains only the polymorphic NAND/NOR gates because only these gates are available in REPOMO32. Figure 3 shows a part of one of them which calculates 240 x x / 32 x x. In the figure, the mapping of the circuit to one REPOMO32 chip is shown (compare to the vacant REPOMO32 structure in Figure 1). CLEs configured as polymorphic are violet ones. Note that outputs y_0–y_3 are always 0 (first "valid" output bit is y_4), outputs called "AUX" are internal signals of the multiplier, they are used for interconnection among other REPOMO32 modules.

3.2 Polymorphic Multiplexer

Also a final multiplexer, which selects between N-tap filter in the standard mode and M-tap filter in the backup mode, could be implemented as a polymorphic circuit. Its circuit structure is described in [11]. If employed polymorphic gates are in the NAND mode, data from A input are passed to the output, for NOR mode, data from B are passed to the output. If used polymorphic gates are V_{dd} sensitive and the multiplexer used at the output of proposed filter (see Figure 2), the mode of the filter (standard/backup) could be controlled by V_{dd}.

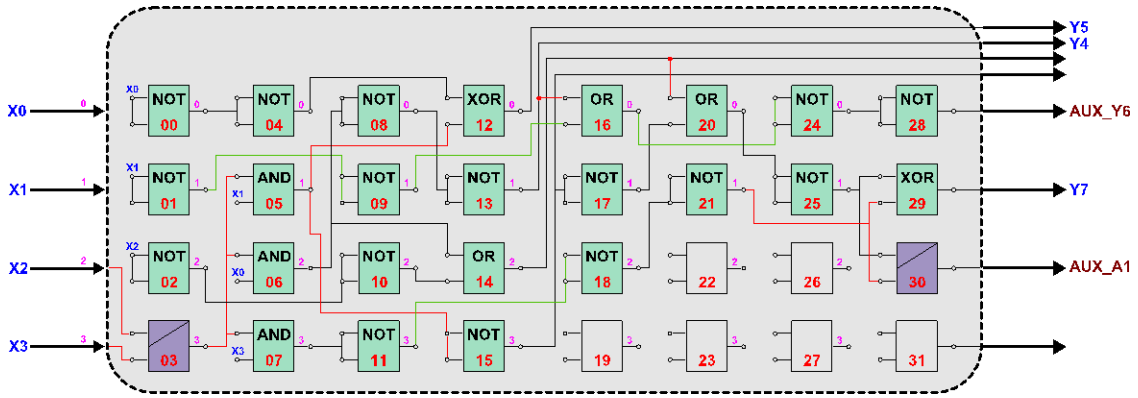

Fig. 3: Part of 240x/32x Polymorphic Constant Multiplier Implemented in REPOMO32

4 EXPERIMENTAL RESULTS

Main intention behind the experimental activities was to put together configuration of REPOMO32 shown on Figure 3, which represents an example of more complex circuit based around combination of conventional and polymorphic gates, and subsequently evaluate its functional properties when deployed into a real chip.

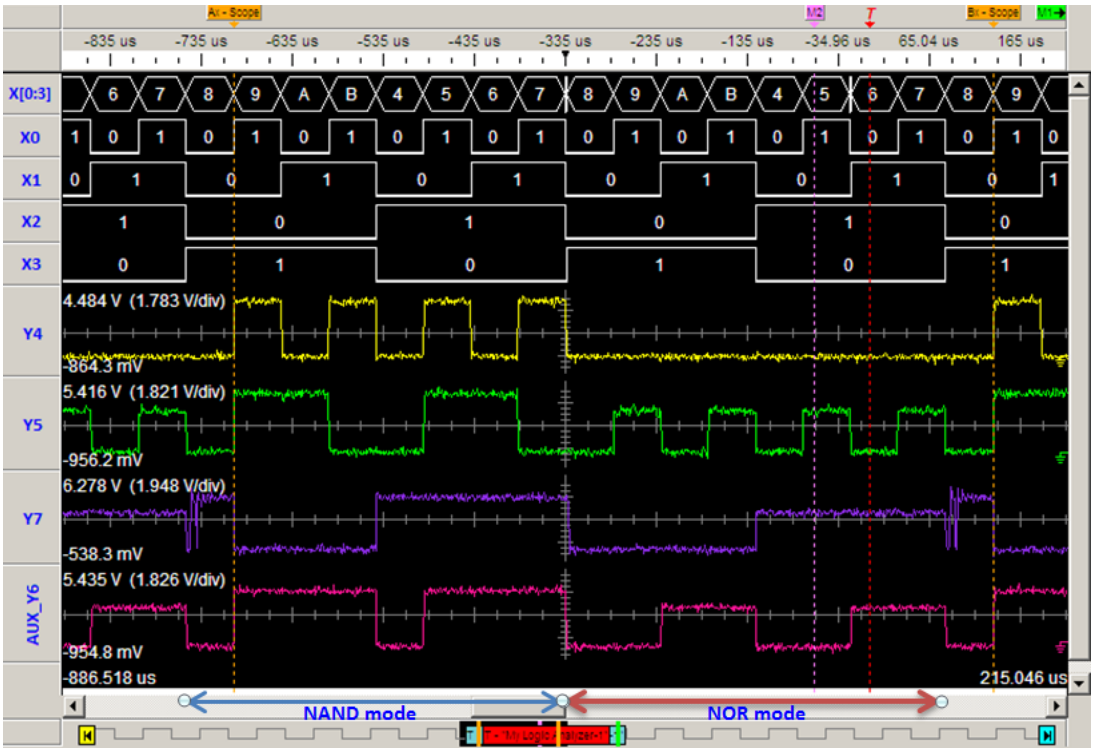

Fig. 4: Behaviour of the Circuitry Implemented in REPOMO32

Signal waveforms depicted on Figure 4 document the behavior of the target circuit. Input stimulus is in this case represented by the signals denoted as *x[0:3]*. For better illustration of polymorphic properties the output signals *y4*, y5, *y7* and *aux_y6* are shown through analog waveforms. One can observe alternation of logic values 1 and 0 within the portion of signal trace that belongs to *y4* where NAND operation mode is active under supply voltage of 5V. Then, circuit enters NOR operating mode with transition of supply voltage to 3.3V and, therefore, signal *y4* hold 0V amplitude till the end of current computational cycle. These two

operating modes can be distinguished in even better way when analyzing amplitudes of the remaining signals, for example *y5*.

5 CONCLUSIONS

The results obtained throughout experimental implementation followed by its analysis have undoubtedly confirmed the implementation feasibility of the initial theoretical concept behind polymorphic FIR filter. Combination of several REPOMO32 chips would finally allow the whole filter to be realized. It's evident that even complex circuit structures of this nature can be successfully mapped onto the relatively constrained resources available in REPOMO32. Advantages of polymorphic electronics were also demonstrated here on a real example.

6 ACKNOWLEDGMENTS

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